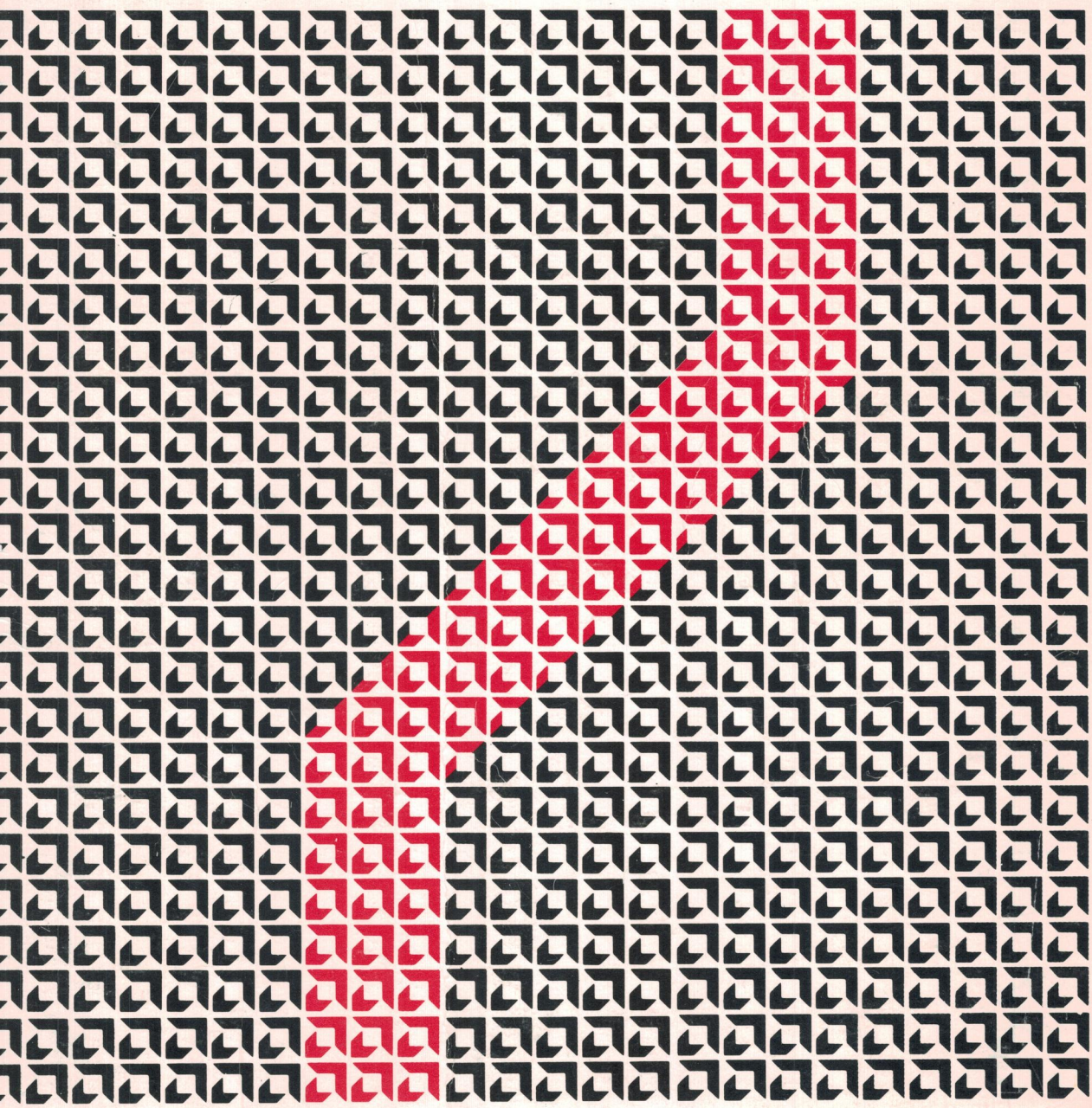
Advanced Micro Devices

The Designers' Guide



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Printed in U.S.A.

The Designers' Choice

Advanced Micro Devices, the newest giant among the major semiconductor manufacturers, offers a product portfolio numbering over 600 complex, monolithic, integrated circuits with emphasis on microprocessors, memories and their related peripheral circuits.

Included herein are selected data sheets and application notes on several recently introduced key AMD® circuits. And, a full set of various indexes and cross reference charts.

Advanced Micro Devices, the Designers' Choice, the company with the commitment – A Commitment to Excellence – where all devices are manufactured in compliance with MIL-STD-883, MIL-M-38510 and MIL-Q-9858.

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PRODUCT ASSURANCE
MIL-M-38510 • MIL-STD-883

The product assurance program at Advanced Micro Devices defines manufacturing flow, establishes standards and controls, and confirms the product quality at critical points. Standardization under this program assures that all products meet military and government agency specifications for reliable ground applications. Further screening for users desiring flight hardware and other higher reliability classes is simplified because starting product meets all initial requirements for high-reliability parts.

The quality standards and screening methods of this program are equally valuable for commercial parts where equipment must perform reliably with minimum field service.

Two military documents provide the foundation for this program. They are:

MIL-M-38510 – General Specification for Microcircuits
MIL-STD-883 – Test Methods and Procedures for Microelectronics

MIL-M-38510 describes design, processing and assembly workmanship guidelines for military and space-grade integrated circuits. All circuits manufactured by Advanced Micro Devices for full temperature range (−55°C to +125°C) operation meet these quality requirements of MIL-M-38510.

MIL-STD-883 defines detail testing and inspection methods for integrated circuits. Three of the methods are quality and processing standards directly related to product assurance:

Test Method 2010 defines the visual inspection of integrated circuits before sealing. By confirming fabrication and assembly quality, inspection to this standard assures the user of reliable circuits in long-term field applications. Standard inspection at Advanced Micro Devices includes all the requirements of the latest revision of Method 2010, condition B.

Test Method 5004 defines three reliability classes of parts. All must receive certain basic inspection, preconditioning and screening stresses. The classes are:

Class C – Used where replacement can be readily accomplished. Screening steps are given in the AMD processing flow chart.

Class B – Used where maintenance is difficult or expensive and where reliability is vital. Devices are upgraded from Class C to Class B by 160-hour burn-in at 125°C followed by more extensive electrical measurements. All other screening requirements are the same.

Class S – Used where replacement is extremely difficult and reliability is imperative. Class S screening selects extra reliability parts by expanded visual and X-ray inspection, further burn-in, and tighter sampling inspection.

All hermetically sealed integrated circuits (military and commercial) manufactured by Advanced Micro Devices are screened to MIL-STD-883, Class C. Molded integrated circuits receive Class C screening except that centrifuge and hermeticity steps are omitted.

Optional extended processing to MIL-STD-883, Class B is available for all AMD integrated circuits. Parts procured to this screening are marked with a "−B" following the standard part number, except that linear 100, 200 or 300 series are suffixed "/883B".

Test Method 5005 defines qualification and quality conformance procedures. Subgroups, tests and quality levels are given for Group A (electrical), Group B (mechanical quality related to the user's assembly environment), Group C (die related tests) and Group D (package related tests). Group A tests are always performed; Group B, C and D may be specified by the user.

MANUFACTURING, SCREENING AND INSPECTION FOR INTEGRATED CIRCUITS

All integrated circuits are screened to MIL-STD-883, Method 5004, Class C; quality conformance inspection where required is performed to Class B quality levels on either Class B or Class C product.

All full-temperature-range (−55°C to +125°C) circuits are manufactured to the workmanship requirements of MIL-M-38510.

The flow chart identifies processing steps as they relate to MIL-STD-883 and MIL-M-38510.

STANDARD PROCESSING CLASS C Steps 1 Through 25

HERMETIC PACKAGE PROCESS

MOLDED PACKAGE PROCESS

1 **INSPECTION**

Purchased or fabricated starting materials are inspected for conformance to specified requirements. Inspection follows written procedures, and records are analyzed for supplier quality negotiations.

2 **WAFER FABRICATION**

Repeated masking, etching and diffusion processes produce finished dice in wafer form.

3 **IN-PROCESS INSPECTION**

Each wafer is inspected prior to irreversible process steps.

4 **FINISHED WAFER INSPECTION**

Sample wafers from each finished diffusion lot are inspected to confirm lot quality before release for test and assembly.

5 **WAFER ELECTRICAL TEST**

Electrical probe test of every die. A computer-controlled system measures static and dynamic parameters and identifies dice that do not meet electrical requirements.

6 **DIE SEPARATION**

Wafers are separated into individual dice and electrical rejects are removed.

7 **VISUAL INSPECTION**

Separated dice are inspected and selected at high magnification.

8 **QUALITY INSPECTION**

Decisions at the 100% inspection are reviewed through periodic random sampling, confirming product quality and revealing any need for operator retraining.

9 **DIE ATTACH**

10 **QUALITY INSPECTION**

Strength of die attachment, position of die and visual quality of eutectic wetting are confirmed periodically by inspecting random samples and push-testing the attached dice.

11 **WIRE BOND**

Hermetic: Aluminum wires, ultrasonic bonding.
Molded: Gold wires, thermocompression bonding.

12 **QUALITY INSPECTION**

Weld strength, bond size and position, wire dress and general workmanship are confirmed periodically by comparing random samples with assembly instructions and quality standards. Bond strength is plotted on statistical control charts, providing early warning of process drifts.

13 **INTERNAL VISUAL INSPECTION**

Assembled but unsealed units are individually inspected at low and high power.

QUALITY STANDARDS:

All devices – MIL-STD-883, Method 2010, Condition B (latest revision). Full temperature devices – MIL-M-38510, Para. 3.7 for workmanship (re-bonding limits).

14 **QUALITY INSPECTION**

Decisions at the 100% inspection are reviewed through periodic random sampling, providing confirmation of product quality and revealing any need for operator retraining.

15a **FINAL SEAL**

(Hermetic devices)

15b **ENCAPSULATE**

(Molded Devices)

16 **HIGH TEMPERATURE STORAGE**

MIL-STD-883, Method 1008, Cond. C: 150°C, 24 hr

17 **TEMPERATURE CYCLE**

MIL-STD-883, Method 1010, Cond. C: −65°C, +150°C, 10 cycles

18 **CENTRIFUGE**

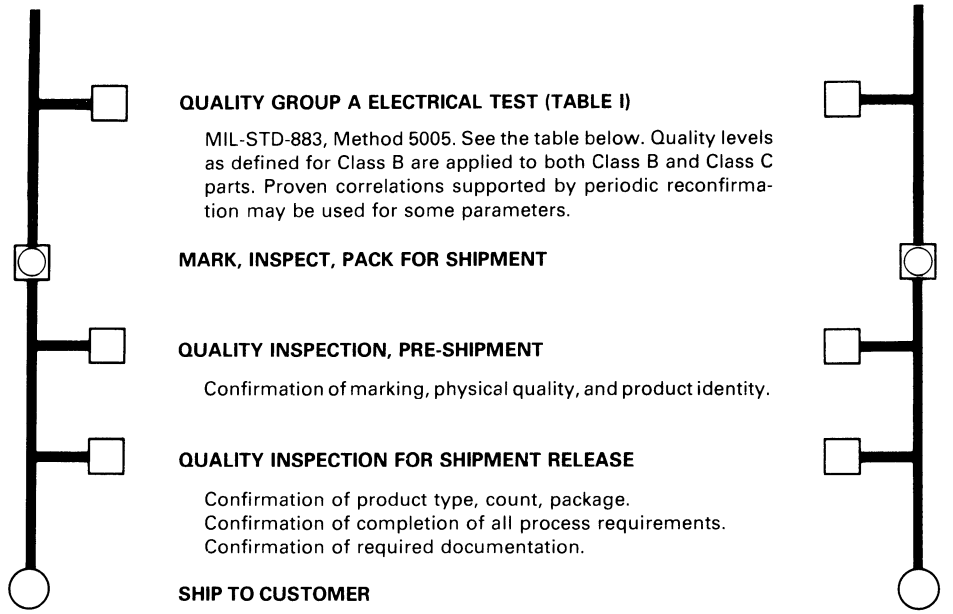
MIL-STD-883, Method 2001, Cond. E: 30,000 G

19 **SEAL (HERMETICITY) TEST**

MIL-STD-883, Method 1014, Cond. A or B: Fine Leak
MIL-STD-883, Method 1014, Cond. C2: Gross Leak

20 **ELECTRICAL TEST**

MIL-STD-883, Method 5004, Para. 3.1.12: Static, dynamic, functional tests at 25°C or in certain products at the most critical extreme temperature to assure accuracy of device selection.



21 **QUALITY GROUP A ELECTRICAL TEST (TABLE I)**

MIL-STD-883, Method 5005. See the table below. Quality levels as defined for Class B are applied to both Class B and Class C parts. Proven correlations supported by periodic reconfirmation may be used for some parameters.

22 **MARK, INSPECT, PACK FOR SHIPMENT**

23 **QUALITY INSPECTION, PRE-SHIPMENT**

Confirmation of marking, physical quality, and product identity.

24 **QUALITY INSPECTION FOR SHIPMENT RELEASE**

Confirmation of product type, count, package.
Confirmation of completion of all process requirements.
Confirmation of required documentation.

25 **SHIP TO CUSTOMER**

This AMD standard product meets screening requirements of MIL-STD-883, Class C.

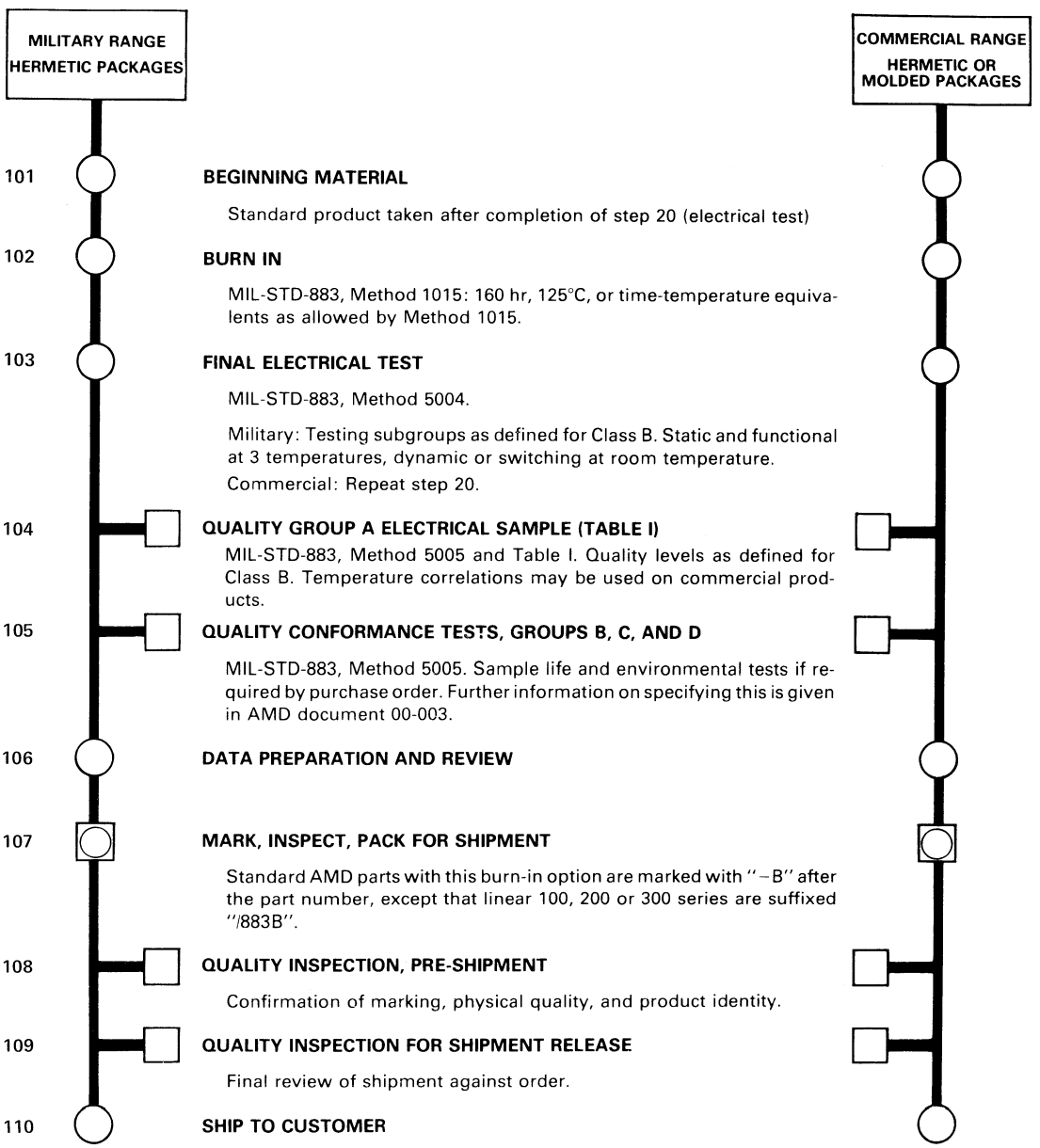
GROUP A ELECTRICAL TESTS
From MIL-STD-883, Method 5005, Table I

Subgroups	LTPD (Note 1)	Initial Sample Size
Subgroup 1 – Static tests at 25°C	5	45
Subgroup 2 – Static tests at maximum rated operating temperature	7	32
Subgroup 3 – Static tests at minimum rated operating temperature	7	32
Subgroup 4 – Dynamic tests at 25°C – Linear devices	5	45
Subgroup 5 – Dynamic tests at maximum rated operating temperature – Linear devices	7	32
Subgroup 6 – Dynamic tests at minimum rated operating temperature – Linear devices	7	32
Subgroup 7 – Functional tests at 25°C	5	45
Subgroup 8 – Functional tests at maximum and minimum rated operating temperatures	10	22
Subgroup 9 – Switching tests at 25°C – Digital devices	7	32
Subgroup 10 – Switching tests at maximum rated operating temperature – Digital devices (Note 2)	10	10
Subgroup 11 – Switching tests at minimum rated operating temperature – Digital devices (Note 2)	10	10

1. Sampling plans are based on LTPD tables of MIL-M-38510. The smaller initial sample size, based on zero rejects allowed, has been chosen unless otherwise indicated. If necessary, the sample size will be increased once to the quantity corresponding to an acceptance number of 2. The minimum reject number in all cases is 3.
2. These subgroups are usually performed during initial device characterization only.

OPTIONAL EXTENDED PROCESSING
CLASS B
Steps 101 Through 110

Advanced Micro Devices offers several extended processing options to meet customer high-reliability requirements. These are defined in AMD document 00-003. The flow chart below outlines Option B, a 160-hr burn in. Military temperature range devices processed to this flow (in the left column) meet the screening requirements of MIL-STD-883, Class B.



101 **BEGINNING MATERIAL**

Standard product taken after completion of step 20 (electrical test)

102 **BURN IN**

MIL-STD-883, Method 1015: 160 hr, 125°C, or time-temperature equivalents as allowed by Method 1015.

103 **FINAL ELECTRICAL TEST**

MIL-STD-883, Method 5004.

Military: Testing subgroups as defined for Class B. Static and functional at 3 temperatures, dynamic or switching at room temperature.

Commercial: Repeat step 20.

104 **QUALITY GROUP A ELECTRICAL SAMPLE (TABLE I)**

MIL-STD-883, Method 5005 and Table I. Quality levels as defined for Class B. Temperature correlations may be used on commercial products.

105 **QUALITY CONFORMANCE TESTS, GROUPS B, C, AND D**

MIL-STD-883, Method 5005. Sample life and environmental tests if required by purchase order. Further information on specifying this is given in AMD document 00-003.

106 **DATA PREPARATION AND REVIEW**

107 **MARK, INSPECT, PACK FOR SHIPMENT**

Standard AMD parts with this burn-in option are marked with "–B" after the part number, except that linear 100, 200 or 300 series are suffixed "/883B".

108 **QUALITY INSPECTION, PRE-SHIPMENT**

Confirmation of marking, physical quality, and product identity.

109 **QUALITY INSPECTION FOR SHIPMENT RELEASE**

Final review of shipment against order.

110 **SHIP TO CUSTOMER**

Military temperature range parts meet screening requirements of MIL-STD-883, Class B.

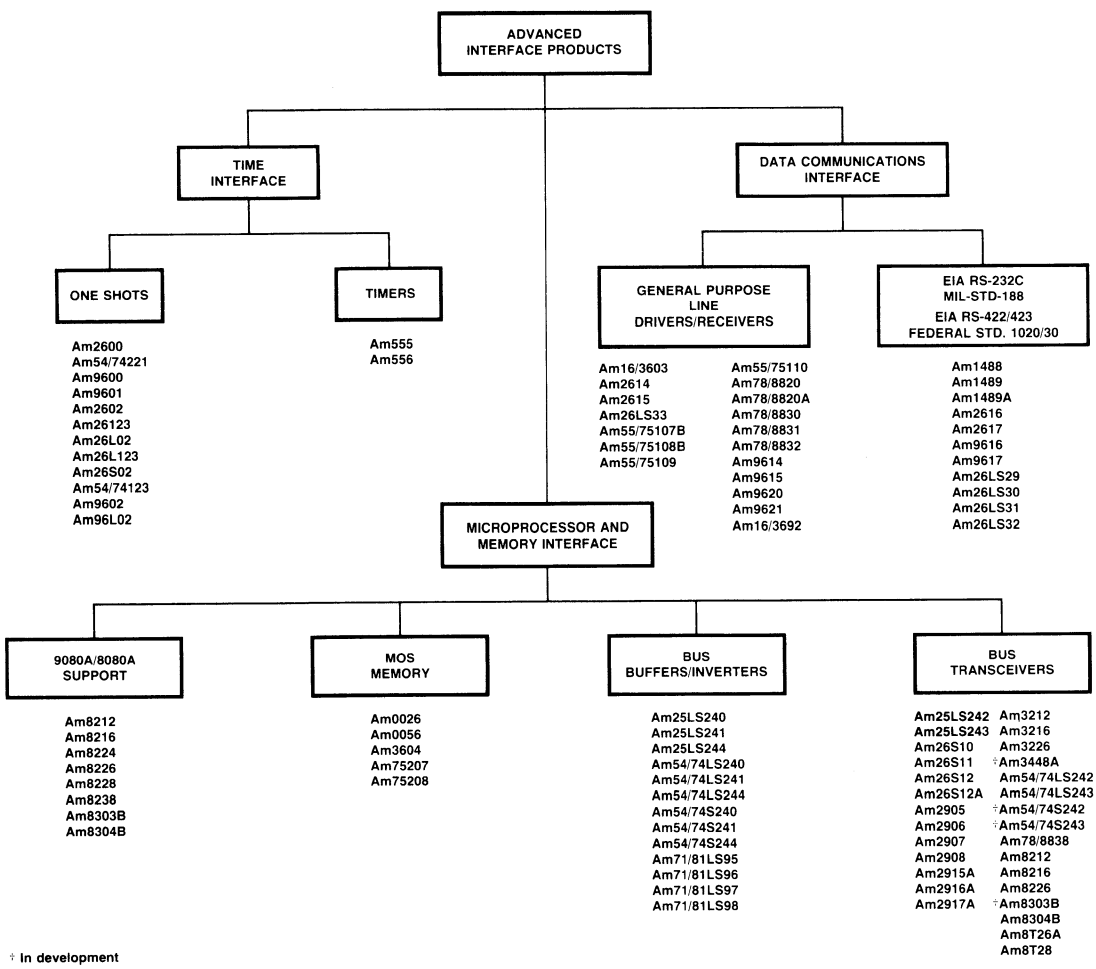
OTHER OPTIONS

Document 00-003, "Extended Processing Options", further defines Option B as well as other screening or sampling options available or special order. Available options are listed here for reference.

Option	Description	Effect
A	Modified Class A screen (Similar to Class S screening)	Provides space-grade product, following most Class S requirements of MIL-STD-883, Method 5004.
B	160-hr operating burn in	Upgrades a part from Class C to Class B.
X	Radiographic inspection (X-ray)	Related to Option A. Provides limited internal inspection of sealed parts.
S	Scanning Electron Microscope (SEM) metal inspection	Sample inspection of metal coverage of die.
V	Preseal visual inspection to MIL-STD-883, Method 2010, Cond. A	More stringent visual inspection of assemblies and die surfaces prior to seal.
P	Particle impact noise (PIN) screen with ultrasonic detection.	Detects loose particles of approximately 0.5 mil size or larger, which could affect reliability in zero-G or high vibration applications.
Q	Quality conformance inspection (Group B, C and D life and environmental tests)	Samples from the lot are stressed and tested per Method 5005. The customer's order must state which groups are required. Group B destroys 16 devices; Group C, 92 devices; Group D, 60 devices.

Product Guides and Cross References

Interface Circuits



† In development

ALPHA NUMERIC CROSS REFERENCE

This list includes devices which can be replaced directly by an Advanced Micro Devices product. In some cases an alternate source vendor may not choose to use the same part number as the original manufacturer. To minimize the number of marking options we recommend ordering the device by the original source designation, as noted in this list.

DEVICE	DESCRIPTION	ORDER #
Am25LS240	Octal Inverting Buffer/Driver	AM25LS240
Am25LS241	Octal Non-Inverting Buffer/Driver	AM25LS241
Am25LS242	Quad Inverting Transceiver	AM25LS242
Am25LS243	Quad Non-Inverting Transceiver	AM25LS243
Am25LS244	Octal Non-Inverting Buffer/Driver	AM25LS244
Am2600	One-Shot	AM2600
Am2602	Dual One-Shot	AM2602
Am2614	Quad Line Driver	AM2614
Am2615	Dual Line Receiver	AM2615
Am2616	EIA/MIL 188C Quad Line Driver	AM2616
Am2617	EIA Quad Line Receiver	AM2617
Am26123	Dual One-Shot	AM26123
Am26L02	Low-Power, Dual One-Shot	AM26L02
Am26L123	Low-Power, Dual One-Shot	AM26L123
Am26LS29	Quad EIA RS-423 Line Driver	AM26LS29
Am26LS30	EIA RS-422/423 Line Driver	AM26LS30
Am26LS31	Quad Differential Line Driver	AM26LS31
Am26LS32	Quad Line Receiver EIA RS-422/423	AM26LS32
Am26LS33	Quad Line Receiver	AM26LS33
Am26S02	Dual One-Shot	AM26S02
Am26S10	Quad Inverting Bus Transceiver	AM26S10
Am26S11	Quad Non-Inverting Bus Transceiver	AM26S11
Am26S12	Quad Bus Transceiver (Hysteresis)	AM26S12
Am26S12A	Quad Bus Transceiver (Hysteresis)	AM26S12A
Am2905	Quad LSI Bus Transceiver – O.C.	AM2905
Am2906	Quad LSI Bus Transceiver – O.C.	AM2906
Am2907	Quad LSI Bus Transceiver – O.C.	AM2907
Am2908	Quad LSI Bus Transceiver – O.C.	AM2908
Am2915A	Quad LSI Bus Transceiver – Three-State	AM2915A
Am2916A	Quad LSI Bus Transceiver – Three-State	AM2916A
Am2917A	Quad LSI Bus Transceiver – Three-State	AM2917A
†DP7303B	Octal Inverting Transceiver	DP7303B
†DP7304B	Octal Bidirectional Transceiver	DP7304B
Am8212	8-Bit I/O Port for 9080A/8080A	AM8212
Am8216	Quad Bus Driver for 9080A/8080A	AM8216
Am8224	Clock Generator for 9080A/8080A	AM8224
Am8226	Quad Bus Inverter for 9080A/8080A	AM8226
Am8228	System Controller for 9080A/8080A	AM8228
Am8238	System Controller for 9080A/8080A	AM8238
DM54123	Dual One-Shot	SN54123
DM71LS95	Octal Non-Inverting Buffer/Driver	DM71LS95
DM71LS96	Octal Inverting Buffer/Driver	DM71LS96
DM71LS97	Octal Non-Inverting Buffer/Driver	DM71LS97
DM71LS98	Octal Inverting Buffer/Driver	DM71LS98
DM74123	Dual One-Shot	SN74123
DM7820	Dual Differential Line Receiver	DM7820
DM7820A	Dual Differential Line Receiver	DM7820A
DM7830	Dual Differential Line Receiver	DM7830
DM7831	Three-State Line Driver	DM7831
DM7832	Three-State Line Driver	DM7832
DM81LS95	Octal Non-Inverting Buffer/Driver	DM81LS95
DM81LS96	Octal Inverting Buffer/Driver	DM81LS96
DM81LS97	Octal Non-Inverting Buffer/Driver	DM81LS97
DM81LS98	Octal Inverting Buffer/Driver	DM81LS98
DM8601	One-Shot	9601*C
DM8602	Dual One-Shot	9602*C
DM8820	Dual Differential Line Receiver	DM8820
DM8820A	Dual Differential Line Receiver	DM8820A
DM8830	Dual Differential Line Driver	DM8830
DM8831	Three-State Line Driver	DM8831
DM8832	Three-State Line Driver	DM8832
DM9601	One-Shot	9601*M
DM9602	Dual One-Shot	9602*M
DP8303B	Octal Inverting Transceiver	DP8303B
DP8304B	Octal Bidirectional Transceiver	DP8304B
DS0026	Two Phase MOS Clock Driver	MH0026
DS0026C	Two Phase MOS Clock Driver	MH0026C
DS0056	Two Phase MOS Clock Driver	DS0056
DS0056C	Two Phase MOS Clock Driver	DS0056C
DS1488	Quad EIA Line Driver	MC1488
DS1489	Quad EIA Line Receiver	MC1489
DS1489A	Quad EIA Line Receiver	MC1489A
DS1603	Dual Differential Line Receiver	DS1603

DEVICE	DESCRIPTION	ORDER #
DS1691	EIA RS-422/423 Line Driver	AM26LS30
DS1692	Dual Differential Driver	DS1692
DS3603	Dual Differential Line Receiver	DS3603
DS3604	Dual MOS Sense Amp	DS3604
DS3691	EIA RS-422/423 Line Driver	AM26LS30
DS3692	Dual Differential Driver	DS3692
DS55107	Dual Differential Line Receiver	SN55107B
DS55108	Dual Differential Line Receiver	SN55108B
DS55109	Dual Differential Line Driver	SN55109
DS55110	Dual Differential Line Driver	SN55110
DS75107	Dual Differential Line Receiver	SN75107B
DS75108	Dual Differential Line Receiver	SN55108B
DS75109	Dual Differential Line Driver	SN75109
DS75110	Dual Differential Line Driver	SN75110
DS7820	Dual Differential Line Receiver	DM7820
DS7820A	Dual Differential Line Receiver	DM7820A
DS7831	Three-State Line Driver	DM7831
DS7832	Three-State Line Driver	DM7832
DS7838	Unified Quad Bus Transceiver	DS7838
DS8820	Dual Differential Line Receiver	DM8820
DS8820A	Dual Differential Line Receiver	DM8820A
DS8830	Dual Differential Line Receiver	DM8830
DS8831	Three-State Line Driver	DM8831
DS8832	Three-State Line Driver	DM8832
DS8838	Unified Quad Bus Transceiver	DS8838
LM163	Dual Differential Line Receiver	DS1603
LM363	Dual Differential Line Receiver	DS3603
LM363A	Dual MOS Sense Amp/Line Receiver	DS3604
LM555	Precision Timer	SE555
LM555C	Precision Timer	NE555
LM556	Dual Precision Timer	SE556
LM556C	Dual Precision Timer	NE556
LM1488	Quad EIA Line Driver	MC1488
LM1489	Quad EIA Line Receiver	MC1489
LM1489A	Quad EIA Line Receiver	MC1489A
LM55107	Dual Differential Line Receiver	SN55107B
LM55108	Dual Differential Line Receiver	SN55108
LM55109	Dual Differential Line Driver	SN55109
LM55110	Dual Differential Line Driver	SN55110
LM75107	Dual Differential Line Receiver	SN75107B
LM75108	Dual Differential Line Receiver	LM75108B
LM75109	Dual Differential Line Driver	SN75109
LM75110	Dual Differential Line Driver	SN75110
LM7520	Dual Sense Amp; ±4mV Threshold	SN7520
LM7521	Dual Sense Amp; ±7mV Threshold	SN7521
LM7524	Dual Sense Amp; ±4mV Threshold	SN7524
LM7525	Dual Sense Amp; ±7mV Threshold	SN7525
LM75325	Core Memory Driver	SN75325
MC1455	Precision Timer	NE555
MC1488	Quad EIA Line Driver	MC1488
MC1489	Quad EIA Line Receiver	MC1489
MC1489A	Quad EIA Line Receiver	MC1489A
MC1555	Precision Timer	SE555
†MC3448A	IEEE-488 Quad Transceiver	MC3448A
MC3456	Dual Precision Timer	NE556
MC3556	Dual Precision Timer	SE556
MC8601	One-Shot	9601*C
MC8602	Dual One-Shot	9602*C
MC9601	One-Shot	9601*M
MC9602	Dual One-Shot	9602*M
MC55107	Dual Differential Line Receiver	SN55107B
MC55108	Dual Differential Line Receiver	SN55108B
MC55109	Dual Differential Line Driver	SN55109
MC55110	Dual Differential Line Driver	SN55110
MC75107	Dual Differential Line Receiver	SN75107B
MC75108	Dual Differential Line Receiver	SN75108B
MC75109	Dual Differential Line Driver	SN75109
MC75110	Dual Differential Line Driver	SN75110
MH0026	Two-Phase MOS Clock Driver	MH0026
MH0026C	Two-Phase MOS Clock Driver	MH0026C
MMH0026	Two-Phase MOS Clock Driver	MMH0026
MMH0026C	Two-Phase MOS Clock Driver	MMH0026C
N8T22	One-Shot	9601*C

ALPHA NUMERIC CROSS REFERENCE (Cont.)

DEVICE	DESCRIPTION	ORDER #
N8T26	Quad Three-State Bus Transceiver	N8T26
N8T26A	Quad Three-State Bus Transceiver	N8T26A
N8T28	Quad Three-State Bus Transceiver	N8T28
NE555	Precision Timer	NE555
NE556	Dual Precision Timer	NE556
S8T22	One-Shot	9601*M
S8T26	Quad Three-State Bus Transceiver	S8T26
†S8T26A	Quad Three-State Bus Transceiver	S8T26A
†S8T28	Quad Three-State Bus Transceiver	S8T28
SE555	Precision Timer	SE555
SE556	Dual Precision Timer	SE556
SN52555	Precision Timer	SE555
SN54123	Dual One-Shot	SN54123
SN54221	Dual One-Shot	SN54221
SN54S240	Octal Inverting Buffer/Driver	†SN54S240
SN54S241	Octal Non-Inverting Buffer/Driver	†SN54S241
†SN54S242	Octal Inverting Buffer/Driver	†SN54S242
†SN54S243	Octal Non-Inverting Buffer/Driver	†SN54S243
SN54S244	Octal Inverting Buffer/Driver	†SN54S244
SN55107A	Dual Differential Line Receiver	SN55107B
SN55107B	Dual Differential Line Receiver	SN55107B
SN55108A	Dual Differential Line Receiver	SN55108B
SN55108B	Dual Differential Line Receiver	SN55108B
SN55109	Dual Differential Line Driver	SN55109
SN55110	Dual Differential Line Driver	SN55110
SN55114	Dual Differential Line Driver	9614*M
SN55115	Dual Differential Line Receiver	9615*M
SN55182	Dual Differential Line Receiver	DM7820A
SN55183	Dual Differential Line Receiver	DM7830
SN55369	Two-Phase MOS Clock Driver	MH0026
SN72555	Precision Timer	SN72555
SN74123	Dual One-Shot	SN74123
SN74221	Dual One-Shot	SN74221
SN74LS424	Clock Generator for 9080A/8080A	Am8224
SN74LS240	Octal Inverting Buffer/Driver	SN74LS240
SN74LS241	Octal Non-Inverting Buffer/Driver	SN74LS241
SN74LS242	Quad Inverting Transceiver	SN74LS242
SN74LS243	Quad Non-Inverting Transceiver	SN74LS243
SN74LS244	Octal Non-Inverting Buffer/Driver	SN74LS244
SN74S240	Octal Inverting Buffer/Driver	SN74S240
SN74S241	Octal Non-Inverting Buffer/Driver	SN74S241
†SN74S242	Quad Inverting Transceiver	†SN74S242
†SN74S243	Quad Non-Inverting Transceiver	†SN74S243
SN74S244	Octal Inverting Buffer/Driver	SN74S244
SN75107A	Dual Differential Line Receiver	SN75107B
SN75107B	Dual Differential Line Receiver	SN75107B
SN75108A	Dual Differential Line Receiver	SN75108B
SN75108B	Dual Differential Line Receiver	SN75108B
SN75109	Dual Differential Line Driver	SN75109
SN75110	Dual Differential Line Driver	SN75110
SN74114	Dual Line Driver	9614*C
SN75115	Dual Differential Line Receiver	9615*C
SN75182	Dual Differential Line Receiver	DM8820A
SN75183	Dual Differential Line Receiver	DM8830
SN75188	Quad EIA Line Driver	MC1488
SN75189	Quad EIA Line Receiver	MC1489
SN75189A	Quad EIA Line Receiver	MC1489A
SN75207	Dual MOS Sense Amp/Line Receiver	SN75207
SN75208	Dual MOS Sense Amp/Line Receiver	SN75208
SN75369	Two-Phase MOS Clock Driver	MH0026
3212	8-Bit I/O Port	3212
3216	Non-Inverting Quad Bus Transceiver	3216
3226	Inverting Quad Bus Transceiver	3226
8212	8-Bit I/O Port for 9080A/8080A	AM8212/8212
8216	Non-Inverting Quad Bus Transceiver	8216
8224	Clock Generator for 9080A/8080A	8224
8226	Inverting Quad Bus Transceiver	8226
8228	System Controller for 9080A/8080A	AM8228/8228
8238	System Controller for 9080A/8080A	AM8238/8238
9600	One-Shot	9600
9601	One-Shot	9601
9602	Dual One-Shot	9602
96L02	Low-Power, Dual One-Shot	96L02
9614	Dual Line Driver	9614
9615	Dual Differential Line Receiver	9615
9616	Triple EIA Line Driver	9616
9617	Triple EIA Line Receiver	9617
9620	Dual Differential Line Receiver	9620
9621	Dual Differential Line Driver	9621

†To be announced. * is the package designator position.

SELECTION GUIDE (Cont.)

LINE DRIVERS

DUAL DIFFERENTIAL		Use With
75109	Open collector differential outputs typical current 6mA, inhibit controls	75107B 75108B
75110	12mA output current version of Am75109	75107B 75108B
8830	Designed for single 5.0V supply operation	7820 or 7820A
8831	Dual differential device which may also be used as a quad single-ended driver. Three-state output.	9615 or 2615
8832	Similar to 8831 but no V_{CC} clamp diodes	9615 or 2615
9614	5 volt supply driver with complementary outputs	9615
9621	200mA transient capability with 130Ω back matching resistor	9620
DIFFERENTIAL EIA RS-422, FEDERAL STD 1020		
26LS31	Quad, high-speed, low output skew	26LS32 or
26LS30	Dual, high output CMR	26LS33
SINGLE ENDED		
2614	High-speed quad driver for multi-channel, common ground operation.	2615
SINGLE ENDED, EIA RS-232-C		
1488	Quad EIA RS-232C driver (14 pins)	1489/ 1489A
2616	Quad 16-pin driver for EIA RS-232C, CCITT V.24 and MIL-188C interface	2617
9616	Triple EIA RS-232C driver (14 pins)	9617
SINGLE ENDED, EIA RS-423, FEDERAL STD 1030		
26LS29	Quad, three-state	26LS32 or
26LS30	Quad, mode control	26LS33

BUS BUFFERS/DRIVERS

		t_{pd} (TYP)	I_{OL} (MAX)
25LS240 74LS240 74S240 81LS96	Inverting octal buffer/driver with three-state output	10 10 4.5 9.0	48 24 68 16
25LS241 74LS241 74S241 81LS95	Non-inverting octal buffer/driver with three-state output	12 12 6.0 12	48 24 68 16
25LS242 74LS242 †74S242	Inverting buffer/driver with two quad data paths connected input-to-output	10 10 4.5	48 24 68
25LS243 74LS243 †74S243	Non-inverting buffer/driver with two quad data paths connected input-to-output	12 12 6.0	48 24 68
25LS244 74LS244 74S244 81LS97	Non-inverting octal buffer/driver with three-state output and two inverting enables	12 12 6.0 12	48 24 68 16
81LS98	Inverting octal buffer/driver with three-state output and two inverting enables	9.0	16

†In development

LINE RECEIVERS

DUAL DIFFERENTIAL		Use With
3603	Receiver with differential input to detect signals > 25mV. Three-state outputs.	75110
75107B	Totem-pole TTL output version of Am363	75109 or 75110
75108B	Open collector TTL output version of Am363	75109 or 75110
8820	Designed for ±15V common mode using 5.0V supply	8830
8820A	Higher speed, tighter spec 8820	8830
9615	±15 volt common mode, 5 volt supply receivers with uncommitted collector and active pull-up controls	9614
9620	±15 volt common mode receiver with direct and attenuated inputs	9621
QUAD DIFFERENTIAL		
26LS33	±15 volt common mode, 5 volt supply, three-state output	26LS31
QUAD DIFFERENTIAL EIA RS-422, FEDERAL STD 1020		
26LS32	±7 volt common mode, 5 volt supply, three-state output	26LS31
SINGLE ENDED		
2615	Receiver for 3 volt single-ended TTL level data	2614
SINGLE ENDED, EIA RS-232-C		
1489	Quad EIA RS-232C receiver with input threshold hysteresis	1488
1489A	Higher threshold version of Am1489	1488
2617	Quad EIA RS-232 receiver specified over military temperature range (same pinout as Am1489A)	2616
9617	Triple EIA RS-232 receiver with adjustable hysteresis	9616
SINGLE ENDED, EIA RS-423, FEDERAL STD 1030		
26LS32	±7 volt common mode, 5 volt supply, three-state output	26LS29 26LS30

SELECTION GUIDE (Cont.)

SPECIAL FUNCTIONS

TIMERS	
555	Single, Precision oscillator/timer
556	Dual version 555

MOS MEMORY

DRIVERS	
0026	Dual 5MHz Two-Phase MOS clock driver
0056	0026 with added V_{BB} terminal
SENSE AMPLIFIERS	
3604	Differential input for signals > 10mV, Three-state outputs
75207	Totem-pole TTL output 3604
75208	Open-collector 3604

MOS-MICROPROCESSOR INTERFACE CIRCUITS

8080A/9080A	
8212	8-Bit input/output port, with storage
8216	4-Bit parallel bidirectional bus driver
8224	Clock generator and driver
8226	Inverting version 8216
8228	System controller and bus driver
8238	System controller and bus driver with extended IOW/MEMW
8303B	Two 8226's in one 20 pin package
8304B	Two 8216's in one 20 pin package

BUS TRANSCEIVERS

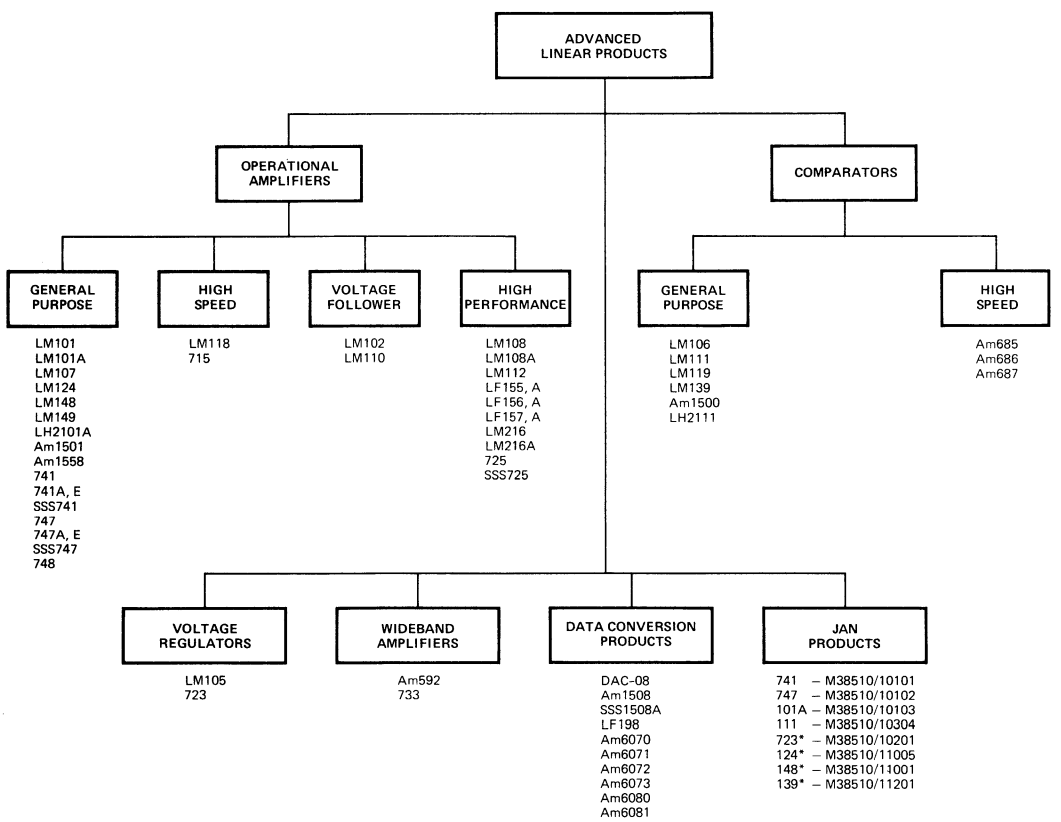
Device	Output	Function	Hysteresis	Speed (Note 1)	Comments
QUAD					
Am26S10	100mA-O.C.	Inverting	No	20ns	SN55/75138 pin out
Am26S11	100mA-O.C.	Non-Inverting to bus; Inverting off bus	No	22ns	Same as Am26S10 except non-inverting to bus
Am26S12	100mA-O.C.	Inverting	Yes-0.6V	32ns	Same pin out as DS78/8838 and 8T38
Am26S12A	100mA-O.C.	Inverting	Yes-1.05V	32ns	Wider threshold Am26S12
Am2905	100mA-O.C.	Inverting	No	31ns (Note 2)	Has 2-input multiplexer
Am2906	100mA-O.C.	Inverting	No	31ns (Note 2)	Has 2-input multiplexer and parity
Am2907	100mA-O.C.	Inverting	No	31ns (Note 2)	Includes parity, 2.0V receiver V_{TH}
Am2908	100mA-O.C.	Inverting	No	31ns (Note 2)	Includes parity, 1.5V receiver V_{TH}
Am2915A	48mA/3-St.	Inverting	No	31ns (Note 2)	Has 2-input multiplexer
Am2916A	48mA/3-St.	Inverting	No	31ns (Note 2)	Has 2-input multiplexer and parity
Am2917A	48mA/3-St.	Inverting	No	31ns (Note 2)	Includes parity
Am3216	50mA/3-St.	Non-Inverting	No	34ns	Same as 8216 except different A.C. loading spec
Am3226	50mA/3-St.	Inverting	No	30ns	Same as 8216 except different A.C. loading spec
Am3448A	48mA/3-St.-O.C.	Non-Inverting	Yes	32ns	IEEE 488 compatible
Am78/8838	50mA-O.C.	Inverting	No	38ns	Same pin out and function as Am26S12A and 8T38
Am8T26A	48mA/3-St.	Inverting	No	19ns	V_{OH} MOS compatible
Am8T28	48mA/3-St.	Non-Inverting	No	25ns	V_{OH} MOS compatible
Am8216	50mA/3-St.	Non-Inverting	No	34ns	Similar to 8T28
Am8226	50mA/3-St.	Non-Inverting	No	30ns	Similar to 8T26A
OCTAL					
Am8303B	48mA/3-St.	Inverting	No	14ns	Same as two 8226's in one 20 pin package
Am8304B	48mA/3-St.	Non-Inverting	No	24ns	Same as two 8216's in one 20 pin package

Notes: 1. Typical delay at 28°C for input to bus plus receiver to output.
2. Bus enable to bus plus bus to receiver output. All parts include register or driver plus receiver with latch.

Linear Circuits

- **Function Selector Guide**
- **Ordering and Package Guide**
- **Jan Cross Reference and Ordering Guide**
- **Competitive Cross Reference**

Advanced Micro Devices offers a broad line of high performance Linear integrated circuits including operational amplifiers, comparators, voltage regulators, wideband amplifiers and D to A conversion circuits. All Advanced Micro Devices Linear circuits are processed to the reliability and quality requirements of MIL-STD-883A and MIL-M-38510.



*In Development

FUNCTION SELECTOR GUIDE

Type	Description	Features	Product
Uncompensated Op Amps	General Purpose	500nA I_B, 5mV Vos	LM101
	General Purpose	500nA I_B, 5mV Vos	LM748
	Improved General Purpose	75nA I_B, 2mV Vos	LM101A
	Dual Improved General Purpose	75nA I_B, 2mV Vos	AM1501
	Dual Improved General Purpose	75nA I_B, 2mV Vos	LH2101A
	Instrumentation	100nA I_B, 1mV Vos, 0.5μV/°C TCVIO	725
	Improved Instrumentation	70nA I_B, 0.1mV Vos, 0.1μV/°C TCVIO	SSS725
	Low Input Current Precision	2nA I_B, 2mV Vos, 0.2nA IOS	LM108
	Low Input Current and Offset Voltage Precision	2nA I_B, 0.5mV Vos, 0.2nA IOS, 5μV/°C TCVIO	LM108A
	High Speed	15V/μsec slew rate, 750nA I_B, 5mV Vos	715
Internally Compensated Op Amps	General Purpose	500nA I_B, 5mV Vos	741
	Improved General Purpose	80nA I_B, 3mV Vos, 30nA I_{OS}, 50μV/V PSRR	741A, E
	High Performance	50nA I_B, 2mV Vos	SSS741
	Dual General Purpose	500nA I_B, 5mV Vos	747
	Dual Improved Generai Purpose	80nA I_B, 3mV Vos, 30nA I_{OS}, 50μV/V PSRR	747A, E
	Dual High Performance	50nA I_B, 2mV Vos	SSS747
	Dual General Purpose	500nA I_B, 5mV Vos	AM1558
	Quad General Purpose	150nA I_B, 5mV Vos, Single or Dual Supply, 3 to 30V, 1mW/op amp at +5V	LM124 LM124A
	Quad 741	500nA I_B, 5mV Vos	LM148
	Quad Decompensated	500nA I_B, 5mV Vos A_V (min.) = 5	LM149
	Improved General Purpose	75nA I_B, 2mV Vos	LM107
	Low Input Current Precision	2nA I_B, 2mV Vos	LM112
	Very Low Input Current Precision	150pA I_B, 10mV Vos	LM216
	Very Low Input Current Precision	50pA I_B, 3mV Vos	LM216A
	High Speed	50V/μsec slew rate, 4mV Vos, 250nA I_B	LM118
	FET Input General Purpose	5mV Vos, 20pA I_{OS}, 100pA I_B	LF155
	FET Input General Purpose	2mV Vos, 5μV/°C TC V_{10}, 10pA I_{OS}, 50pA I_B	LF155A
	FET Input Wide Band	5mV Vos, 20pA I_{OS}, 100pA I_B, 7.5V/μsec SR	LF156
	FET Input Wide Band	2mV Vos, 5μV/°C TC V_{10}, 10pA I_{OS}, 50pA I_B, 10V/μsec SR	LF156A
	FET Input Wideband Decompensated	5mV Vos, 20pA I_{OS}, 100pA I_B, 30V/μsec SR (A_V = 5)	LF157
	Fet Input Wide Band Decompensated	2mV Vos, 5μV/°C TC V_{10}, 10pA I_{OS}, 50pA I_B, 40V/μsec SR (A_V = 5)	LF157A
Voltage Followers	Low Input Current, High Speed	10nA I_B, 5mV Vos, 20V/μsec slew rate, $10^{10}\Omega$ Rin	LM102
	Improved Low Input Current High Speed	3nA I_B, 4mV Vos, 20V/μsec slew rate, $10^{10}\Omega$ Rin	LM110
Voltage Comparators	General Purpose	100nA I_B, 3mV Vos, 250ns Response Time, 50V and 50mA Output	LM111
	Dual General Purpose	100nA I_B, 3mV Vos, 250ns Response Time, 50V and 50mA Output	LH2111
	Dual General Purpose	100nA I_B, 3mV Vos, 250ns Response Time, 50V and 50mA Output	AM1500
	High Speed	20μA I_B, 2mV Vos, 40ns Response Time, 24V and 100mA Output	LM106
	Dual General Purpose	500nA I_B, 4mV Vos, 80ns Response Time, 35V and 25mA Output, +5 or +15V Supply	LM119
	Quad General Purpose	100nA I_B, 2mV Vos, Single or Dual Supply 2 to 36V, 1mW/comp. at +5V	LM139 LM139A
	Very Fast ECL Output	10μA I_B, 2mV Vos, 6.5ns Response Time	AM685
	Very Fast TTL Output	10μA I_B, 2mV Vos, 12ns Response Time	AM686
	Dual Very Fast ECL Output	10μA I_B, 2mV Vos, 6.5ns Response Time	AM687
Voltage Regulators	General Purpose	2-37V Output, 0.15% load reg., 50V input, 150mA Output	723
	General Purpose	4.5-40V Output, 0.05% load reg., 50V input, 12mA Output	LM105
D to A Converter Products	8-Bit Multiplying D-to-A Converter	Accuracy 0.19%, Settling Time 300nsec typ.	AM1508
	8-Bit Multiplying D-to-A Converter	Accuracy 0.1%, Settling Time 135nsec	SSS1508A
	FET Input Sample and Hold	Gain Error .005%, Acquisition Time	DAC-08
		10μsec Z_{IN} 10^{10}Ohm	LF198
	Companding D to A Converters	12 bit Dynamic Range, A-law or μlaw	AM6070/1/2/3
	Bus Compatible D to A Converters	.1% Accuracy, Compatible with any Microprocessor	AM6080/81
Wideband Amplifiers	Differential Input and Output	40-120MHz B.W., 100-400 Voltage Gain	733
	Differential Input and Output	40-120MHz B.W., 100-400 Voltage Gain	AM592

DICE – All Advanced Micro Devices Linear products are available as electrically tested and optically inspected dice for assemblers of hybrid circuits. Dice are processed to MIL-STD-883A level B and packaged in waffle packs. Gold backing is not available.

ADVANCED LINEAR – ORDERING AND PACKAGE GUIDE

DEVICE NUMBER	ORDER NUMBER 0°C to +70°C				ORDER NUMBER −55°C to +125°C			
	Metal Can	Hermetic DIP	Molded DIP	Dice	Metal Can	Hermetic DIP	Flat Pack	Dice
LM101	LM301H	LM301D	LM301N	LD301	LM101H	LM101D	LM101F	LD101
*			LM201N		LM201H	LM201D	LM201F	
LM101A	LM301AH	LM301AD	LM301AN	LD301A	LM101AH	LM101AD	LM101AF	LD101A
*			LM201AN		LM201AH	LM201AD	LM201AF	
LM102	LM302H	LM302D		LD302	LM102H	LM102D	LM102F	LD102
*					LM202H	LM202D	LM202F	
LM105	LM305H			LD305	LM105H			LD105
*	LM305AH				LM205H			
LM106	LM306H	LM306D		LD306	LM106H		LM106F	LD106
*					LM206H		LM206F	
LM107	LM307H	LM307D		LD307	LM107H	LM107D	LM107F	LD107
*					LM207H	LM207D	LM207F	
LM108	LM308H	LM308D	LM308N	LD308	LM108H	LM108D	LM108F	LD108
*					LM208H	LM208D	LM208F	
LM108A	LM308AH	LM308AD	LM308AN	LD308A	LM108AH	LM108AD	LM108AF	LD108A
*					LM208AH	LM208AD	LM208AF	
LM110	LM310H	LM310D	LM310N	LD310	LM110H	LM110D	LM110F	LD110
*					LM210H	LM210D	LM210F	
LM111	LM311H	LM311D	LM311N	LD311	LM111H	LM111D	LM111F	LD111
*					LM211H	LM211D	LM211F	
LM112	LM312H	LM312D		LD312	LM112H	LM112D	LM112F	LD112
*					LM212H	LM212D	LM212F	
LM118	LM318H	LM318D	LM318N	LD318	LM118H	LM118D	LM118F	LD118
*					LM218H	LM218D	LM218F	
LM119	LM319H	LM319D	LM319N	LD319	LM119H	LM119D	LM119F	LD119
*					LM219H	LM219D	LM219F	
LM124		LM324D	LM324N	LD324		LM124D	LM124F	LD124
*						LM224D	LM224F	
LM124A		LM324AD	LM324AN	LD324A		LM124AD	LM124AF	LD124A
*						LM224AD	LM224AF	
LM139		LM339D	LM339N	LD339		LM139D	LM139F	LD139
*						LM239D	LM239F	
LM139A		LM339AD	LM339AN	LD339A		LM139AD	LM139AF	LD139A
*						LM239AD	LM239AF	
LM148		LM348D	LM348N	LD348		LM148D		LD148
*						LM248D		
LM149		LM349D	LM349N	LD349		LM149D		LD149
*						LM249D		
LF155	LF355H		LF355N	LD355	LF155H			LD155
*					LF255H			
LF155A	LF355AH			LD355A	LF155AH			LD155A
*								
LF156	LF356H		LF356N	LD356	LF156H			LD156
*					LF256H			
LF156A	LF356AH			LD356A	LF156AH			LD156A
*								
LF157	LF357H		LF357N	LD357	LF157H			LD157
*					LF257H			
LF157A	LF357AH			LD357A	LF157AH			LD157A
*								
LF198	LF398H			LD398	LF198H			LD198
*					LF298H			
LM216	LM316H	LM316D		LD316	LM216H	LM216D	LM216F	LD216
*								
LM216A	LM316AH	LM316AD		LD316A	LM216AH	LM216AD	LM216AF	LD216A
*								
AM592	AM592HC	AM592DC	AM592PC	AM592XC	AM592HM	AM592DM		AM592XM
AM685*	AM685HL	AM685DL		AM685XL	AM685HM	AM685DM		AM685XM
AM686	AM686HC	AM686DC		AM686XC	AM686HM	AM686DM		AM686XM
AM687*		AM687DL		AM687XL		AM687DM		AM687XM
715	715HC	715DC		715XC	715HM	715DM		715XM
723	723HC	723DC	723PC	723XC	723HM	723DM		723XM
725	725HC	725DC	725CN	725XC	725HM	725DM		725XM
SSS725	SSS725CJ	SSS725CP			SSS725J	SSS725P		
733	733HC	733DC		733XC	733HM	733DM	733FM	733XM
741	741HC	741DC		741XC	741HM	741DM	741FM	741XM
741A	741EHC	741EDC			741AHM	741ADM	741AFM	
SSS741	SSS741CJ				SSS741J			
747	747HC	747DC	747PC	747XC	747HM	747DM	747FM	747XM
747A	747EHC	747EDC			747AHM	747ADM	747AFM	
SSS747	SSS747CK	SSS747CP			SSS747K	SSS747P	SSS747M	
748	748HC	748DC	748PC	748XC	748HM	748DM	748FM	748XM
AM1500		AM1500DC				AM1500DM	AM1500FM	
*						AM1500DL	AM1500FL	
AM1501		AM1501DC				AM1501DM	AM1501FM	
*						AM1501DL	AM1501FL	
AM1508		AM1408L8				AM1508L8		
		AM1408L7						
		AM1408L6						
AM1558	AM1458H				AM1558H			
LH2101A		LH2301AD				LH2101AD	LH2101AF	
*						LH2201AD	LH2201AF	
LH2111		LH2311D				LH2111D	LH2111F	
*		AMDAC-08EQ				LH2211D	LH2211F	
DAC-08		AMDAC-08CQ				AMDAC-08AQ		
AM6070/1/2/3		AM6070DC	AM6070PC	6070XC		AMDAC-08Q		
						AM6070DM		

*Indicates −25°C to +85°C Operating Temperature Range.

For MIL-STD-883A Class B processing order as follows: For all LM100 and LM2100 series devices add/883B suffix.
Example: LM101AH/883B, LH2111D/883B

For other devices add B suffix.
Example: 741HMB, AM687DMB, AM1500DMB

ADVANCED LINEAR PROCESSING

Every AMD Linear integrated circuit is manufactured to the full requirements of MIL-STD-883A level C or better. AMD has been rigorously inspected by NASA and DESC and has received full line certification by both to supply high reliability Linear circuits on NASA and JAN programs.

During a period when the industry is continually looking for ways to decrease cost through production efficiency as well as process simplification, AMD has maintained the highest integrity and in many instances developed more sophisticated and costly processes to enhance device performance and reliability. The following special processing is representative of the importance AMD places on maintaining product reliability.

AMD Wafer Processing

- Controlled oxide step profile for superior metal coverage.
- Wafer lots regularly SEM inspected on in-house SEM.
- Proprietary passivation process prevents MOS channeling and inherently provides extra radiation hardness.

AMD Electrical Testing

- All devices, in all packages, 100% tested at room, high and low temperatures.
- All devices tested for AC parameters.
- All internally compensated devices undergo capacitor stress testing to eliminate marginal units.
- When required by application many devices are tested at 150°C to simulate die temperatures reached under continuous operation.

AMD–JAN LINEAR PRODUCT GUIDE

The following Linear devices are available as fully qualified JM38510 parts:

Device Type	Slash Sheet Number
741	JM38510/10101BGC
	JM38510/10101BGA
747	JM38510/10102BCA
	JM38510/10102BCB
	JM38510/10102BIC*
101A	JM38510/10103BGC
	JM38510/10103BGA
111	JM38510/10304BGC
723	JM38510/10201*
139	JM38510/11201*
124	JM38510/11005*
148	JM38510/11001*

* Qualification in progress.

THE FUTURE – LINEAR LSI

Linear processing is advancing dramatically and AMD is at the forefront of this technology expansion with the processes already developed for the next generation linear circuits. The standard high voltage process has been advanced in two directions, both employing ion implantation as a key and incorporating FET's together with bipolar devices monolithically. One process is being used to build a series of operational amplifiers using J-FET input transistors; the other is an advanced MOSFET compatible bipolar process which will be used in a new generation of data and speech communications circuits.

Three years ago the analog group at AMD developed the Am685, 686 and 687 that were billed as the world's fastest ECL, TTL and DUAL ECL comparators. Their claim has been unchallenged by anyone. The process that was developed for these products employed thin epitaxial layers, shallow junctions and advanced barrier layer metallization and allowed the integration of 1GHz transistors and fast Schottky diode clamps.

Poised now for entry into the area of high-speed data acquisition and communication this process is being upgraded by a quantum jump to enable the fabrication of a family of building blocks to be introduced in the near future, comprising a D/A converter sample-and-hold and difference amplifiers and a high-speed quantizer, which form the heart of an A/D converter system. The quantizer can also be used to make a full parallel 8-bit A/D converter capable of operating at 800 megabits/sec. Developments that make this possible are new thin film resistor materials and special photolithography techniques that permit the fabrication of monolithic devices with substantially reduced capacitances and operating frequencies of 2GHz. Interconnection will employ multilayer metallization with its attendant increase on component density. The quantizer can be dubbed an entry into LINEAR LSI.

LINEAR CROSS REFERENCE GUIDE

Fairchild	AMD
MC1458G	AM1458H
MC1558G	AM1558H
LM101D	LM101D
LM101H	LM101H
LM101AD	LM101AD
LM101AF	LM101AF
LM101AH	LM101AH
LM102H	LM102H
LM105H	LM105H
LM107H	LM107H
LM108AH	LM108AH
LM108H	LM108H
LM110H	LM110H
LM111H	LM111H
LM139D	LM139D
LM201D	LM201D
LM201H	LM301H
LM201AD	LM201AD
LM201AF	LM201AF
LM201AH	LM201AH
LM207H	LM207H
LM208H	LM208H
LM208AH	LM208AH
LM301AD	LM301AD
LM301AH	LM301AH
LM301AN	LM301AN
LM302H	LM302H
LM305H	LM305H
LM305AH	LM305AH
LM307H	LM307H
LM308H	LM308H
LM308AH	LM308AH
LM310H	LM310H
LM311H	LM311H
LM311N	LM311N
LM339D	LM339D
LM339N	LM339N
715DC	715DC
715DM	715DM
715HC	715HC
715HM	715HM
723DC	723DC
723DM	723DM
723HC	723HC
723HM	723HM
725HC	725HC
725HM	725HM
725PC	725CN
733DC	733DC
733DM	733DM
733FM	733FM
733HC	733HC
733HM	733HM
741DC	741DC
741DM	741DM
741FM	741FM
741HC	741HC
741HM	741HM
741ADM	741ADM
741AFM	741AFM
741AHM	741AHM
741EDC	741EDC
741EHC	741EHC
747DC	747DC
747DM	747DM
747HC	747HC
747HM	747HM
747PC	747PC
747ADM	747ADM
747AHM	747AHM
747EDC	747EDC
747EHC	747EHC
748DC	748DC
748DM	748DM

Fairchild	AMD
748FM	748FM
748HC	748HC
748HM	748HM
748PC	748PC
760DC	AM686DC**
760DM	AM686DM**
760HC	AM686HC**
760HM	AM686HM**
775DM	LM139D
775DC	LM339D
775PC	LM339N

National	AMD
LF111D, J	LF111D
LF111F	LF111F
LF111H	LF111H
LF155H	LF155H
LF155AH	LF155AH
LF156H	LF156H
LF156AH	LF156AH
LF157H	LF157H
LF157AH	LF157AH
LF198H	LF198H
LF211D, J	LF211D
LF211F	LF211F
LF211H	LF211H
LF255H	LF255H
LF256H	LF256H
LF257H	LF257H
LF298H	LF298H
LF311D	LF311D
LF311H	LF311H
LF355H	LF355H
LF355N	LF355N
LF355AH	LF355AH
LF356H	LF356H
LF356N	LF356N
LF356AH	LF356AH
LF357H	LF357H
LF357N	LF357N
LF357AH	LF357AH
LF398H	LF398H
LH2101AD,J	LH2101AD
LH2101AF	LH2101AF
LH2111D,J	LH2111D
LH2111F	LH2111F
LH2201AD,J	LH2201AD
LH2201AF	LH2201AF
LH2211D,J	LH2211D
LH2211F	LH2211F
LH2301AD,J	LH2301AD
LH2311D,J	LH2311D
LM101D,J	LM101D
LM101F	LM101F
LM101H	LM101H
LM101AD,J	LM101AD
LM101AF	LM101AF
LM101AH	LM101AH
LM102D,J	LM102D
LM102F	LM102F
LM102H	LM102H
LM105F	LM105F
LM105H	LM105H
LM106F	LM106F
LM106H	LM106H
LM107D,J	LM107D
LM107F	LM107F
LM107H	LM107H
LM108D,J	LM108D
LM108F	LM108F
LM108H	LM108H
LM108AD,J	LM108AD

**Improved functional equivalent

National	AMD
LM108AF	LM108AF
LM108AH	LM108AH
LM110D,J	LM110D
LM110F	LM110F
LM110H	LM110H
LM111D,J	LM111D
LM111F	LM111F
LM111H	LM111H
LM112D,J	LM112D
LM112F	LM112F
LM112H	LM112H
LM118D,J	LM118D
LM118F	LM118F
LM118H	LM118H
LM119D,J	LM119D
LM119F	LM119F
LM119H	LM119H
LM124D,J	LM124D
LM124F	LM124F
LM139D,J	LM139D
LM139AD,J	LM139AD
LM139F	LM139F
LM139AF	LM139AF
LM148D	LM148D
LM149D	LM149D
LM201H	LM301H
LM201AD,J	LM201AD
LM201AF	LM201AF
LM201AH	LM201AH
LM202H	LM202H
LM205H	LM205H
LM206H	LM206H
LM207D,J	LM207D
LM207F	LM207F
LM207H	LM207H
LM208AD,J	LM208AD
LM208AF	LM208AF
LM208AH	LM208AH
LM208D,J	LM208D
LM208F	LM208F
LM208H	LM208H
LM210D,J	LM210D
LM210H	LM210H
LM211D,J	LM211D
LM211F	LM211F
LM211H	LM211H
LM212D,J	LM212D
LM212F	LM212F
LM212H	LM212H
LM216AD,J	LM216AD
LM216AF	LM216AF
LM216AH	LM216AH
LM216D,J	LM216D
LM216F	LM216F
LM216H	LM216H
LM218D,J	LM218D
LM218F	LM218F
LM218H	LM218H
LM219D,J	LM219D
LM219F	LM219F
LM219H	LM219H
LM224D,J	LM224D
LM239D,J	LM239D
LM239AD,J	LM239D
LM248D	LM248D
LM249D	LM249D
LM301AD,J	LM301AD
LM301AF	LM301AF
LM301AH	LM301AH
LM301AN	LM301AN
LM302F	LM302F
LM302H	LM302H
LM305F	LM305F
LM305H	LM305H

National	AMD
LM305AH	LM305AH
LM306F	LM306F
LM306H	LM306H
LM307D,J	LM307D
LM307F	LM307F
LM307H	LM307H
LM308AD,J	LM308AD
LM308AF	LM308AF
LM308AH	LM308AH
LM308AN	LM308AN
LM308D,J	LM308D
LM308F	LM308F
LM308H	LM308H
LM308N	LM308N
LM310D,J	LM310D
LM310F	LM310F
LM310H	LM310H
LM310N	LM310N
LM311D,J	LM311D
LM311F	LM311F
LM311N	LM311N
LM312D,J	LM312D
LM312F	LM312F
LM312H	LM312H
LM316AD,J	LM316AD
LM316AF	LM316AF
LM316AH	LM316AH
LM316D,J	LM316D
LM316F	LM316F
LM316H	LM316H
LM318D,J	LM318D
LM318F	LM318F
LM318H	LM318H
LM318N	LM318N
LM319H	LM319H
LM319D,J	LM319D
LM319N	LM319N
LM324D,J	LM324D
LM324N	LM324N
LM339D,J	LM339D
LM339AD,J	LM339AD
LM339N	LM339N
LM339AN	LM339AN
LM348D	LM348D
LM348N	LM348N
LM349D	LM349D
LM349N	LM349N
LM723D,J	723DM
LM723H	723HM
LM723CD,J	723DC
LM723CH	723HC
LM725H	725HM
LM725CH	725HC
LM725CN	725CN
LM725D,J	725DM
LM725CD,J	725DC
LM733D,J	733DM
LM733H	733HM
LM733CD,J	733DC
LM733CH	733HC
LM741D,J	741DM
LM741F	741FM
LM741H	741HM
LM741CD,J	741DC
LM741CF	741FC
LM741CH	741HC
LM747D,J	747DM
LM747H	747HM
LM747F	747FM
LM747CD,J	747DC
LM747CP	747PC
LM747CH	747HC
LM 747CN	747PC
LM748H	748HM

LINEAR CROSS REFERENCE GUIDE (Cont.)

National	AMD
LM748CH	748HC
LM748CN	748PC
LM1458H	AM1458H
LM1558H	AM1558H

Motorola	AMD
MC1408L6	AM1408L6
MC1408L7	AM1408L7
MC1408L8	AM1408L8
MC1508L8	AM1508L8
MC1458G	AM1458H
MC1558G	AM1558H
MC1723CG	723HC
MC1723CL	723DC
MC1723G	723HM
MC1723L	723DM
MC1733CG	733HC
MC1733CL	733DC
MC1733F	733FM
MC1733G	733HM
MC1733L	733DM
MC1741CG	741HC
MC1741CL	741DC
MC1741F	741FM
MC1741G	741HM
MC1741L	741DM
MC1747CG	747HC
MC1747CL	747DC
MC1747G	747HM
MC1747L	747DM
MC1748CG	748HC
MC1748G	748HM
MLM101AG	LM101AH
MLM105G	LM105H
MLM107G	LM107H
MLM110G	LM110H
MLM111F	LM111F
MLM111G	LM111H
MLM111L	LM111D
MLM201AG	LM201AH
MLM205G	LM205H
MLM207G	LM207H
MLM210G	LM210H
MLM211G	LM211H
MLM211L	LM211D
MLM301AG	LM301AH
MLM301API	LM301AN
MLM305G	LM305H
MLM307G	LM307H
MLM310G	LM310H
MLM311G	LM311H
MLM211PI	LM311N
MLM311L	LM311D

Texas Inst.	AMD
SN52101AJ	LM101AD
SN52101AL	LM101AH
SN52101AZ	LM101AF
SN52105L	LM105H
SN52106FA	LM106F
SN52106L	LM106H
SN52107J	LM107D
SN52107L	LM107H
SN52107Z	LM107F
SN52108AFA	LM108AF
SN52108AJA	LM108AD
SN52108AL	LM108AH
SN52108FA	LM108F
SN52108JA	LM108D
SN52108L	LM108H
SN52111FA	LM111F
SN52111J	LM111D
SN52111L	LM111H
SN52118FA	LM118F
SN52118JA	LM118D
SN52118L	LM118H
SN52723J	723DM
SN52723L	723HM
SN52733FA	733FM
SN52733J	733DM
SN52733L	733HM
SN52741FA	741FM
SN52741JA	741DM
SN52741L	741HM
SN52747FA	747FM
SN52747JA	747DM
SN52747L	747HM
SN52748FA	748FM
SN52748JA	748DM
SN52748L	748HM
SN72301AJ	LM301AD
SN72301AL	LM301AH
SN72305L	LM305H
SN72306L	LM306H
SN72307J	LM307D
SN72307L	LM307H
SN73208AJA	LM308AD
SN72308AL	LM308AH
SN72308JA	LM308D
SN72308L	LM308H
SN72311J	LM311D
SN72311L	LM311H
SN72318JA	LM318D
SN72318L	LM318H
SN72723J	723DC
SN72723L	723HC
SN72733J	733DC
SN72733L	733HC
SN72741JA	741DC
SN72741L	741HC
SN72747JA	747DC
SN72747L	747HC
SN72748JA	748DC
SN72748L	748HC

Signetics	AMD
NE529K	AM686HC**
SE529K	AM686HM**
SE592K	AM592HM
NE592K	AM592HC
SE592A	AM592PC
LM101F	LM101D
LM101T	LM101H
LM101AF	LM101AD
LM101AT	LM101AH
LM107F	LM107D
LM107T	LM107H
LM108F	LM108D
LM108T	LM108H
LM108AF	LM108AD
LM108AT	LM108AH
LM111F	LM111D
LM111T	LM111H
LM119H	LM119H
LM119D	LM119D
LM124F	LM124D
LM139F	LM139D

**Improved functional equivalent

Signetics	AMD
LM201T	LM301H
LM201AF	LM201AD
LM201AT	LM201AH
LM201AV	LM201AN
LM207F	LM207D
LM207T	LM207H
LM208F	LM208D
LM208T	LM208H
LM208AF	LM208AD
LM208AT	LM208AH
LM211F	LM211D
LM211T	LM211H
LM219H	LM219H
LM219D	LM219D
LM224F	LM224D
LM239F	LM239D
LM301AT	LM301AH
LM301AV	LM301AN
LM307F	LM307D
LM307T	LM307H
LM308F	LM308D
LM308T	LM308H
LM308V	LM308N
LM308AF	LM308AD
LM308AT	LM308AH
LM311F	LM311D
LM311T	LM311H
LM311V	LM311N
LM319H	LM319H
LM319D	LM319D
LM319A	LM319N
LM324A	LM324N
LM324F	LM324D
LM339A	LM339N
LM339F	LM339D
UA723CF	723DC
UA723CL	723HC
UA723F	723DM
UA723L	723HM
UA733CA	733PC
UA733CF	733DC
UA733CK	733HC
UA733F	733DM
UA733K	733HM
UA741CF	741DC
UA741CT	741HC
UA741F	741DM
UA741T	741HM
UA747CA	747PC
UA747CF	747DC
UA747CK	747HC
UA747F	747DM
UA747K	747HM
UA748CT	748HC
UA748F	748DM
UA748T	748HM

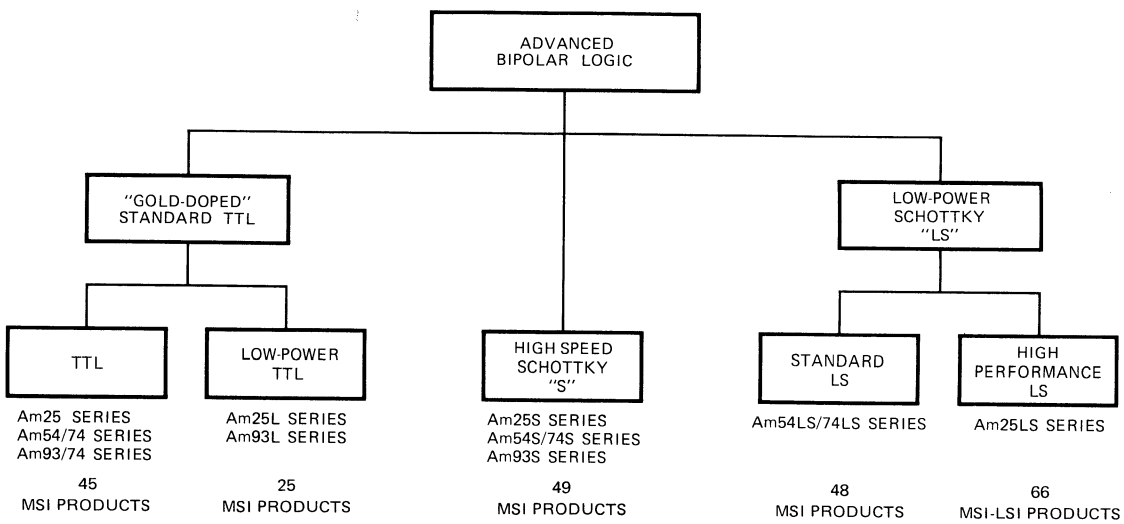
Raytheon	AMD
LM101D	LM101D
LM101F	LM101F
LM101H	LM101H
LM101AD	LM101AD
LM101AF	LM101AF
LM101AH	LM101AH
LM105F	LM105F
LM105H	LM105H
LM106H	LM106H
LM107D	LM107D
LM107F	LM107F
LM107H	LM107H
LM108D	LM108D
LM108F	LM108F
LM108H	LM108H
LM108AD	LM108AD
LM108AF	LM108AF
LM108AH	LM108AH
LM111D	LM111D
LM111F	LM111F
LM111H	LM111H
LM112D	LM112D
LM112F	LM112F
LM112H	LM112H
LM118H	LM118H
LM216D	LM216D
LM216H	LM216H
LM216AD	LM216AD
LM216AH	LM216AH
LM301AD	LM301AD
LM301AH	LM301AH
LM301AN	LM301AN
LM305H	LM305H
LM305AH	LM305AH
LM306H	LM306H
LM307D	LM307D
LM307H	LM307H
LM308D	LM308D
LM308H	LM308H
LM308AD	LM308AD
LM308AH	LM308AH
LM311D	LM311D
LM311H	LM311H
LM311N	LM311N
LM312D	LM312D
LM312H	LM312H
LM316D	LM316D
LM316H	LM316H
LM316AD	LM316AD
LM316AH	LM316AH
LM318H	LM318H
RM723D	723DM
RC723D	723DC
RM723T	723HM
RC723T	723HC
RM725T	725HM
RC725T	725HC
RM733D	733DM
RC733D	733DC
RM733Q	733FM
RC733Q	733FC
RM733T	733HM
RC733T	733HC
RC733DP	733PC
RM741D	741DM
RC741D	741DC
RM741Q	741FM
RC741Q	741FC
RM741T	741HM
RC741T	741HC
RM474D	747DM
RC747D	747DC
RM747T	747HM
RC747T	747HC
RC747DP	747PC
RM748T	748HM
RC748T	748HC

Bipolar Logic Circuits

- **Schottky MSI**
- **Low-Power Schottky MSI-LSI**
- **Standard TTL/MSI**
- **Low-Power TTL/MSI**

Advanced Micro Devices offers a broad line of complex TTL/MSI and LSI bipolar logic integrated circuits. Four basic process technologies are employed to meet the various speed, power and cost combinations required by manufacturers of high performance digital systems. The table below compares the relative speed-power performance of each of the families.

The Advanced Bipolar Logic line consists of both proprietary and industry standard devices fabricated with Schottky, Low Power Schottky and conventional "gold-doped" processes. All Advanced Micro Devices' circuits are processed to the reliability and quality requirements of MIL-STD-883.



Family		Ave. Gate Propagation Delay	Ave. Power Per Gate	Typ. Register Clock Freq.
High-Speed Schottky	Am25S Am54S/74S Am93S	3ns	20mW	110MHz
Low-Power Schottky	Am25LS Am54LS/74LS	5ns 10ns	2mW 2mW	65MHz 40MHz
Standard TTL	Am25 Am54/74 Am93	10ns	10mW	40MHz
Low-Power Standard TTL	Am25L Am93L	25ns	2.5mW	15MHz

Am25LS HIGH PERFORMANCE LS	Am54/74LS STANDARD LS	DESCRIPTION	PACKAGE PINS
25LS07	54/74LS378	Six-Bit Register; Common Enable	16
25LS08	54/74LS379	Four-Bit Register; Common Enable	16
25LS09	54/74LS399	Four-Bit Register; Multiplexed Inputs	16
25LS14	(54/74LS384)	Eight-Bit Serial/Parallel Two's Complement Multiplier	16
25LS15	(54/74LS385)	Four-Bit Serial/Parallel Adder Subtractor	20
25LS22	(54/74LS322)	Eight-Bit Serial/Parallel Register; Sign Extend	20
25LS23	(54/74LS323)	Eight-Bit Universal Shift Register; Synchronous Clear	16
25LS138	54/74LS138	One-of-Eight Decoder/Demultiplexer	16
25LS139	54/74LS139	Dual One-of-Four Decoder/Demultiplexer	16
25LS148	54/74LS148	Priority Encoder; Eight-Line to Three-Line	16
25LS151	54/74LS151	Eight-Input Multiplexer	16
25LS153	54/74LS153	Dual Four-Input Multiplexer	16
25LS157	54/74LS157	Quad Two-Input Multiplexer; Non-Inverting	16
25LS158	54/74LS158	Quad Two-Input Multiplexer; Inverting	16
25LS160A	54/74LS160A	Synchronous BCD Decade Counter; Asynchronous Clear	16
25LS161A	54/74LS161A	Synchronous Four-Bit Binary Counter; Asynchronous Clear	16
25LS162A	54/74LS162A	Synchronous BCD Decade Counter; Synchronous Clear	16
25LS163A	54/74LS163A	Synchronous Four-Bit Binary Counter; Synchronous Clear	16
25LS164	54/74LS164	Eight-Bit Serial-In, Parallel-Out Shift Register	14
25LS168A	54/74LS168A	Synchronous BCD Decade Up-Down Counter; Programmable	16
25LS169A	54/74LS169A	Synchronous Four-Bit Binary Up-Down Counter; Programmable	16
25LS174	54/74LS174	Six-Bit Register; Common Clear	16
25LS175	54/74LS175	Quad Register; Common Clear	16
25LS181	54/74LS181	Four-Bit ALU/Function Generator	24
25LS190	54/74LS190	BCD Decade Up-Down Counter; Down-Up Mode Control	16
25LS191	54/74LS191	Four-Bit Binary Up-Down Counter; Down-Up Mode Control	16
25LS192	54/74LS192	BCD Decade Up-Down Counter; Dual Clocks	16
25LS193	54/74LS193	Four-Bit Binary Up-Down Counter; Dual Clocks	16
25LS194A	54/74LS194A	Four-Bit Register; Shift Right, Left or Parallel Load	16
25LS195A	54/74LS195A	Four-Bit Register; Shift Right or Parallel Load	16
25LS240†	54/74LS240	Octal Bus Driver; Inverting, Three-State Outputs	20
25LS241†	54/74LS241	Octal Bus Driver; Non-Inverting, Three-State Outputs (G, $\overline{G}$ inputs)	20
25LS242†	54/74LS242	Quad Bus Transceiver; Inverting	14
25LS243†	54/74LS243	Quad Bus Transceiver; Non-Inverting	14
25LS244†	54/74LS244	Octal Bus Driver; Non-Inverting, Three-State Outputs	20
25LS251	54/74LS251	Eight-Input Multiplexer; Three-State Outputs	16
25LS253	54/74LS253	Dual Four-Input Multiplexer; Three-State Outputs	16
25LS257	54/74LS257	Quad Two-Input Multiplexer; Non-Inverting, Three-State Outputs	16
25LS258	54/74LS258	Quad Two-Input Multiplexer; Inverting, Three-State Outputs	16
25LS273	54/74LS273	Octal D-Register; Common Clear	20
*25LS281	*54/74LS281	Four-Bit Parallel Accumulator	24
25LS299	54/74LS299	Eight-Bit Universal Shift Register, Asynchronous Clear	20
–	(54/74LS322)	See Am25LS22	20
–	(54/74LS323)	See Am25LS23	20
25LS373	54/74LS373	Octal Transparent Latch; Three-State Outputs	20
25LS374	54/74LS374	Octal D-Register; Three-State Outputs	20
25LS377	54/74LS377	Octal D-Register; Common Enable	20
25LS378	54/74LS378	Six-Bit Register, Common Enable (25LS07)	16
25LS379	54/74LS379	Four-Bit Register, Common Enable (25LS08)	16
25LS381	54/74LS381	Four-Bit ALU/Function Generator(20 pin 25LS181)	20
–	(54/74LS382)	See Am25LS2517	20
–	(54/74LS384)	See Am25LS14	16
–	(54/74LS385)	See Am25LS15	20
–	(54/74LS388)	See Am25LS2518	16
25LS399	54/74LS399	Four-Bit Register, Multiplexed Inputs (25LS09)	16
–	54/74LS424	See Am8224 (Am9080A/8080A Clock Generator)	16
25LS533	54/74LS533	Inverting version LS373	20
*25LS534	54/74LS534	Inverting version LS374	20
–	(54/74LS568)	See Am25LS2568	20
–	(54/74LS569)	See Am25LS2569	20
–	54/74LS668	Synchronous BCD Decade Up-Down Counter; Programmable	16
–	54/74LS669	Synchronous Four-Bit Binary Up-Down Counter; Programmable	16

†The Am25LS240-244 are 48mA sink versions of the 54-74LS240-244.
Part numbers shown in parentheses are pin-for-pin equivalent devices with electrical specification differences. Order 25LS part numbers only.

LOW-POWER SCHOTTKY MSI-LSI LOGIC
25LS • 54/74LS SERIES

Am25LS HIGH PERFORMANCE LS	Am54/74LS STANDARD LS	DESCRIPTION	PACKAGE PINS
25LS2513	–	Priority Encoder; Three-State Ouptuts, Eight-Line to Three-Line	20
25LS2516	–	Eight-Bit by Eight-Bit Serial Parallel Multiplier/Accumulator	40
25LS2517	(54/74LS382)	Four-Bit ALU/Function Generator; Overflow Detection	20
25LS2518	(54/74LS388)	Quad Register with Standard and Three-State Outputs	16
25LS2519	–	Quad Register with Dual Three-State Outputs	20
25LS2520	–	Octal D-Register; Common Clear and Enable, Three-State Outputs	22
25LS2521	–	Eight-Bit Comparator	20
*25LS2525	–	System Timing Element	20
25LS2535	–	Eight-Bit Multiplexer; Control Storage	20
25LS2536	–	Eight-Bit Decoder; Control Storage	20
25LS2537	–	One-of-Ten Decoder; Three-State Outputs	20
25LS2538	–	One-of-Eight Decoder; Three-State Outputs	20
25LS2539	–	Dual One-of-Four Decoder; Three-State Outputs	20
25LS2568	(54/74LS568)	BCD Decade Up-Down Counter; Three-State Outputs	20
25LS2569	(54/74LS569)	Four-Bit Binary Up-Down Counter; Three-State Outputs	20

HIGH-SPEED SCHOTTKY MSI LOGIC
25S SERIES

25S05	Four by Two, Two's Complement Multiplier	24
25S07	Six-Bit Register; Clock Enable	16
25S08	Four-Bit Register; Clock Enable	16
25S09	Four-Bit Register; Two-Input Multiplexer on Inputs	16
25S10	Four-Bit, Four-Way Shifter	16
25S18	Quad Register; Standard and Three-State Outputs	16
*25S373	32mA Sink Version 54/74S373 (MMI 57/67S373)	20
*25S374	32mA Sink Version 54/74S374 (MMI 57/67S374)	20
*25S533	32mA Sink Version 54/74S533 (MMI 57/67S382)	20
*25S534	32mA Sink Version 54/74S534 (MMI 57/67S378)	20

54/74S • 82S • 93S SERIES

–	82S62	Nine-Input Parity Checker Generator	14
54S/74S138	–	One-of-Eight Decoder/Demultiplexer	16
54S/74S139	93S21	Dual One-of-Four Decoder/Demultiplexer	16
54S/74S151	–	Eight-Input Multiplexer	16
54S/74S153	–	Dual Four-Input Multiplexer	16
54S/74S157	93S22	Quad Two-Input Multiplexer; Non-Inverting	16
54S/74S158	–	Quad Two-Input Multiplexer; Inverting	16
54S/74S160	93S10	Synchronous BCD Decade Counter, Asynchronous Clear	16
54S/74S161	93S16	Synchronous Four-Bit Binary Counter, Asynchronous Clear	16
54S/74S174	–	Six-Bit Register with Clear	16
54S/74S175	–	Quad Register with Clear	16
54S/74S181	(93S41)	Four-Bit ALU/Function Generator	24
54S/74S182	(93S42)	Look-Ahead Carry Generator	16
54S/74S194	–	Four-Bit Register; Shift Right, Left or Parallel Load	16
54S/74S195	(93S00)	Four-Bit Register; Shift Right or Parallel Load	16
54S/74S251	–	Three-State Eight-Input Multiplexer	16
54S/74S253	–	Three-State Dual Four-Input Multiplexer	16
54S/74S257	–	Three-State Quad Two-Input Multiplexer; Non-Inverting	16
54S/74S258	–	Three-State Quad Two-Input Multiplexer; Inverting	16
54S/74S240	–	Octal Bus Driver; Inverting, Three-State Outputs	20
54S/74S241	–	Octal Bus Driver; Non-Inverting, Three-State Outputs (G, G inputs)	20
*54S/74S242	–	Quad Bus Transceiver; Inverting	14
*54S/74S243	–	Quad Bus Transceiver; Non-Inverting	14
54S/74S244	–	Octal Bus Driver; Non-Inverting, Three-State Outputs	20
54S/74S350	–	Four-Bit Four-Way Shifter	16
*54S/74S373	–	Octal Transparent Latch	20
*54S/74S374	–	Octal D-Type Register; Three-State Outputs	20
54S/74S378	–	Six-Bit Register; Common Enable	16
54S/74S379	–	Four-Bit Register; Common Enable	16
54S/74S388	–	Quad Register; Standard and Three-State Outputs	16
54S/74S399	–	Four-Bit Register; Multiplexed Inputs	16
54S/74S412	–	See Am8212 (Am9080A/8080A Eight-Bit I/O Port)	24
*54S/74S533	–	Inverting Version S373 (MMI 57/67S380)	20
*54S/74S534	–	Inverting Version S374 (MMI 57/67S376)	20
–	93S48	Twelve-Input Parity Generator/Checker	16

*In development. Check with AMD sales office for availability.

ADVANCED MICRO DEVICES
SCHOTTKY AND LOW-POWER SCHOTTKY MSI
FUNCTIONAL SELECTOR GUIDE

Advanced Micro Devices offers a complete line of Schottky and Low-Power Schottky MSI products. On the following pages are a selector guide for these products and brief data on several of the most useful parts. For complete data refer to our Schottky and Low-Power Schottky Data Book.

DESCRIPTION	HIGH-PERFORMANCE LOW-POWER SCHOTTKY	STANDARD LOW-POWER SCHOTTKY	HIGH-SPEED SCHOTTKY
REGISTERS			
Four-Bit Register with Common Clock Enable	*25LS08	54/74LS379	*25S08/54/74S379
Four-Bit Register with Two-Input Multiplexers on Inputs	*25LS09	54/74LS399	*25S09/54/74S399
Four-Bit Register with Standard and Three-State Outputs	†25LS2518/29LS18		†25S18/54/74S388/2918
Four-Bit, Two-Output Three-State Register	†25LS2519/2919		
Four-Bit Register with Common Clear	25LS175	54/74LS175	54/74S175
Four-Bit Register; Shift Right, Left or Parallel Load	25LS194A	54/74LS194A	54/74S194
Four-Bit Register; Shift Right or Parallel Load	25LS195A	54/74LS195A	54/74S195
Six-Bit Register with Common Clock Enable	*25LS07	54/74LS378	*25S07/54/74S378
Six-Bit Register with Common Clear	25LS174	54/74LS174	54/74S174
Eight-Bit, Serial-In, Parallel-Out Register	25LS164	54/74LS164	
Eight-Bit Shift/Storage Register; Synchronous Clear	*25LS23		
Eight-Bit Shift/Storage Register; Asynchronous Clear	25LS299	54/74LS299	
Eight-Bit Shift/Storage Register with Sign Extend	25LS22		
Octal D-Type Register, Common Clear	*25LS273	*54/74LS273	
Octal D-Type Register, Common Clear, Buffered Outputs	*25LS273B		
Octal Transparent Latch (Three-State)	*25LS373	*54/74LS373	*54/74S373
Octal Transparent Latch, Inverting (Three-State)	*25LS533	*54/74LS533	*54/74S533
Octal D-Type Register (Three-State)	*25LS374	*54/74LS374	*54/74S374
Octal D-Type Register, Inverting (Three-State)	*25LS534	*54/74LS534	*54/74S534
Octal D-Type Register, Common Enable	*25LS377	*54/74LS377	
Octal D-Type Register, Common Enable, Buffered Outputs	*25LS377B		
Octal D-Type Register, Common Enable and Clear, Three-State	†25LS2520/2920		
DECADE (BCD) COUNTERS			
Asynchronous Clear	25LS160	54/74LS160	54/74S160/93S10
Synchronous Clear	25LS162	54/74LS162	
Up-Down, Synchronous Preset	25LS168	54/74LS168	
Up-Down, Asynchronous Preset, Single Clock	25LS190	54/74LS190	
Up-Down, Asynchronous Preset, Dual Clock	25LS192	54/74LS192	
Up-Down, Synchronous Preset, Three-State	*25LS2568		
BINARY HEXADECIMAL COUNTERS			
Asynchronous Clear	25LS161	54/74LS161	54/74S161/93S16
Synchronous Clear	25LS163	54/74LS163	
Up-Down, Synchronous Preset	25LS169	54/74LS169	
Up-Down, Asynchronous Preset, Single Clock	25LS191	54/74LS191	
Up-Down, Asynchronous Preset, Dual Clock	25LS193	54/74LS193	
Up-Down, Synchronous Preset, Three-State	*25LS2569		
QUAD BUS TRANSCEIVERS/DRIVERS			
Quad Bus Transceiver, Inverting (100mA)			*26S10
Quad Bus Transceiver, Non-Inverting (100mA)			*26S11
Quad Bus Transceiver, Inverting	*25LS242	*54/74LS242	*54/74S242
Quad Bus Transceiver, Non-Inverting	*25LS243	*54/74LS243	*54/74S243
Quad Open-Collector Bus Transceiver			*26S12/12A
Quad Three-State Bus Transceiver (Inverting)			*8T26/8T26A
Quad Three-State Bus Transceiver (Non-Inverting)			*8T28
Quad Three-State Bus Transceiver with Receiver Latch (Inverting)	†2927		
Quad Three-State Bus Transceiver with Receiver Register	†2928		
Quad Two I/P Transceiver with Three-State Receiver (O.C.)	†2905		
Quad Two I/P Transceiver with Parity (O.C.)	†2906		
Quad Two I/P Transceiver with Parity (O.C.)	†2907		
Quad Two I/P Transceiver with Parity (O.C. and DEC Q/LSI-II Bus Compatible)	†2908		
Quad Two I/P Transceiver with Three-State Receiver (Three-State)	†2915A		
Quad Two I/P Transceiver with Parity (Three-State)	†2916A		
Quad Two I/P Transceiver with Parity (Three-State)	†2917A		
Quad IEEE-488 Bidirectional Bus Transceiver	*3448A		

FUNCTIONAL SELECTOR GUIDE (Cont.)

DESCRIPTION	HIGH-PERFORMANCE LOW-POWER SCHOTTKY	STANDARD LOW-POWER SCHOTTKY	HIGH-SPEED SCHOTTKY
OCTAL BUS TRANSCEIVERS/DRIVERS			
Octal Bus Driver, Inverting	*25LS240	*54/74LS240	*54/74S240
Octal Bus Driver, Non-Inverting (Complementary G, $\overline{G}$ Inputs)	*25LS241	*54/74LS241	*54/74S241
Octal Bus Driver, Non-Inverting	*25LS244	*54/74LS244	*54/74S244
Octal Bidirectional Bus Transceiver (Non-Inverting)			*73/8304B
Octal Bidirectional Bus Transceiver (Inverting)			*73/8303
Octal Buffer/Driver (Non-Inverting)		*81LS95	
Octal Buffer/Driver (Inverting)		*81LS96	
Octal Buffer/Driver (Non-Inverting)		*81LS97	
Octal Buffer/Driver (Inverting)		*81LS98	
OPERATORS (ALU, MULTIPLIER, PRIORITY ENCODER, etc.)			
Four by Two Two's Complement Multiplier			25S05
Four-Bit, Four-Way Shifter			*25S10/54/74S350
Four-Bit ALU/Function Generator	25LS181	54/74LS181	54/74S181
Four-Bit ALU/Function Generator	25LS2517		
Four-Bit ALU/Function Generator	25LS381	54/74LS381	
Priority Encoder, Eight Line to Three Line	25LS148	54/74LS148	
Four-Bit Serial Adder/Subtracter	25LS15		
Priority Encoder, Three-State	25LS2513		
Eight by One Serial/Parallel Two's Complement Multiplier	25LS14		
Eight-Bit by Eight-Bit Multiplier/Accumulator	*25LS2516		
Eight-Bit by Eight-Bit Combinatorial Multiplier, Latch Outputs			*25S557
Eight-Bit by Eight-Bit Combinatorial Multiplier			*25S558
Eight-Bit Comparator	25LS2521		
System Clock Generator and Driver	†25LS2525/2925		
MEMORY INTERFACE			
Dynamic Memory Controller	*25LS2564		
DECODER/DEMULTIPLEXERS			
One-of-Ten Decoder/Demultiplexer, Polarity Control	25LS2537		
One-of-Eight Decoder/Demultiplexer	25LS138	54/74LS138	54/74S138
One-of-Eight Decoder/Demultiplexer with Control Storage	*25LS2536		
Dual One-of-Four Decoder/Demultiplexer	25LS139	54/74LS139	54/74S139/93S21
One-of-Eight Decoder/Demultiplexer, Polarity Control	†25LS2538/2921		
Dual One-of-Four Decoder/Demultiplexer, Polarity Control	25LS2539		
MULTIPLEXERS			
Eight-Input Multiplexer	25LS151	54/74LS151	54/74S151
Eight-Input Multiplexer with Control Storage	†25LS2535/2922		
Three-State Eight-Input Multiplexer	25LS251	54/74LS251	54/74S251
Dual Four-Input Multiplexer	25LS153	54/74LS153	54/74S153
Three-State Dual Four-Input Multiplexer	25LS253	54/74LS253	54/74S253
Quad Two-Input Multiplexer; Non-Inverting	25LS157	54/74LS157	54/74S157/93S22
Three-State Quad Two-Input Multiplexer; Non-Inverting	25LS257	54/74LS257	54/74S257
Quad Two-Input Multiplexer; Inverting	25LS158	54/74LS158	54/74S158
Three-State Quad Two-Input Multiplexer; Inverting	25LS258	54/74LS258	54/74S258
MONOSTABLE (ONE-SHOT)			
Dual Retriggerable, Resettable Monostable Multivibrator			26S02
PARITY CHECKER/GENERATORS			
Nine-Input Parity Checker/Generator			82S62
Twelve-Input Parity Checker/Generator			93S48

*Logic Diagram and Connection Diagram are on following pages. Refer to Schottky and Low-Power Schottky Data Book for complete data sheet information.

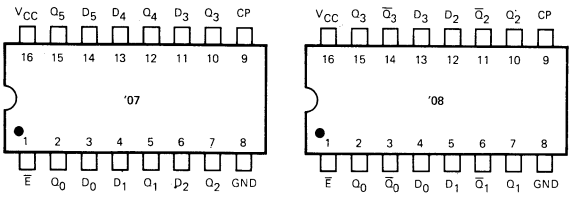
†Refer to previous sections for complete data sheet information (Am29XX)

REGISTERS

Am25LS07 • Am25LS08
Am25S07 • Am25S08

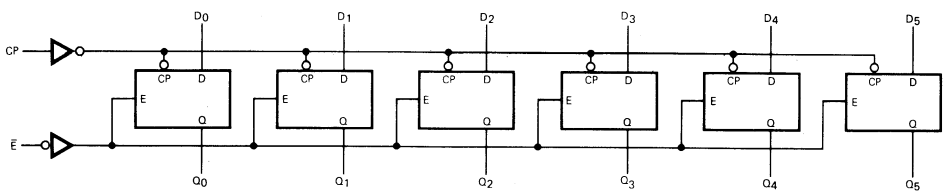
- Positive edge-triggered parallel D registers
- Common clock and common enable

CONNECTION DIAGRAMS

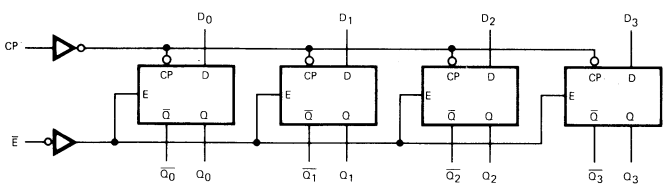


LOGIC DIAGRAMS

'07



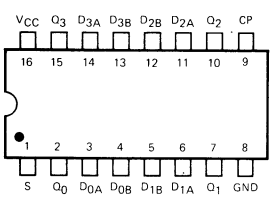
'08



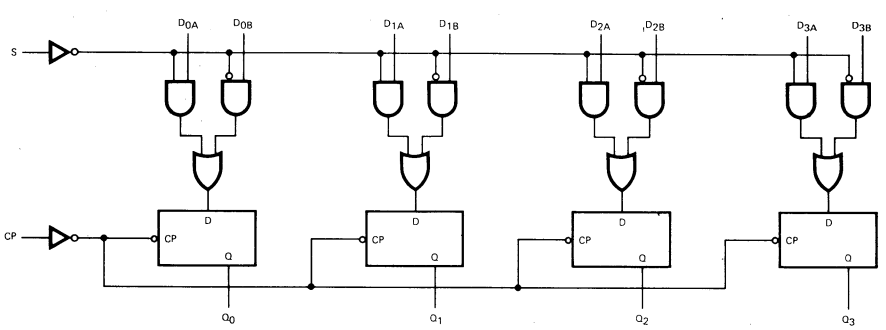
Am25LS09 • Am25S09

- 4-bit register accepts data from one-of-two 4-bit input fields
- Buffered common edge-triggered clock

CONNECTION DIAGRAM



LOGIC DIAGRAM

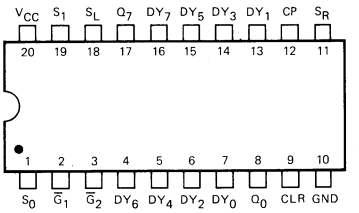


REGISTERS

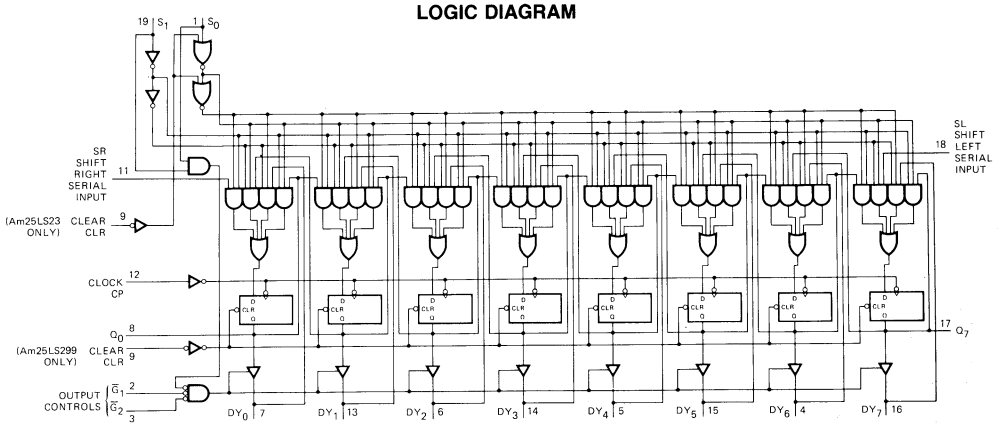
Am25LS23 • Am25LS299

- 8-bit shift/storage registers
- Four modes – Load, Shift Left, Shift Right, Store
- Synchronous clear Am25LS23, Asynchronous clear Am25LS299
- Three-state outputs
- Cascadable left or right
- Common input/output pins

CONNECTION DIAGRAM



LOGIC DIAGRAM

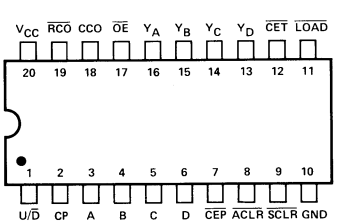


COUNTERS

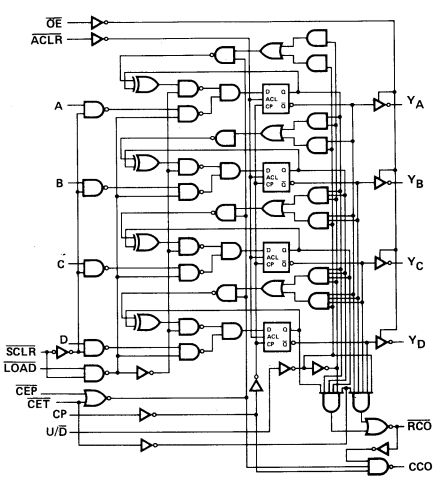
Am25LS2568 • Am25LS2569

- 4-bit synchronous counter, synchronously programmable
- Both synchronous and asynchronous clear inputs
- Three-state counter outputs interface directly with bus organized systems
- Internal look-ahead carry logic and two count enable lines for high-speed cascaded operation
- Ripple carry output for cascading
- Clock carry output for convenient modulo configuration
- Fully buffered outputs

CONNECTION DIAGRAM



LOGIC DIAGRAM Am25LS2569



Am25LS2568 is similar but limits count to binary 9.

REGISTERS

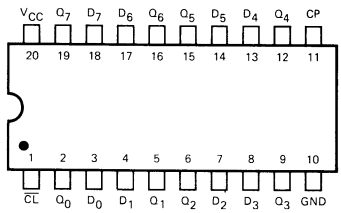
Am25LS273 • Am54LS/74LS273

- 8-bit register with common clock and common clear
- Positive edge-triggered with clock to output delay 15ns typ.
- Buffered common clock and common clear

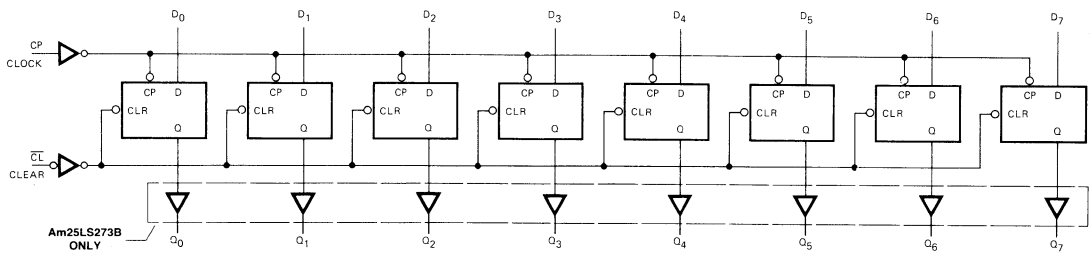
Am25LS273B

- Buffered outputs to eliminate output commutation

CONNECTION DIAGRAM



LOGIC DIAGRAM



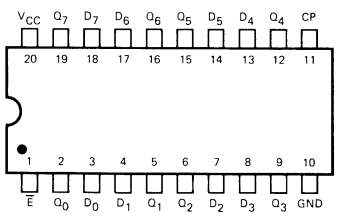
Am25LS377 • Am54LS/74LS377

- 8-bit register with common enable
- Positive edge-triggered with clock to output delay 14ns typ.
- Buffered common clock and common clock enable

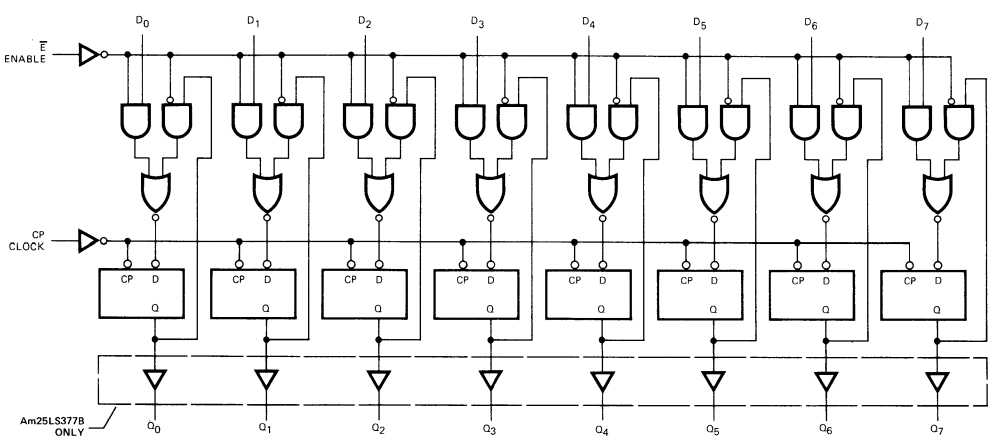
Am25LS377B

- Buffered outputs to eliminate output commutation

CONNECTION DIAGRAM



LOGIC DIAGRAM

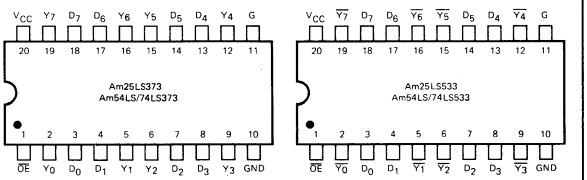


REGISTERS

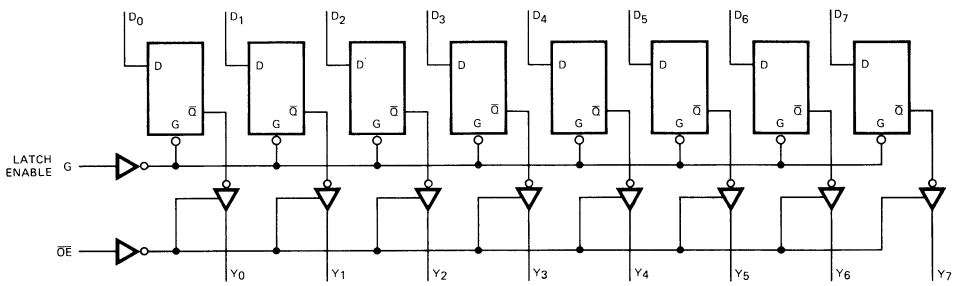
Am25LS/54LS/74LS373 • Am54S/74S373
Am25LS/54LS/74LS533 • Am54S/74S533

- Octal latches with three-state outputs
- Non-inverting outputs on '373
- Inverting outputs on '533
- Hysteresis on latch enable input

CONNECTION DIAGRAMS



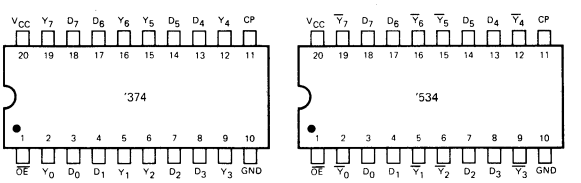
LOGIC DIAGRAM



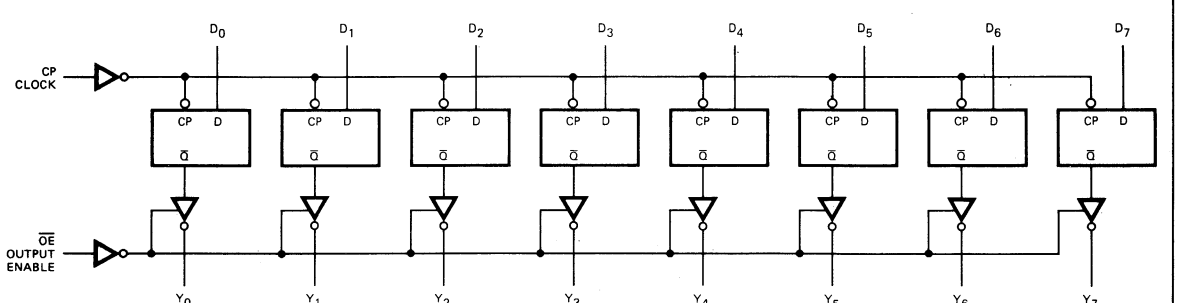
Am25LS/54LS/74LS374 • Am54S/74S374
Am25LS/54LS/74LS534 • Am54S/74S534

- 8-bit registers with three-state outputs
- Buffered common clock and common enable
- Positive edge-triggered, D-type flip-flops
- Non-inverting '374 and inverting '534

CONNECTION DIAGRAMS



LOGIC DIAGRAM



BUS TRANSCEIVERS/DRIVERS

Am25LS/54LS/74LS240/241/242/243/244

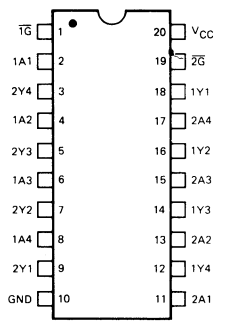
- PNP inputs and three-state outputs
- Am25LS V_{OL} specified at I_{OL} = 48mA
- Data-to-output t_{PD} = 18ns max.
- Input hysteresis 0.4V typ.
- 20-pin package with 0.300" pin row spacing

Am54S/74S240/241/242/243/244

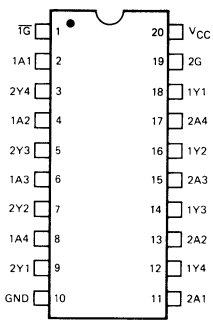
- PNP inputs and three-state outputs
- V_{OL} of 0.55V at 64mA for Am74S; 48mA for Am54S
- Data-to-output t_{PD}: Inverting = 7.0ns max., non-inverting = 9.0ns max.
- Input hysteresis 0.4V typ.
- 20-pin package with 0.300" pin row spacing

CONNECTION DIAGRAMS

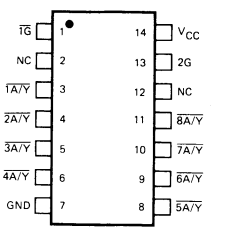
'240



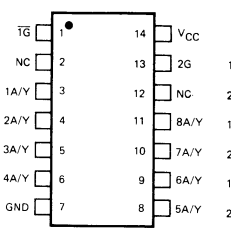
'241



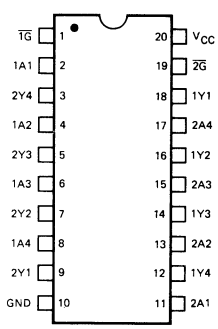
'242



'243

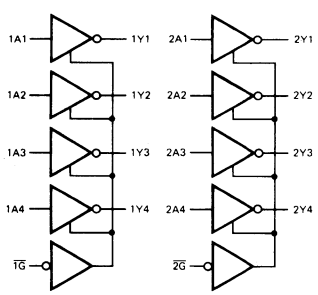


'244

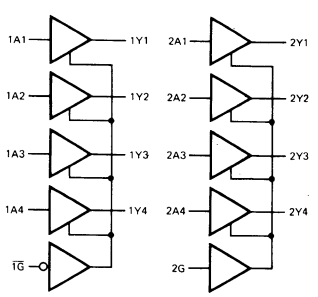


LOGIC DIAGRAMS

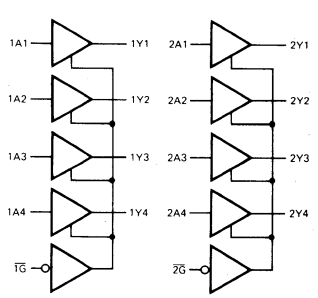
'240



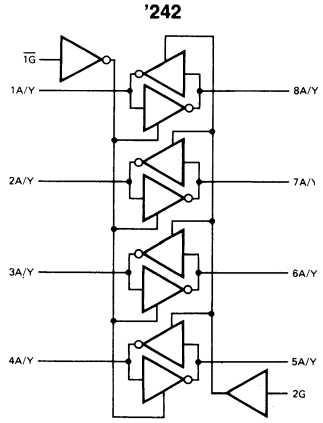
'241



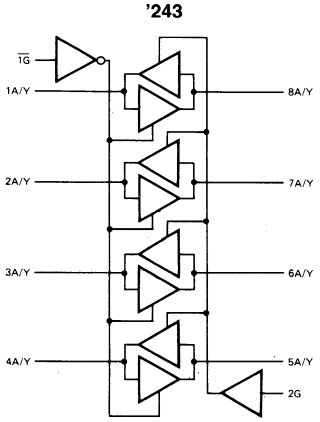
'244



'242



'243

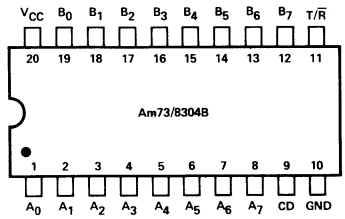


BUS TRANSCEIVERS/DRIVERS

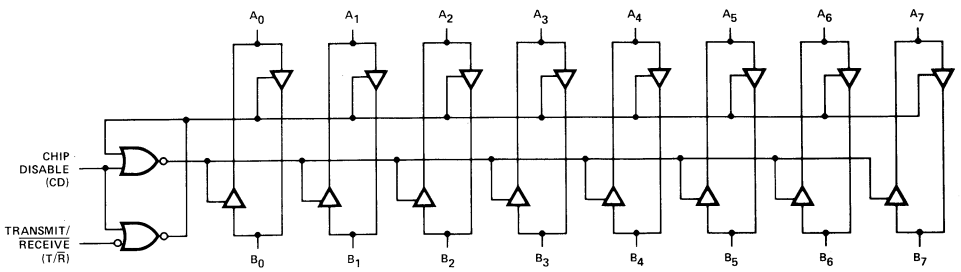
Am73/8303 • Am73/8304B

- 8-bit bidirectional data flow reduces system package count
- Three-state inputs/outputs for interfacing with bus-oriented systems
- PNP inputs reduce input loading
- V_{CC} – 1.15V V_{OH} interfaces with TTL, MOS, and CMOS
- 48mA, 300pF bus drive capability
- Transmit/Receive and Chip Disable simplify control logic
- Bus port stays in high-impedance state during power up/down

CONNECTION DIAGRAM



LOGIC DIAGRAM (DM73/8304B)

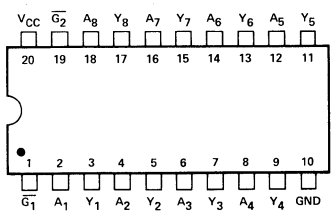


All buffers are inverting on Am73/8303B.

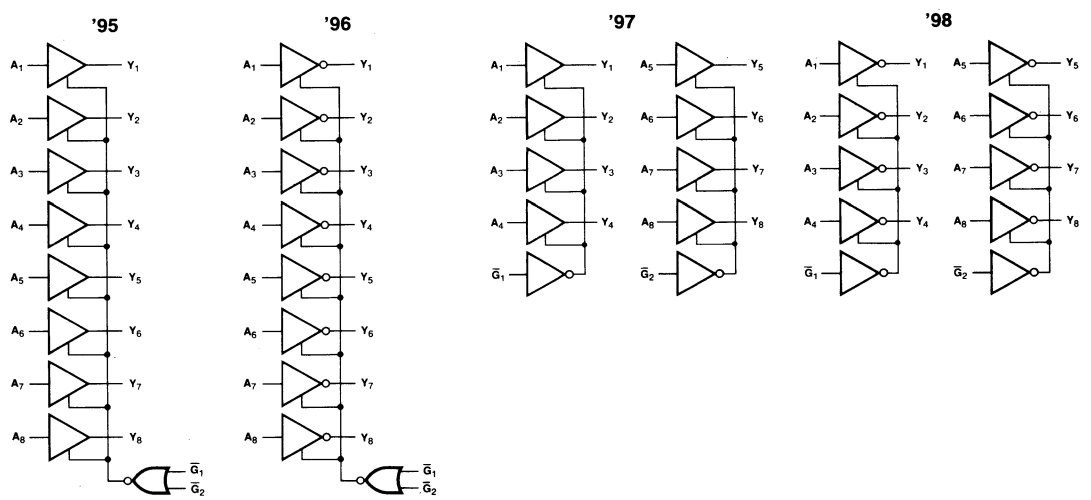
Am71/81LS95 • Am71/81LS96
Am71/81LS97 • Am71/81LS98

- 8-bit byte/nibble oriented buffers
- Three-state outputs for direct data bus drive
- PNP inputs reduce loading on bus lines
- Inverting and non-inverting versions

CONNECTION DIAGRAM



LOGIC DIAGRAMS

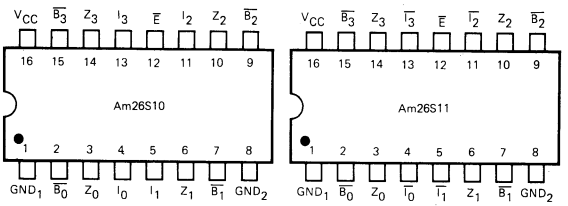


BUS TRANSCEIVERS

Am26S10 • Am26S11

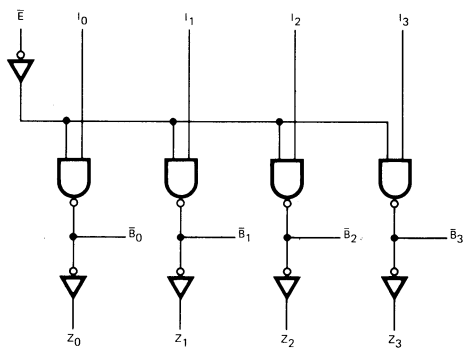
- Input to bus is inverting on Am26S10
- Input to bus is non-inverting on Am26S11
- Quad high-speed open collector bus transceivers
- Driver outputs can sink 100mA at 0.8V max.
- Bus compatible with Am2905, Am2906, and Am2907
- PNP inputs to reduce input loading

CONNECTION DIAGRAMS

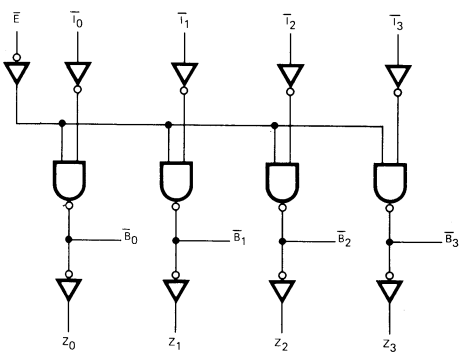


LOGIC DIAGRAMS

Am26S10



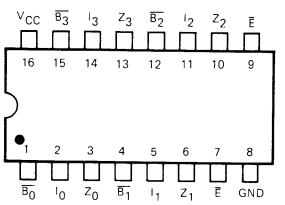
Am26S11



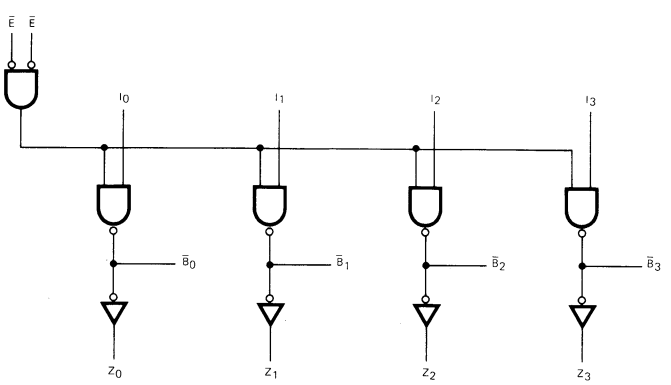
Am26S12 • Am26S12A

- Quad high-speed bus transceivers
- Driver outputs can sink 100mA at 0.7V typ.
- Open collector outputs
- Am26S12 hysteresis thresholds are 1.4V/2.0V typ.
- Am26S12A hysteresis thresholds are 1.2V/2.25V typ.

CONNECTION DIAGRAM



LOGIC DIAGRAM

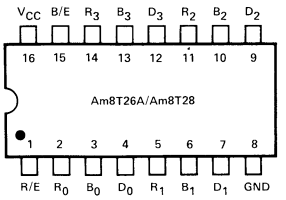


BUS TRANSCEIVERS/DRIVERS

Am8T26A • Am8T28

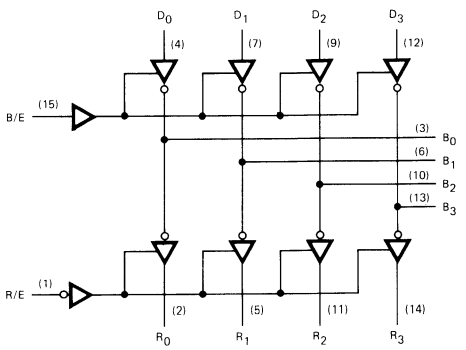
- 48mA driver sink current
- Three-state outputs on driver and receiver
- PNP inputs
- Am8T26A has inverting outputs
- Am8T28 has non-inverting outputs

CONNECTION DIAGRAM

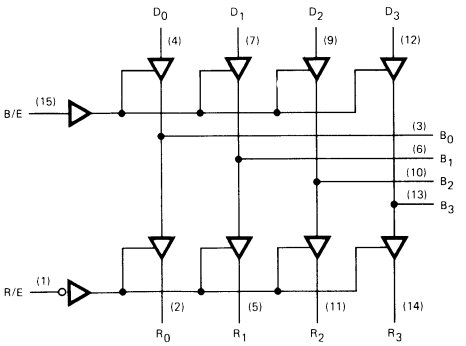


LOGIC DIAGRAMS

Am8T26A



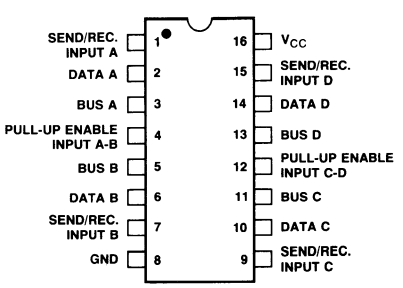
Am8T28



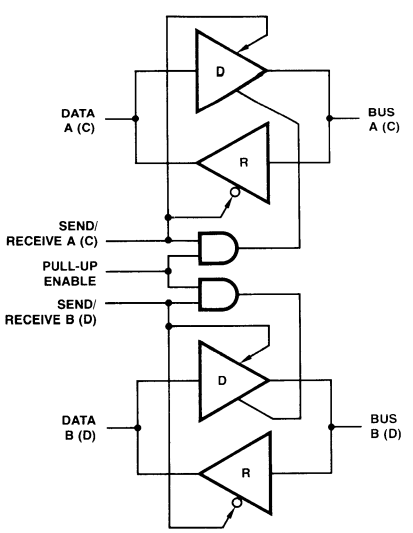
Am3448A

- IEEE-488 quad bidirectional transceiver
- Three-state outputs
- High impedance inputs
- Receiver hysteresis – 600mV typ.
- Fast propagation times – 50-20ns typ.
- TTL compatible receiver outputs
- Single +5 volt supply
- Open collector driver output option
- Power up/power down protection (No invalid information transmitted to bus)
- No bus loading when power is removed from device
- Required termination characteristics provided

CONNECTION DIAGRAM



LOGIC DIAGRAM
1/2 Am3448A

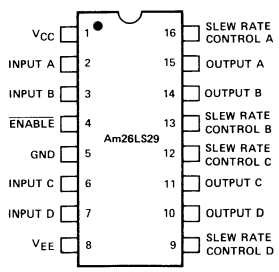


LINE DRIVERS

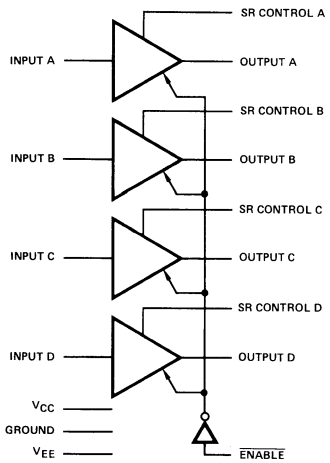
Am26LS29

- Four single-ended line drivers in one package
- Meets all requirements of RS-423
- Output short-circuit protection
- Individual rise time control for each output
- 50Ω transmission line drive capability
- High capacitive load drive capability
- Low I_{CC} and I_{EE} power consumption (26mW/driver typ.)
- Three-state outputs for bus oriented systems
- Outputs do not clamp line with power off or in high-impedance state over entire transmission line voltage range of RS-423
- Low current PNP inputs compatible with TTL, MOS and CMOS

CONNECTION DIAGRAM



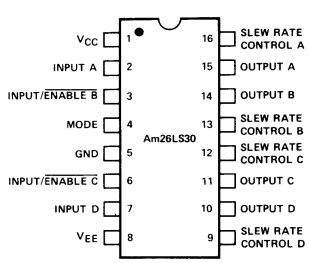
LOGIC DIAGRAM



Am26LS30

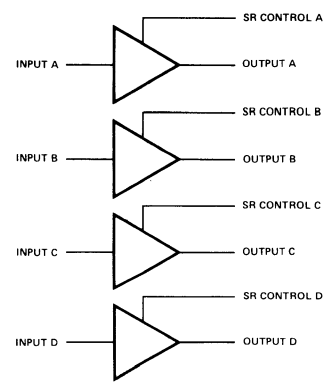
- Dual RS-422 line driver or quad RS-423 line driver
- Driver outputs do not clamp line with power off or in high-impedance state
- Individually three-state drivers when used in differential mode
- Low I_{CC} and I_{EE} power consumption
  - RS-422 differential mode 35mW/driver typ.
  - RS-423 single-ended mode 26mW/driver typ.
- Individual slew rate control for each output
- 50Ω transmission line drive capability (RS-422 into virtual ground)
- Low current PNP inputs compatible with TTL, MOS and CMOS
- High capacitive load drive capability

CONNECTION DIAGRAM

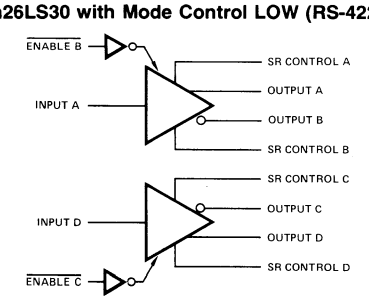


LOGIC DIAGRAMS

Am26LS30 with Mode Control HIGH (RS-423)



Am26LS30 with Mode Control LOW (RS-422)

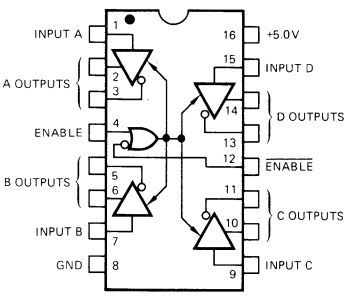


LINE DRIVERS AND RECEIVERS

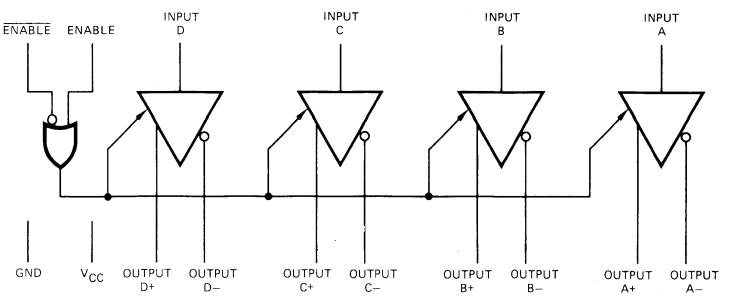
Am26LS31

- Four line drivers in one package
- Meets the requirements of EIA standard RS-422
- High output drive capability for 100Ω terminated transmission lines
- Output short-circuit protection
- Complementary outputs
- Outputs won't load line when $V_{CC} = 0$
- Output skew – 2.0ns typ.
- Input to output delay – 12ns
- Operation from single +5V supply

CONNECTION DIAGRAM



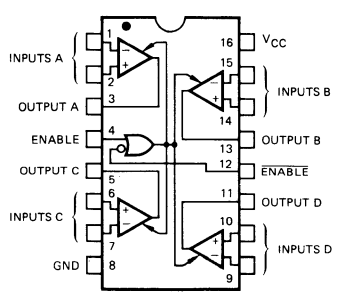
LOGIC DIAGRAM



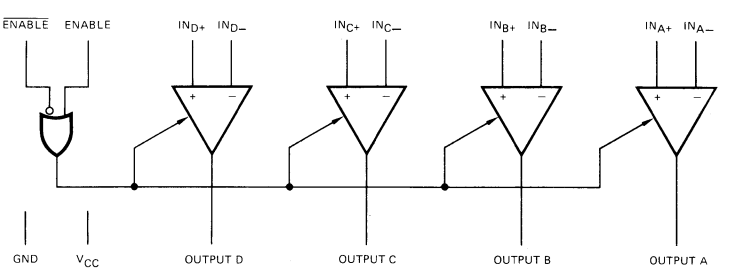
Am26LS32 • Am26LS33

- Quad differential line receivers
- Am26LS32 meets all the requirements of RS-422 and RS-423
- Input voltage range 15V on Am26LS33; 7V on Am26LS32
- ±0.2V sensitivity over the input voltage range on Am26LS32; ±0.5V sensitivity on Am26LS33
- Fail safe input/output relationship. Output always high when inputs are open
- Three-state drive, with choice of complementary output enables, for receiving directly onto a data bus
- 6k minimum input impedance
- 30mV input hysteresis
- Operation from single +5V supply

CONNECTION DIAGRAM



LOGIC DIAGRAM

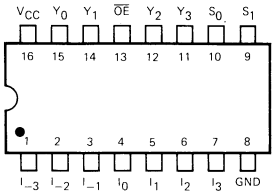


SHIFTERS

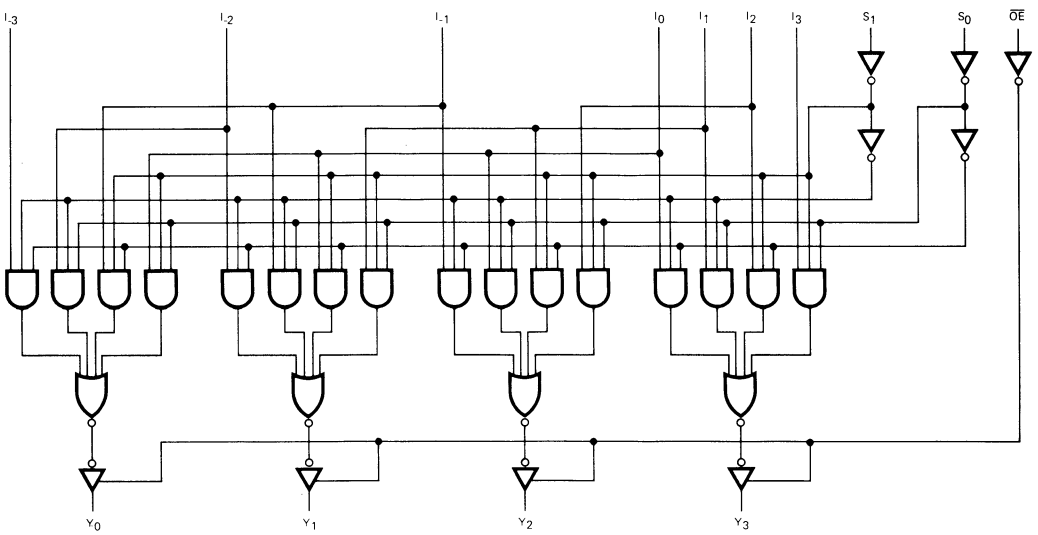
Am25S10

- Shifts 4 bits 0, 1, 2 or 3 places
- Three-state outputs
- t_{PD} 6.5ns typ.
- Easy expansion to any number of bits without propagation delay increase

CONNECTION DIAGRAM



LOGIC DIAGRAM

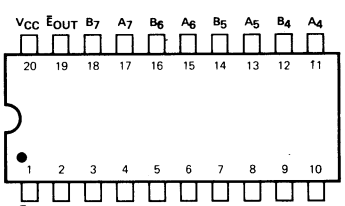


COMPARATORS

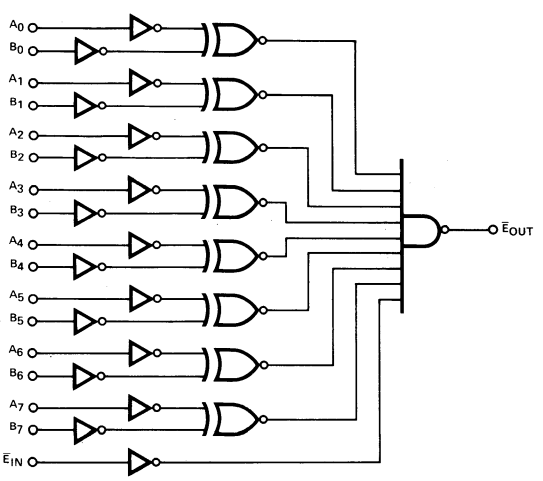
Am25LS2521

- 8-bit byte oriented equal-to comparator
- Easily cascadable using $\overline{E}_{IN}$
- Combinatorial logic with t_{PD} = 9.0ns typ.
- Broad application in conditional gating and microprocessor memory address decoding

CONNECTION DIAGRAM



LOGIC DIAGRAM

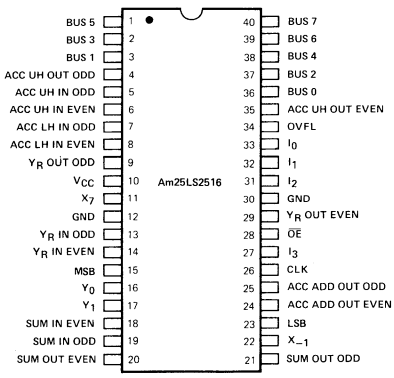


MULTIPLIERS

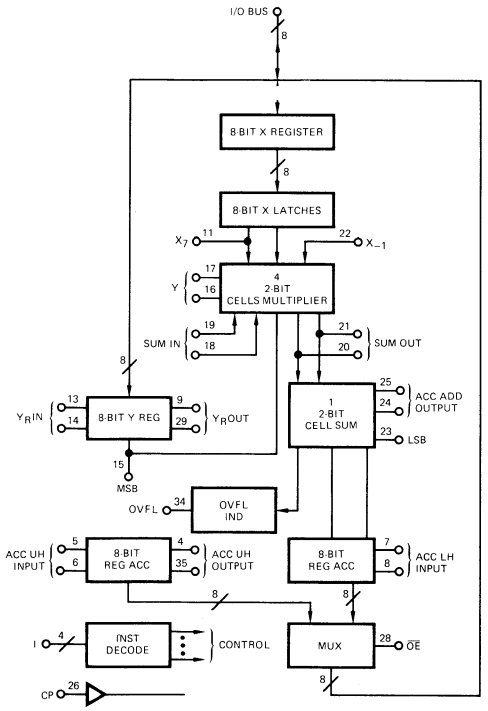
Am25LS2516

- 8-bit by 8-bit serial/parallel multiplier
- Two's complement, two-bit look-ahead carry-save arithmetic
- Microprogrammable – four-bit instruction code for load, multiply, and read operations
- Cascadable, two devices perform full 16-bit multiplication without additional hardware
- 8-bit byte parallel, bidirectional, bussed I/O
- On-chip registers and double length accumulator
- Overflow indicator
- Three-state shared bus input/output lines
- High-speed architecture provides clock rates of 20MHz typ.

CONNECTION DIAGRAM



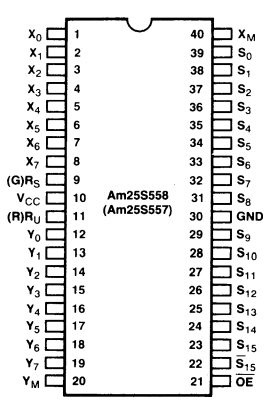
LOGIC DIAGRAM



Am25S557 • Am25S558

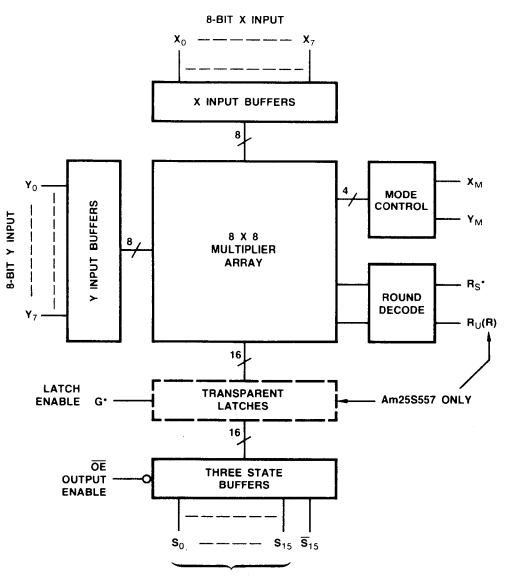
- 8-bit by 8-bit combinatorial multiplier
- Full 8 x 8 multiply in 45ns typ.
- Cascades to 16 x 16 in 110ns typ.
- Unsigned, two's complement or mixed operands
- MSB and MSB outputs for easy expansion
- Implements common rounding algorithms with additional logic
- Three-state outputs
- Transparent 16-bit latch in Am25S557

CONNECTION DIAGRAM



Pin assignments shown are for Am25S558. G and R shown in parentheses are pin assignments for Am25S557.

LOGIC DIAGRAM



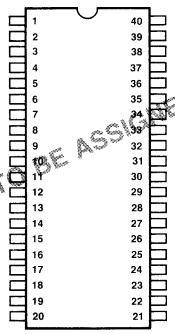
*Pin 9 is G for Am25S557 and R_S for Am25S558.

DYNAMIC MEMORY CONTROLLERS

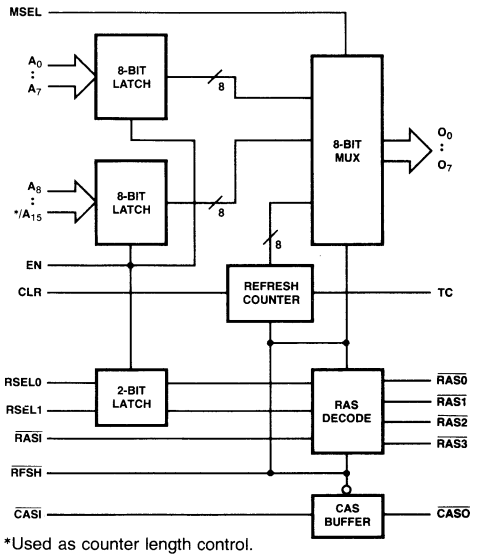
Am25LS2564

- Dynamic memory controller for 16k and 64k MOS RAMs
- 8-bit refresh counter for refresh address generation, has clear input and terminal count output
- Latched input RAS decoder provides four RAS outputs, all active during refresh
- Common chip minimizes speed differential/skew
- 3-port 8-bit address multiplexer with Schottky speed

CONNECTION DIAGRAM



LOGIC DIAGRAM
Dynamic Memory Controller



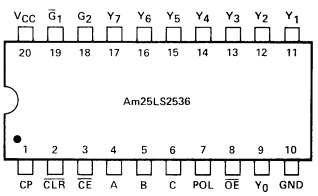
*Used as counter length control.

DECODERS

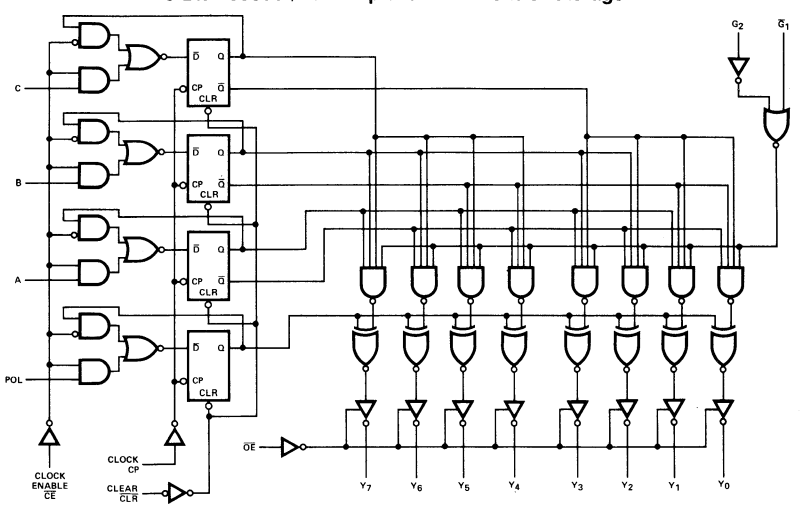
Am25LS2536

- 8-bit decoder/demultiplexer with control storage
- 3-state outputs
- Common clock enable
- Common clear
- Polarity control

CONNECTION DIAGRAM



LOGIC DIAGRAM
8-Bit Decoder/Demultiplexer with Control Storage



Product Selection Guide

MOS MICROPROCESSOR & SUPPORT CIRCUITS

AMD Part Number	Description	Availability
	CPU	
AmZ8000	0 to +70°C	3rd Q. 1979
AmZ8001	0 to +70°C	4th Q. 1979
AmZ8002	0 to +70°C	4th Q. 1979
Am8035	0 to +70°C	2nd Q. 1979
Am8048	0 to +70°C	2nd Q. 1979
Am8085A	0 to +70°C	Now
Am9085A	−55 to +125°C	Now
Am9080A/-2/-1/-4	0 to +70°C	Now
Am9080A/-2/-1	−40 to +85°C	Now
Am9080A/-2	−55 to +125°C	Now
	SECOND SOUCE SUPPORT	
Am8041	Univ. Peripheral Interface	Now
Am8212	8-Bit I/O Port	Now
Am8216	Non-Inverting Bus Transceiver	Now
Am8224	Clock Generator	Now
Am8226	Inverting Bus Transceiver	Now
Am8228	System Controller	Now
Am8238	Extended Write System Controller	Now
Am8251	Prog. Communications Interface	Now
Am8253	Programmable Interval Timer	3rd Q. 1979
Am8255	Prog. Peripheral Interface	Now
Am8255A	Prog. Peripheral Interface	Now
Am8257	Direct Memory Access Controller	Now
Am8279	Keyboard/Display	Now
	STATIC READ/WRITE RANDOM ACCESS MEMORIES	
Am8155	2K RAM with I/O	2nd Q. 1979
Am9044B/C/E	4K x 1	Now
Am9244B/C/E	4K x 1	Now
Am9101A/B/C/D	256 x 4, 22 Pin	Now
Am91L01A/B/C	256 x 4, 22 Pin	Now
Am9102A/B/C/D	1K x 1, 16 Pin	Now
Am91L02A/B/C	1K x 1, 16 Pin	Now
Am9111A/B/C/D	256 x 4, 18 Pin	Now
Am91L11A/B/C	256 x 4, 18 Pin	Now
Am9112A/B/C/D	256 x 4, 16 Pin	Now
Am91L12A/B/C	256 x 4, 16 Pin	Now
Am9114B/C/E	1K x 4, 18 Pin	Now
Am91L14B/C/E	1K x 4, 18 Pin	Now
Am9124B/C/E	1K x 4, 18 Pin	Now
Am91L24B/C/E	1K x 4, 18 Pin	Now
Am9131A/B/C/D/E	1K x 4, 22 Pin	Now
Am91L31A/B/C/D	1K x 4, 22 Pin	Now
Am9141A/B/C/D/E	4K x 1, 22 Pin	Now
Am91L41A/B/C/D	4K x 1, 22 Pin	Now
Am9044B/C/D/E	4K x 1, 18 Pin	Now
Am9244B/C/D/E	4K x 1, 18 Pin	Now
Am90L44B/C/D	4K x 1, 18 Pin	Now
Am92L44B/C/D	4K x 1, 18 Pin	Now

AMD Part Number	Description	Availability
	DYNAMIC READ/WRITE RANDOM ACCESS MEMORIES	
Am9050C/D/E	4K x 1, 18 Pin	Now
Am9060C/D/E	4K x 1, 22 Pin	Now
	MASK PROGRAMMABLE READ-ONLY MEMORIES	
Am9208B/C/D	1K x 8, 250 nsec. max.	Now
Am9216B/C	2K x 8, 300 nsec. max	Now
Am8316A	2K x 8, 850 nsec. max.	Now
Am8316E	2K x 8, 450 nsec. max.	Now
Am9232	4K x 8, 350 nsec. max.	Now
Am9233	4K x 8, 350 nsec. max.	Now
	ERASABLE READ-ONLY MEMORIES	
Am1702A/-1/-2	256 x 8, 1.0 µsec/550 nsec/650 nsec	Now
Am2708	1K x 8, 450 nsec.	Now
Am2716	2K x 8, 450 nsec.	2nd Q. 1979
Am2732	4K x 8, 450 nsec.	4th Q. 1979
	IMPROVED SUPPORT	

		REPLACES	
Am8224-4	High-Speed Generator	N/A	Now
Am8238-4	High-Speed System Controller	N/A	Now
Am9511	Arithmetic Processing Unit	N/A	Now
Am9513	System Timing Element	8253	2nd Q. 1979
Am9517	Multi-mode DMA Controller	8257	Now
Am9519	Universal Interrupt Controller	8259	Now
Am9551/-4	Prog. Communications Interface	8251	Now
Am9555	Prog. Peripheral Interface	8255	Now
Am25LS138	1-of-8 Decoder	8205	Now
Am25LS139	Dual 1-of-4 Decoder	8205	Now
***Am25LS273**	8-Bit Common Clear Register	8212	Now
***Am25LS373**	8-Bit Transparent Latch	8212	Now
***Am25LS374**	8-Bit 3-State Register	8212	Now
***Am25LS377**	8-bit Common Enable Register	8212	Now
***Am25SL2513**	Priority Encoder	8214&8212	Now
***Am25LS2537**	1-of-10 3-State Decoder	8205 (2)	Now
***Am25LS2538**	1-of-8 3-State Decoder	N/A	Now
***Am25LS2539**	Dual 1-of-4 3-State Decoder	N/A	Now

*All combine high performance and low power in space saving 20-pin package.

CPU: 9080A=480 nsec. −2=380 nsec. −1=320 nsec. −4=250 nsec.
MEM: A=500 nsec. B=400 nsec. C=300 nsec. D=250 nsec. E=200 nsec.

MOS MEMORY

STATIC R/W RANDOM-ACCESS MEMORIES

Part Number	Organization	Maximum Access Time (ns)	Temp. Range	Supply Voltage	Outputs	Data I/O Configuration	Package Pins	Operating Power Max. (mW)	Standby Power Max. (mW)
Am9101A	256 x 4	500	C, M	+5	3-State	Separate	22	290	46
Am91L01A	256 x 4	500	C, M	+5	3-State	Separate	22	173	37
Am9101B	256 x 4	400	C, M	+5	3-State	Separate	22	290	46
Am91L01B	256 x 4	400	C, M	+5	3-State	Separate	22	173	37
Am9101C	256 x 4	300	C, M	+5	3-State	Separate	22	315	46
Am91L01C	256 x 4	300	C, M	+5	3-State	Separate	22	189	37
Am9101D	256 x 4	250	C	+5	3-State	Separate	22	315	46
Am9102	1024 x 1	650	C, M	+5	3-State	Separate	16	263	42
Am91L02	1024 x 1	650	C, M	+5	3-State	Separate	16	158	35
Am9102A	1024 x 1	500	C, M	+5	3-State	Separate	16	263	42
Am91L02A	1024 x 1	500	C, M	+5	3-State	Separate	16	158	35
Am9102B	1024 x 1	400	C, M	+5	3-State	Separate	16	263	42
Am91L02B	1024 x 1	400	C, M	+5	3-State	Separate	16	158	35
Am9102C	1024 x 1	300	C, M	+5	3-State	Separate	16	290	42
Am91L02C	1024 x 1	300	C, M	+5	3-State	Separate	16	173	35
Am9102D	1024 x 1	250	C	+5	3-State	Separate	16	290	42
Am9111A	256 x 4	500	C, M	+5	3-State	Bussed	18	290	46
Am91L11A	256 x 4	500	C, M	+5	3-State	Bussed	18	173	37
Am9111B	256 x 4	400	C, M	+5	3-State	Bussed	18	290	46
Am91L11B	256 x 4	400	C, M	+5	3-State	Bussed	18	173	37
Am9111C	256 x 4	300	C, M	+5	3-State	Bussed	18	315	46
Am91L11C	256 x 4	300	C, M	+5	3-State	Bussed	18	189	37
Am9111D	256 x 4	250	C	+5	3-State	Bussed	18	315	46

MOS MEMORY

STATIC R/W RANDOM-ACCESS MEMORIES

Part Number	Organi-zation	Maximum Access Time (ns)	Temp. Range	Supply Voltage	Outputs	Data I/O Config-uraton	Package Pins	Operating Power Max (mW)	Standby Power Max (mW)	
Am9112A	256 x 4	500	C, M	+5	3-State	Bussed	16	290	46	
Am91L12A	256 x 4	500	C, M	+5	3-State	Bussed	16	173	37	
Am9112B	256 x 4	400	C, M	+5	3-State	Bussed	16	290	46	
Am91L12B	256 x 4	400	C, M	+5	3-State	Bussed	16	173	37	
Am9112C	256 x 4	300	C, M	+5	3-State	Bussed	16	315	46	
Am91L12C	256 x 4	300	C, M	+5	3-State	Bussed	16	189	37	
Am9112D	256 x 4	250	C	+5	3-State	Bussed	16	315	46	
Am9114B	1024 x 4	450	C, M	+5	3-State	Bussed	18	367		
Am9114C	1024 x 4	300	C, M	+5	3-State	Bussed	18	367		
Am9114E	1024 x 4	200	C	+5	3-State	Bussed	18	367		
Am91L14B	1024 x 4	450	C, M	+5	3-State	Bussed	18	262		
Am91L14C	1024 x 4	300	C, M	+5	3-State	Bussed	18	262		
Am91L14E	1024 x 4	200	C	+5	3-State	Bussed	18	262		
Am9124B	1024 x 4	450	C, M	+5	3-State	Bussed	18	367	157	Δ
Am9124C	1024 x 4	300	C, M	+5	3-State	Bussed	18	367	157	Δ
Am9124E	1024 x 4	200	C	+5	3-State	Bussed	18	367	157	Δ
Am91L24B	1024 x 4	450	C, M	+5	3-State	Bussed	18	262	105	Δ
Am91L24C	1024 x 4	300	C, M	+5	3-State	Bussed	18	262	105	Δ
Am91L24E	1204 x 4	200	C	+5	3-State	Bussed	18	262	105	Δ
Am9130A	1024 x 4	500	C, M	+5	3-State	Bussed	22	578	84	
Am9130B	1024 x 4	400	C, M	+5	3-State	Bussed	22	578	84	
Am9130C	1024 x 4	300	C, M	+5	3-State	Bussed	22	578	84	
Am9130D	1024 x 4	250	C	+5	3-State	Bussed	22	578	84	
Am9130E	1024 x 4	200	C	+5	3-State	Bussed	22	578	84	
Am91L30A	1024 x 4	500	C, M	+5	3-State	Bussed	22	367	72	
Am91L30B	1024 x 4	400	C, M	+5	3-State	Bussed	22	367	72	
Am91L30C	1024 x 4	300	C, M	+5	3-State	Bussed	22	367	72	
Am91L30D	1024 x 4	250	C	+5	3-State	Bussed	22	367	72	
Am9131A	1024 x 4	500	C, M	+5	3-State	Bussed	22	578	84	
Am9131B	1024 x 4	400	C, M	+5	3-State	Bussed	22	578	84	
Am9131C	1024 x 4	300	C, M	+5	3-State	Bussed	22	578	84	
Am9131D	1024 x 4	250	C	+5	3-State	Bussed	22	578	84	
Am9131E	1024 x 4	200	C	+5	3-State	Bussed	22	578	84	
Am91L31A	1024 x 4	500	C, M	+5	3-State	Bussed	22	367	72	
Am91L31B	1024 x 4	400	C, M	+5	3-State	Bussed	22	367	72	
Am91L31C	1024 x 4	300	C, M	+5	3-State	Bussed	22	367	72	
Am91L31D	1024 x 4	250	C	+5	3-State	Bussed	22	367	72	
Am9140A	4096 x 1	500	C, M	+5	3-State	Separate	22	578	84	
Am9140B	4096 x 1	400	C, M	+5	3-State	Separate	22	578	84	
Am9140C	4096 x 1	300	C, M	+5	3-State	Separate	22	578	84	
Am9140D	4096 x 1	250	C	+5	3-State	Separate	22	578	84	
Am9140E	4096 x 1	200	C	+5	3-State	Separate	22	578	84	
Am91L40A	4096 x 1	500	C, M	+5	3-State	Separate	22	367	72	
Am91L40B	4096 x 1	400	C, M	+5	3-State	Separate	22	367	72	
Am91L40C	4096 x 1	300	C, M	+5	3-State	Separate	22	367	72	
Am91L40D	4096 x 1	250	C	+5	3-State	Separate	22	367	72	
Am9141A	4096 x 1	500	C, M	+5	3-State	Separate	22	578	84	
Am9141B	4096 x 1	400	C, M	+5	3-State	Separate	22	578	84	
Am9141C	4096 x 1	300	C, M	+5	3-State	Separate	22	578	84	
Am9141D	4096 x 1	250	C	+5	3-State	Separate	22	578	84	
Am9141E	4096 x 1	200	C	+5	3-State	Separate	22	578	84	
Am91L41A	4096 x 1	500	C, M	+5	3-State	Separate	22	367	72	
Am91L41B	4096 x 1	400	C, M	+5	3-State	Separate	22	367	72	
Am91L41C	4096 x 1	300	C, M	+5	3-State	Separate	22	367	72	
Am91L41D	4096 x 1	250	C	+5	3-State	Separate	22	367	72	
Am9044B	4096 x 1	450	C, M	+5	3-State	Separate	18	385		
Am9044C	4096 x 1	300	C, M	+5	3-State	Separate	18	385		
Am9044D	4096 x 1	250	C, M	+5	3-State	Separate	18	385		
Am9044E	4096 x 1	200	C	+5	3-State	Separate	18	385		
Am9244B	4096 x 1	450	C, M	+5	3-State	Separate	18	385	165	Δ
Am9244C	4096 x 1	300	C, M	+5	3-State	Separate	18	385	165	Δ
Am9244D	4096 x 1	250	C, M	+5	3-State	Separate	18	385	165	Δ
Am9244E	4096 x 1	200	C	+5	3-State	Separate	18	385	165	Δ
Am90L44B	4096 x 1	450	C, M	+5	3-State	Separate	18	275		
Am90L44C	4096 x 1	300	C, M	+5	3-State	Separate	18	275		
Am90L44D	4096 x 1	250	C	+5	3-State	Separate	18	275		
Am92L44B	4096 x 1	450	C, M	+5	3-State	Separate	18	275	110	Δ
Am92L44C	4096 x 1	300	C, M	+5	3-State	Separate	18	275	110	Δ
Am92L44D	4096 x 1	250	C	+5	3-State	Separate	18	275	110	Δ
***Am9147-70	4096 x 1	70	C, M	+5	3-State	Separate	18	990	165	Δ
***Am9147-55	4096 x 1	55	C	+5	3-State	Separate	18	990	165	Δ

ΔAutomatic power down with chip select.

MOS MEMORY

DYNAMIC R/W RANDOM-ACCESS MEMORIES

Part Number	Organization	Maximum Access Time (ns)	Temp. Range	Supply Voltages	Operating Power (mW)	Outputs	Data I/O Configuration	Package Pins	Refresh Time (ns)	Standby Power-Max. (mW)
Am9050C	4096 x 1	300	C	−5, +12	750	Open Drain	Bussed	18	2.0	3.0
Am9050D	4096 x 1	250	C	−5, +12	750	Open Drain	Bussed	18	2.0	3.0
Am9050E	4096 x 1	200	C	−5, +12	750	Open Drain	Bussed	18	2.0	3.0
Am9060C	4096 x 1	300	C	±5, +12	750	3-State	Separate	22	2.0	3.0
Am9060D	4096 x 1	250	C	±5, +12	750	3-State	Separate	22	2.0	3.0
Am9060E	4096 x 1	200	C	±5, +12	750	3-State	Separate	22	2.0	3.0
Am90L50C	4096 x 1	300	C	−5, +12	396	Open Drain	Bussed	18	2.0	3.0
Am90L50D	4096 x 1	250	C	−5, +12	396	Open Drain	Bussed	18	2.0	3.0
Am90L50E	4096 x 1	200	C	−5, +12	396	Open Drain	Bussed	18	2.0	3.0
Am90L60C	4096 x 1	300	C	±5, +12	396	3-State	Separate	22	2.0	3.0
Am90L60D	4096 x 1	250	C	±5, +12	396	3-State	Separate	22	2.0	3.0
Am90L60E	4096 x 1	200	C	±5, +12	396	3-State	Separate	22	2.0	3.0
**Am9016C	16384 x 1	300	C	±5, +12	480	3-State	Separate	16	2.0	20.0
**Am9016D	16384 x 1	250	C	±5, +12	480	3-State	Separate	16	2.0	20.0
**Am9016E	16384 x 1	200	C	±5, +12	480	3-State	Separate	16	2.0	20.0
Am9016F	16384 x 1	150	C	±5, +12	480	3-State	Separate	16	2.0	20.0

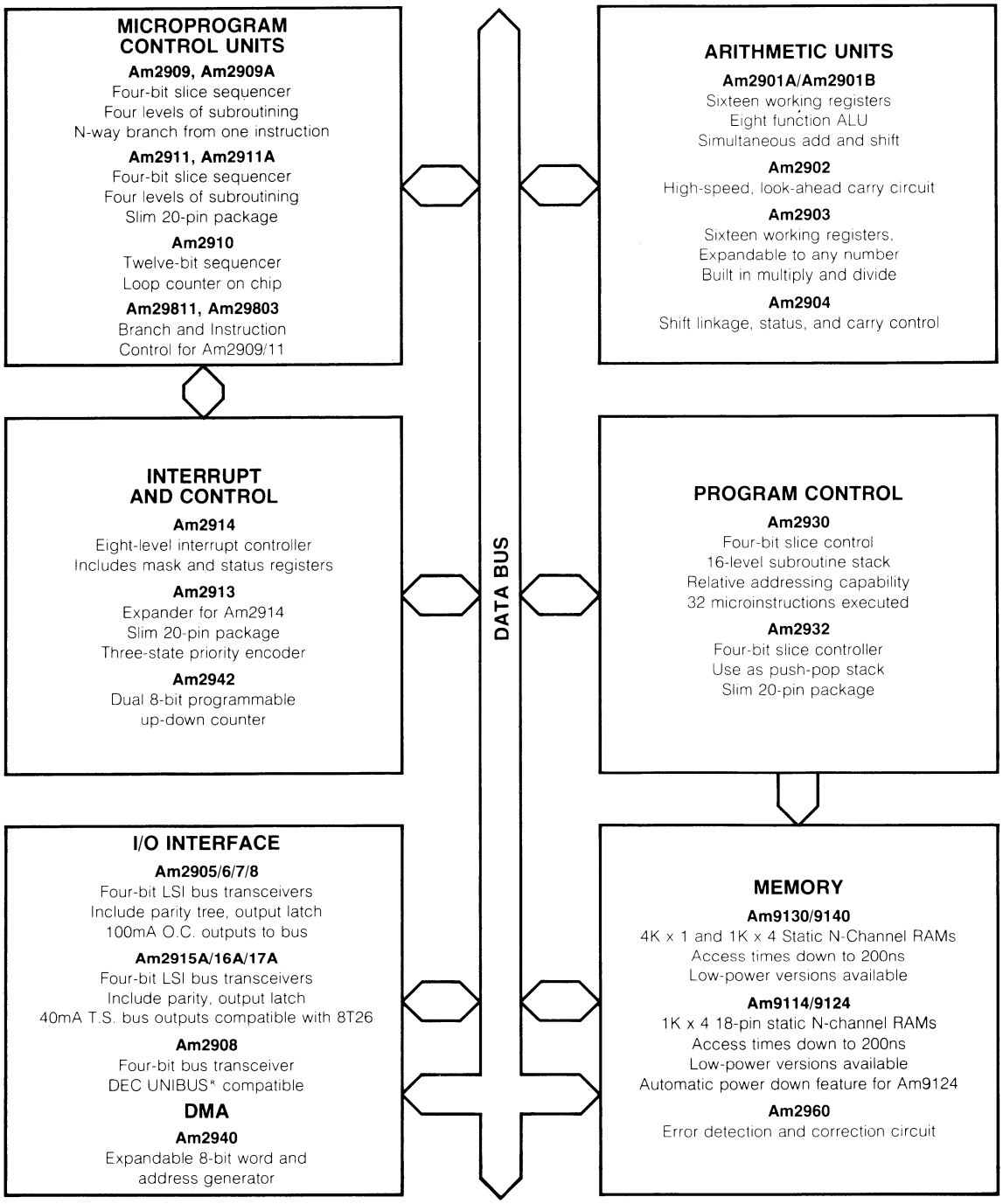
READ-ONLY MEMORIES

Part Number	Organization	Access Time (ns)	Temp. Range	Supply Voltages	Operating Power – Max. (mW)	Outputs
C8316A	2048 x 8	850	C	+5	514	3-State
C8316E	2048 x 8	450	C	+5	499	3-State
Am9208B	1024 x 8	400	C, M	+5, +12	620	3-State
Am9208C	1024 x 8	300	C, M	+5, +12	620	3-State
Am9208D	1024 x 8	250	C	+5, +12	700	3-State
Am9214	512 x 8	500	C, M	+5	263	3-State
Am9216B	2048 x 8	400	C, M	+5, +12	660	3-State
Am9216C	2048 x 8	300	C	+5, +12	700	3-State
Am9217A	2048 x 8	550	C, M	+5	367	3-State
Am9217B	2048 x 8	450	C, M	+5	367	3-State
Am9218B	2048 x 8	450	C, M	+5	367	3-State
Am9218C	2048 x 8	350	C	+5	367	3-State
**Am9232	4096 x 8	350	C, M	+5	500	3-State

ERASABLE PROGRAMMABLE READ-ONLY MEMORY

Part Number	Organization	Access Time (nsec)	Temp. Range	Supply Voltages	Operating Power – Max. (mW)	Outputs
Am1702A	256 x 8	1000	C, E	−9V, +5V	676	3-State
Am1702A-1	256 x 8	550	C, E	−9V, +5V	676	3-State
Am1702A-2	256 x 8	650	C, E	−9V, +5V	676	3-State
Am1702AL	256 x 8	1000	C, E	−9V, +5V	–	3-State
Am1702AL-1	256 x 8	550	C, E	−9V, +5V	–	3-State
Am1702AL-2	256 x 8	650	C, E	−9V, +5V	–	3-State
Am2708	1024 x 8	450	C, M	+5V, +12V, −5V	800	3-State
**Am2716	2048 x 8	450	C	+5V	–	3-State
****Am2732	4192 x 8	450	C	+5V	–	3-State

BIPOLAR MICROPROCESSOR AND SUPPORT CIRCUITS



SOFTWARE AND HARDWARE

Am2900K1 Evaluation and Learning Kit
An introduction to microprogramming

AMDASM Microprogram Assembler
General Purpose meta-assembler for microinstructions up to 128 bits wide

System 29 Complete hardware and firmware development system.

APPLICATIONS MATERIAL

A 16-bit Microprogrammed Computer
The Microprogramming Handbook
Microprogrammable Interrupt using the Am2914
High Performance Disc Controller
Emulation of the Am9080A/8228
How To Build A Microcomputer (10-part series)
Microprogramming Card
Microprogram Design with the Am2900 Family

BIPOLAR MEMORY

STATIC R/W RANDOM-ACCESS MEMORIES

Part Number	Organization	Maximum Access Time (ns)	Temp. Range	Operating Power – Max. (mW)	Outputs
Am3101	16 x 4	60	C	550	Open Collector
Am3101-1XC†	16 x 4	35	C	525	Open Collector
Am3101-1XM†	16 x 4	50	M	580	Open Collector
Am5489-1†	16 x 4	50	M	580	Open Collector
Am7489	16 x 4	60	C	550	Open Collector
Am7489-1†	16 x 4	35	C	525	Open Collector
Am31L01AXC	16 x 4	55	C	185	Open Collector
Am31L01AXM	16 x 4	65	M	210	Open Collector
Am27S02XC	16 x 4	35	C	550	Open Collector
Am27S02XM	16 x 4	50	M	580	Open Collector
Am27S03XC	16 x 4	35	C	550	3-State
Am27S03XM	16 x 4	50	M	580	3-State
Am27S02AXC	16 x 4	25	C	525	Open Collector
Am27S02AXM	16 x 4	30	M	580	Open Collector
Am27S03AXC	16 x 4	25	C	525	3-State
Am27S03AXM	16 x 4	30	M	580	3-State
Am27LS02XC	16 x 4	55	C	185	Open Collector
Am27LS02XM	16 x 4	65	M	210	Open Collector
Am27LS03XC	16 x 4	55	C	185	3-State
Am27LS03XM	16 x 4	65	M	210	3-State
Am27S06XC††	16 x 4	25	C	525	Open Collector
Am27S06XM††	16 x 4	30	M	580	Open Collector
Am27S07XC††	16 x 4	25	C	525	3-State
Am27S07XM††	16 x 4	30	M	580	3-State
Am27LS06XC††	16 x 4	55	C	185	Open Collector
Am27LS06XM††	16 x 4	65	M	210	Open Collector
Am27LS07XC††	16 x 4	55	C	185	3-State
Am27LS07XM††	16 x 4	65	M	210	3-State
Am27LS00AXC	256 x 1	35	C	525	3-State
Am27LS00AXM	256 x 1	45	M	550	3-State
Am27LS00XC	256 x 1	45	C	370	3-State
Am27LS00XM	256 x 1	55	M	385	3-State
Am27LS01AXC	256 x 1	35	C	525	Open Collector
Am27LS01AXM	256 x 1	45	M	550	Open Collector
Am27LS01XC	256 x 1	45	C	370	Open Collector
Am27LS01XM	256 x 1	55	M	385	Open Collector

†Option of new improved Am27S02A featuring higher speed and write cycle transparency similar to Am3101 and Am7489
††Same as Am27S02A/03A and Am27LS02/03 respectively with non-inverting outputs

BIPOLAR MEMORY

READ-ONLY MEMORIES

Part Number	Organization	Access Time	Temp. Range	Power Supplies	Operating Power (mW)	Outputs
Am27S80XC	1024 x 8	175	C	+5V	895	Open Collector
Am27S80XM	1024 x 8	275	M	+5V	935	Open Collector
Am27S81XC	1024 x 8	175	C	+5V	895	3-State
Am27S81XM	1024 x 8	275	M	+5V	935	3-State
Am27S82XC†††	1024 x 8	175	C	+5V	895	Open Collector
Am27S82XM†††	1024 x 8	275	M	+5V	935	Open Collector
Am27S83XC†††	1024 x 8	175	C	+5V	895	3-State
Am27S83XM†††	1024 x 8	275	M	+5V	935	3-State

†††Same as Am27S80 and Am27S81 with OR Enable Chip Select.

PROGRAMMABLE READ-ONLY MEMORIES

Part Numbers	Organization	Access Time	Temp. Range	Power Supplies	Operating Power (mW)	Package Pins	Outputs
Am27S18XC	32 x 8	40	C	+5V	605	16	Open Collector
Am27S18XM	32 x 8	50	M	+5V	635	16	Open Collector
Am27S19XC	32 x 8	40	C	+5V	605	16	3-State
Am27S19XM	32 x 8	50	M	+5V	635	16	3-State
Am27LS20XC	256 x 4	45	C	+5V	685	16	Open Collector
Am27LS20XM	256 x 4	60	M	+5V	715	16	Open Collector
Am27LS21XC	256 x 4	45	C	+5V	685	16	3-State
Am27LS21XM	256 x 4	60	M	+5V	715	16	3-State
Am27S12XC	512 x 4	50	C	+5V	685	16	Open Collector
Am27S12XM	512 x 4	60	M	+5V	715	16	Open Collector
Am27S13XC	512 x 4	50	C	+5V	685	16	3-State
Am27S13XM	512 x 4	60	M	+5V	715	16	3-State
Am27S15XC	512 x 8	60	C	+5V	920	24	3-State w/Latches
Am27S15XM	512 x 8	90	M	+5V	1020	24	3-State w/Latches
Am27S26XC	512 x 8	N.A.†	C	+5V	970	22	Open Collector w/Registers
Am27S26XM	512 x 8	N.A.†	M	+5V	1020	22	Open Collector w/Registers
Am27S27XC	512 x 8	N.A.†	C	+5V	970	22	3-State w/Registers
Am27S27XM	512 x 8	N.A.†	M	+5V	1020	22	3-State w/Registers
**Am27S32XC	1024 x 4	55	C	+5V	735	18	Open Collector
**Am27S32XM	1024 x 4	70	M	+5V	800	18	Open Collector
**Am27S33XC	1024 x 4	55	C	+5V	735	18	3-State
**Am27S33XM	1024 x 4	70	M	+5V	800	18	3-State
Am27S28XC	512 x 8	55	C	+5V	920	20	Open Collector
Am27S28XM	512 x 8	70	M	+5V	965	20	Open Collector
Am27S29XC	512 x 8	55	C	+5V	920	20	3-State
Am27S29XM	512 x 8	70	M	+5V	965	20	3-State
Am27S30XC	512 x 8	55	C	+5V	920	24	Open Collector
Am27S30XM	512 x 8	70	M	+5V	965	24	Open Collector
Am27S31XC	512 x 8	55	C	+5V	920	24	3-State
Am27S31XM	512 x 8	70	IM	+5V	965	24	3-State
***Am27S180XC	1024 x 8	60	C	+5V	920	24	Open Collector
***Am27S180XM	1024 x 8	80	M	+5V	1020	24	Open Collector
***Am27S181XC	1024 x 8	60	C	+5V	920	24	3-State
***Am27S181XM	1024 x 8	80	M	+5V	1020	24	3-State

†Normal Access time not applicable – this product contains built-in pipeline registers – nominal address to clock set up time 40ns, clock to output 15ns.

PRODUCT GUIDE

SILICON GATE MOS CIRCUITS

Am1002	Dual 128-Bit Static Shift Register
Am1101A	256-Bit Random Access Memory
Am1402A	Quad 256-Bit Shift Register
Am1403A	Dual 512-Bit Shift Register
Am1404A	1024-Bit Shift Register
Am1405A	512-Bit Shift Register with Recirculate
Am14/1506	Dual 100-Bit Shift Register
Am14/1507	Dual 100-Bit Shift Register
Am1702A/-1/-2	2048-Bit E-PROM
Am2101	256 x 4-Bit Static N-Channel RAM
Am2102	1024-Bit Static N-Channel RAM
Am2111	256 x 4-Bit Static N-Channel RAM
Am2112	256 x 4-Bit Static N-Channel RAM
Am2401	2048-Bit Dyn. N-Channel Shift Register
Am2405	1024-Bit Dyn. N-Channel Shift Register
Am2505	512-Bit Dyn. Shift Register
Am2512	1024-Bit Dyn. Shift Register
Am2521	Dual 128-Bit Static Shift Register
Am2524	512-Bit Shift Register with Recirculate
Am2525	1024-Bit Shift Register with Recirculate
Am2533	1024-Bit Static Shift Register
Am2602	1024-Bit Static N-Channel RAM
Am2708	8192-Bit Erasable PROM
**Am2716	16K-Bit Erasable PROM
Am2732	32K-Bit Erasable PROM
Am2802	10MHz Quad 256-Bit Shift Register
Am2803	10MHz Dual 512-Bit Shift Register
Am2804	10MHz Single 1024-Bit Shift Register
Am2805	512-Bit Shift Register with Recirculate
Am2806	1024-Bit Shift Register with Recirculate
Am2807	512-Bit Shift Register with Recirculate
Am2808	1024-Bit Shift Register with Recirculate
Am2809	Dual 128-Bit Static Shift Register
Am2810	Dual 128-Bit Static Shift Register
Am2812	32 x 8-Bit FIFO Memory
Am2813	32 x 9-Bit FIFO Memory
Am2814	Dual 128-Bit Static Shift Register
Am2825	Dual 1024-Bit Shift Register
Am2826	Dual 1024-Bit Shift Register
Am2827	2048-Bit Shift Register
Am2833	1024-Bit Static Shift Register
Am2841	64 x 4-Bit FIFO Memory
Am2847	Quad 80-Bit Shift Register
Am2855	Quad 128-Bit Static Shift Register
Am2856	Dual 256-Bit Static Shift Register
Am2857	512-Bit Static Shift Register
Am2896	Quad 96-Bit Static Shift Register
Am3114	Dual 128-Bit Static Shift Register
Am3120	Quad 80-Bit Static Shift Register
Am3128	Dual 128-Bit Static Shift Register
Am3341	64 x 4-Bit FIFO Memory
Am3341A	64 x 4-Bit FIFO Memory
Am3347	Quad 80-Bit Static Shift Register
Am3514	512 x 8-Bit Read Only Memory
Am40/5025	Dual 1024-Bit Shift Register
Am40/5026	Dual 1024-Bit Shift Register
Am40/5027	2048-Bit Shift Register with Recirculate
Am40/5055	Quad 128-Bit Static Shift Register
Am40/5056	Dual 256-Bit Static Shift Register
Am40/5057	512-Bit Static Shift Register
Am4102	1024-Bit Static N-Channel RAM
Am7552	1024-Bit Static N-Channel RAM
****AmZ8001	16-Bit Microprocessor – Segmented
****AmZ8002	16-Bit Microprocessor – Unsegmented
**Am8035	8-Bit Single Chip Microcomputer
**Am8041	Universal Peripheral Interface
*Am8048	8-Bit Single Chip Microcomputer
Am8085A	8-Bit Microprocessor
**Am8155	2K RAM with I/O
Am8212	8-Bit I/O Port
Am8216	Non-Inverting Bus Transceiver
Am8224	Clock Generator
Am8224-4	High-Speed Generator
Am8226	Inverting Bus Transceiver
Am8228	System Controller
Am8238	Extended Wire System Controller
Am8238-4	High-Speed System Controller
Am8251	Programmable Communications Interface
**Am8253	Programmable Interval Timer
Am8255	Programmable Peripheral Interface
Am8255A	Programmable Peripheral Interface
Am8257	DMA Controller
Am8279	Keyboard/Display
Am8316A	2048 x 8-Bit Read Only Memory 5V Only
Am8316E	2048 x 8-Bit Read Only Memory 5V Only
**Am9016	16384-Bit Dyn. N-Channel RAM, 16-Pin
Am9050	4096-Bit Dyn. N-Channel RAM, 18-Pin
Am90L50	Low-Power 4096-Bit Dynamic N-Channel RAM, 18-Pin
Am9060	4096-Bit Dyn. N-Channel RAM, 22-Pin
Am90L60	Low-Power 4096-Bit Dynamic N-Channel RAM, 22-Pin
Am9080A/-2/-1/-4	8-Bit Microprocessor
Am9101	256 x 4-Bit Static N-Channel RAM
Am91L01	Low-Power 256 x 4-Bit RAM
Am9102	1024-Bit Static N-Channel RAM
Am91L02	Low-Power 1024-Bit RAM
Am9111	256 x 4-Bit Static N-Channel RAM
Am91L11	Low-Power 256 x 4-Bit RAM
Am9112	256 x 4-Bit Static N-Channel RAM
Am91L12	Low-Power 256 x 4-Bit RAM
Am9114	1024 x 4 Static N-Channel RAM, 18-Pin
Am91L14	Low-Power 1024 x 4 Static N-Channel RAM, 18-Pin
Am9124	1024 x 4 Static N-Channel RAM, 18-Pin
Am91L24	Low-Power 1024 x 4 Static N-Channel RAM, 18-Pin
Am9130	1024 x 4-Bit Static RAM
Am91L30	1024 x 4-Bit Low-Power Static RAM
Am9131	1024 x 4-Bit Static RAM
Am91L31	1024 x 4-Bit Low-Power Static RAM
Am9140	4096 x 1-Bit Static RAM
Am91L40	4096 x 1-Bit Low-Power Static RAM
Am9141	4096 x 1-Bit Static RAM
Am91L41	4096 x 1-Bit Low-Power Static RAM
Am9044	4096 x 1-Bit Static RAM, 18 Pin
Am90L44	Low-Power 4096 x 1-Bit Static RAM, 18 Pin
Am9244	4096 x 1-Bit Static RAM with Power Down, 18-Pin
Am92L44	Low-Power 4096 x 1-Bit RAM with Power Down, 18-Pin
Am9147	Very High-Speed 4096 x 1-Bit Static RAM, 18 Pin
Am9208	1024 x 8-Bit Read Only Memory
Am9214	512 x 8-Bit Read Only Memory
Am9216	2048 x 8-Bit Read Only Memory
Am9217	2048 x 8-Bit Read Only Memory
Am9218	2048 x 8-Bit Read Only Memory
Am9232	4096 x 8-Bit Read Only Memory
Am9233	4096 x 8-Bit Read Only Memory
Am9401	2048-Bit Dyn. N-Channel Shift Register
Am9511	Arithmetic Processor Unit
**Am9513	System Timing Element
Am9517	Multimode DMA Controller
Am9519	Universal Interrupt Controller
Am9551	Programmable Communications Interface
Am9555	Programmable Peripheral Interface
Am9702	2048-Bit E-PROM

INTERFACE CIRCUITS

Am0026/0026C	5MHz Two-Phase MOS Clock Driver
Am0056/0056C	MOS Clock Driver
Am1603/3603	Dual Differential Line Receiver
Am3604	Dual MOS Sense Amp/Line Receiver
Am555	Precision Timer
Am556	Dual Precision Timer
Am1488	Quad EIA Line Driver
Am1489/89A	Quad EIA Line Receiver
Am25LS240	Octal Inv. Buffer
Am25LS241	Octal Non-Inv. Buffer
Am25LS242	Quad Bus Transceiver
Am25LS243	Quad Bus Transceiver
Am25LS244	Octal Non-Inv. Buffer
Am2602	Dual One-Shot
Am26L02	Low-Power, Dual One-Shot
Am2614	Quad Single-Ended, High-Speed Line Driver
Am2615	Dual Single-Ended, Fail-Safe Line Receiver
Am2616	EIA/MIL 188C Quad Line Driver
Am2617	EIA Quad Line Receiver
Am26123	Dual One-Shot
Am26LS29	Quad Line Driver (RS-423)

Am26LS30	Quad Line Driver (RS-423)
Am26LS31	Quad Line Driver (RS-422)
Am26LS32	Quad Line Receiver (RS-422/3)
Am26LS33	Quad Line Receiver
Am26S02	Schottky Dual One Shot
Am26S10	Schottky Quad Bus Transceiver
Am26S11	Schottky Quad Bus Transceiver
Am26S12/12A	Schottky Quad Bus Transceiver
Am2905	Quad Two-Port Bus Transceiver (O.C.)
Am2906	Quad Two-Port Bus Transceiver with Parity (O.C.)
Am2907	Quad Bus Transceiver with Parity (O.C.)
Am2915A	Quad Two Port Bus Transceiver (3-State)
Am2916A	Quad Two Port Bus Transceiver (3-State)
Am2917A	Quad Bus Transceiver (3-State)
Am54/74123	Dual One-Shot
Am54/74221	Dual One-Shot
Am54LS/74LS240	Octal Bus Inverter
Am54LS/74LS241	Octal Bus Buffer
Am54LS/74LS242	Quad Bus Transceiver
Am54LS/74LS243	Quad Bus Transceiver
Am54LS/74LS244	Octal Bus Buffer
Am54S/74S240	Octal Bus Inverter
Am54S/74S241	Octal Bus Buffer
****Am54S/74S242	Quad Bus Transceiver
****Am54S74S243	Quad Bus Transceiver
Am54S/74S244	Octal Bus Buffer
Am55/75107B	Dual Differential Line Receiver
Am55/75108B	Dual Differential Line Receiver
Am55/75109	Dual Differential Line Driver
Am55/75110	Dual Differential Line Driver
Am55/75234	Dual Sense Amplifier, ±4mV Threshold
Am55/75325	Core Memory Driver, 600mA Output
Am75207	Dual MOS Sense Amp/Line Receiver
Am75208	Dual Sense Amp/Line Receiver
***Am8304	Octal Bus Transceiver
***Am71/81LS95	Octal Non-Inv. Buffer
***Am71/81LS96	Octal Inv. Buffer
***Am71/81LS97	Octal Non-Inv. Buffer
***Am71/81LS98	Octal Inv. Buffer
Am78/8820	Dual Differential Line Receiver
Am78/8820A	Dual Differential Line Receiver
Am78/8830	Dual Differential Line Receiver
Am78/8831	TS Line Driver
Am78/8832	TS Line Driver
Am78/8838	Quad Bus Transceiver
Am8T26	Schottky Quad TS Bus Transceiver
Am8T26A	Schottky Quad TS Bus Transceiver
Am8T28	Schottky Quad TS Bus Transceiver
Am8212	8-Bit Input/Output Port
Am8216	4-Bit Bi-directional Bus Driver
Am8224	Clock Generator and Driver
Am8226	4-Bit Bi-directional Bus Driver
Am8228	System Controller and Bus Driver
Am8238	System Controller and Bus Driver
Am9600	One-Shot
Am9601	One-Shot
Am9602	Dual One-Shot
Am96L02	Low-Power, Dual One-Shot
Am9614	Dual Line Driver
Am9615	Dual Differential Line Receiver
Am9616	Triple EIA Line Driver
Am9617	Triple EIA Line Receiver
Am9620	Dual Differential Line Receiver
Am9621	Dual Differential Line Driver

BIPOLAR MICROPROCESSORS

Am2901	4-Bit Bipolar Microprocessor Slice
Am2901A	4-Bit Bipolar Microprocessor Slice
Am2901B	4-Bit Bipolar Microprocessor Slice
Am2902A	Look-Ahead Carry Generator
Am2903	4-Bit Bipolar Microprocessor Slice
Am2904	Status and Shift Control Circuit
Am2905	Quad Two-Input OC Bus Transceiver, TS Receiver
Am2906	Quad Two-Input OC Bus Transceiver, Parity
Am2907	Quad OC Bus Transceiver, Parity, TS Receiver
Am2908	Quad Bus Transceiver, DEC UNIBUS® Compatible
Am2909	Microprogram Sequencer
***Am2909A	High-Speed Am2909
Am2910	Microprogram Controller
Am2911	Microprogram Sequencer
**Am2911A	High-Speed Am2911
Am2913	Expander for Am2914
Am2914	Priority Interrupt Circuit
Am2915A	TS Bus Transceiver
Am2916A	TS Bus Transceiver
Am2917A	TS Bus Transceiver
Am2918	4-Bit Register with Standard and TS Outputs
Am29LS18	Low-Power 2918
Am2919	4-Bit Register with Two TS Output Ports
Am2920	8-Bit TS Register with Clear and Enable
Am2921	One-of-Eight Decoder/Mask Generator
Am2922	Eight-Input MUX with Polarity
***Am2925	Clock Generator
Am2930	Program Control Unit
**Am2932	Program Control Unit
Am2940	DMA Word and Address Counter
Am2942	Counter/Timer
Am2950/51	I/O Port
***Am2960	Error Detection and Correction
Am29700	16 x 4-Bit RAM, OC, Non-Inverting
Am29701	16 x 4-Bit RAM, TS, Non-Inverting
Am29702	16 x 4-Bit RAM, OC, Inverting
Am29703	16 x 4-Bit RAM, TS, Inverting
Am29704	16 x 4-Bit RAM, OC, Two-Port
Am29705	16 x 4-Bit RAM, TS, Two-Port
Am29720	256 x 1-Bit RAM, OC
Am29721	256 x 1-Bit RAM, TS
Am29750A	32 x 8-Bit PROM, OC
Am29751A	32 x 8-Bit PROM, TS
Am29760A	256 x 4-Bit PROM, OC
Am29761A	256 x 4-Bit PROM, TS
Am29770	512 x 4-Bit PROM, OC
Am29771	512 x 4-Bit PROM, TS
Am29772	512 x 8-Bit PROM, OC
Am29773	512 x 8-Bit PROM, TS
Am29774	512 x 8-Bit PROM w/Pipeline Registers, OC
Am29775	512 x 8-Bit PROM w/Pipeline Registers, TS
Am29780	1024 x 4-Bit PROM, OC
Am29781	1024 x 4-Bit PROM, TS
Am29803A	Controller for Am2909
Am29811A	Controller for Am2911
Am29882	1k x 8-Bit ROM, OC
Am29883	1k x 8-Bit ROM, TS

BIPOLAR MEMORY CIRCUITS

Am27LS00A	256 x 1-Bit RAM, TS, 35ns
Am27LS01A	256 x 1-Bit RAM, OC, 35ns
Am27LS00	256 x 1-Bit RAM, TS, 45ns
Am27LS01	256 x 1-Bit RAM, OC, 45ns
Am27S02	16 x 4-Bit RAM, OC, 35ns
Am27S03	16 x 4-Bit RAM, TS, 35ns
Am27LS02	16 x 4-Bit RAM, OC, 55ns, 35mA
Am27LS03	16 x 4-Bit RAM, TS, 55ns, 35mA
Am27S02A	16 x 4-Bit RAM, OC, 25ns
Am27S03A	16 x 4-Bit RAM, TS, 25ns
Am27S06	16 x 4-Bit RAM, OC, 25ns
Am27S07	16 x 4-Bit RAM, TS, 25ns
Am27LS06	16 x 4-Bit RAM, OC, 55ns, 35mA
Am27LS07	16 x 4-Bit RAM, TS, 55ns, 35mA
Am27S12	512 x 4-Bit PROM, OC, 50ns
Am27S13	512 x 4-Bit PROM, TS, 50ns
Am27S15	512 x 8-Bit PROM/Output Latches, TS, 60ns
Am27S18	32 x 8-Bit PROM, OC, 40ns
Am27S19	32 x 8-Bit PROM, TS, 40ns
Am27S20	256 x 4-Bit PROM, OC, 45ns
Am27S21	256 x 4-Bit PROM, TS, 45ns
Am27S26	512 x 8-Bit PROM/Output Registers OC, 50ns
Am27S27	512 x 8-Bit PROM/Output Registers, TS, 50ns
Am27S28	512 x 8-Bit PROM, 20 Pins, OC, 55ns
Am27S29	512 x 8-Bit PROM, 20 Pins, TS, 55ns
Am27S30	512 x 8-Bit PROM, 24 Pins, OC, 55ns
Am27S31	512 x 8-Bit PROM, 24 Pins, TS, 55ns
**Am27S32	1024 x 4-Bit PROM, OC, 55ns
**Am27S33	1024 x 4-Bit PROM, TS, 55ns
Am27S80	1024 x 8-Bit ROM, OC, 175ns
Am27S81	1024 x 8-Bit ROM, TS, 175ns

Am27S82	1024 x 8-Bit ROM, OC, 175ns
Am27S83	1024 x 8-Bit ROM, TS, 175ns
***Am27S180	1024 x 8-Bit PROM, 24 Pins, OC, 60ns
***Am27S181	1024 x 8-Bit PROM, 24 Pins, TS, 60ns
Am3101	16 x 4-Bit RAM, OC, 60ns
Am3101-1	16 x 4-Bit RAM, OC, 35ns
Am3101A	16 x 4-Bit RAM, OC, 35ns
Am31L01	16 x 4-Bit RAM, OC, 110ns, 35mA
Am93411	256 x 1-Bit RAM, OC, 55ns
Am93421	256 x 1-Bit RAM, TS, 55ns
Am93411A	256 x 1-Bit RAM, OC, 45ns
Am93421A	256 x 1-Bit RAM, TS, 45ns
Am54/7489	16 x 4-Bit RAM, OC, 60ns
Am54/7489-1	16 x 4-Bit RAM, OC, 35ns
Am54/74S189	16 x 4-Bit RAM, TS, 35ns
Am54/74S289	16 x 4-Bit RAM, OC, 35ns
Am54/74S201	256 x 1-Bit RAM, TS, 65ns
Am54/74S301	256 x 1-Bit RAM, OC, 65ns
Am75/8599	16 x 4-Bit RAM, TS, 60ns
Am93403	16 x 4-Bit RAM, OC, 60ns

LINEAR INTEGRATED CIRCUITS

Am685	High-Speed ECL Comparator
Am686	High-Speed TTL Comparator
Am687	Dual High-Speed ECL Comparator
Am1500	Dual 111 Comparator
Am1501	Dual 101A Op Amp
Am1508	8-Bit D to A Converter
LM101	General-Purpose Op Amp
LM101A	General-Purpose Op Amp
LM102	High-Speed Voltage Follower
LM105	Voltage Regulator
LM106	High-Speed Voltage Comparator
LM107	Compensated Op Amp
LM108	Instrumentation Op Amp
LM108A	Instrumentation Op Amp
LM110	High-Speed Voltage Follower
LM111	Precision Voltage Comparator
LM112	Compensated High-Performance Op Amp
LM118	High-Speed Op Amp
LM119	Dual High-Speed Comparator
LM124	Quad Operational Amplifier
LM139	Quad Comparator
LM148	Quad Compensated Op Amp
LM149	Quad Op Amp
LF155	FET Input Op Amp
LF156	FET Input Op Amp
LF157	FET Input Op Amp
LF198	Sample Hold
LM216	Compensated High-Performance Op Amp
LM216A	Compensated High-Performance Op Amp
Am592	Video Amplifier
Am715	High-Speed Op Amp
Am723	Voltage Regulator
SSS725	High-Performance Instrumentation Op Amp
Am725	Instrumentation Op Amp
Am733	Video Amp
SSS741	High-Performance Compensated Op Amp
Am741	Compensated Op Amp
SSS747	High Performance Dual Compensated Op Amp
Am747	Dual Compensated Op Amp
Am748	General-Purpose Op Amp
LH2111	Dual 111 Comparator
LH2101A	Dual 101A Op Amp
DAC-08	8-Bit D to A Converter
**Am6012	12-Bit High Speed Multiplying D to A Converter
Am6070	8-Bit μ-Law Industrial Companding D to A Converter
Am6071	8-Bit A-Law Industrial Companding D to A Converter
Am6072	8-Bit μ-Law Companding D to A Converter
Am6073	8-Bit A-Law Companding D to A Converter
Am6080	8-Bit μ-Processor Compatible D to A Converter
Am6081	8-Bit μ-Processor Compatible D to A Converter
****Am6180	Bus Compatible A to D Converter, 8-Bit
***Am6688	4-Bit High Speed Quantizer (A to D Converter)
****Am6689	8-Bit High Speed D to A Converter
****Am6300	Power Control Subsystem

JAN LINEAR

JM38510/10101BGC/A	JAN 741 Op Amp
JM38510/10102BCB/A	JAN 747 Op Amp
JM38510/10102BIC	JAN 747 Op Amp
JM38510/10103BGA	JAN 101A Op Amp
JM38510/10103BGC	JAN 101A Op Amp
JM38510/10201BIC	JAN 723 Regulator
JM38510/10201BCB	JAN 723 Regulator
JM38510/10304BGC/A	JAN 111 Comparator
***JM38510/10304BCB	JAN 111 Comparator
**JM38510/10105BEA	JAN 2101 Op Amp

BIPOLAR LOGIC CIRCUITS HIGH-PERFORMANCE LOW-POWER SCHOTTKY TTL/MSI • LSI

Am25LS07	6-Bit Register with Common Clock Enable
Am25LS08	4-Bit Register with Common Clock Enable
Am25LS09	4-Bit Register with Two-Input Multiplexer on Inputs
Am25LS14	8 x 1 Serial/Parallel Two's Complement Multiplier
Am25LS15	Quad Serial Adder/Subtractor
Am25LS22	8-Bit Serial/Parallel Register
Am25LS23	8-Bit Shift/Storage Register
Am25LS138	1-of-8 Decoder/Demultiplexer
Am25LS139	Dual 1-of-4 Decoder/Demultiplexer
Am25LS148	Priority Encoder
Am25LS151	Eight-Input Multiplexer
Am25LS153	Dual Four-Input Multiplexer
Am25LS157	Quad Two-Input Multiplexer, Non-inverting
Am25LS158	Quad Two-Input Multiplexer, Inverting
Am25LS160A	Synchronous BCD Decade Counter, Asynchronous Clear
Am25LS161A	Synchronous 4-Bit Binary Counter, Asynchronous Clear
Am25LS162A	Synchronous BCD Decade Counter, Synchronous Clear
Am25LS163A	Synchronous 4-Bit Binary Counter, Synchronous Clear
Am25LS164	8-Bit Serial In/Parallel Out Shift Register
Am25LS168A	Synchronous 4-Bit Up/Down Counter
Am25LS169A	Synchronous 4-Bit Up/Down Counter
Am25LS174	6-Bit Register with Common Clear
Am25LS175	Quad Register with Common Clear
Am25LS181	4-Bit ALU/Function Generator
Am25LS190	Synchronous BCD Decade Up/Down Counter, Single Clock
Am25LS191	Synchronous 4-Bit Binary Up/Down Counter, Single Clock
Am25LS192	Synchronous BCD Decade Up/Down Counter
Am25LS193	Synchronous 4-Bit Binary Up/Down Counter
Am25LS194A	4-Bit Register; Shift Right, Left or Parallel Load
Am25LS195A	4-Bit Register; Shift Right or Parallel Load
Am25LS240	Octal Bus Inverter
Am25LS241	Octal Bus Buffer
Am25LS242	Octal Bus Transceiver
Am25LS243	Octal Bus Transceiver
Am25LS244	Octal Buffer
Am25LS251	TS 8-Input Multiplexer
Am25LS253	TS Dual Four-Input Multiplexer
Am25LS257	TS Quad Two-Input Multiplexer, Non-Inverting
Am25LS258	TS Quad Two-Input Multiplexer, Inverting
Am25LS273	Octal D-Type Register
Am25LS299	8-Bit Universal Shift/Storage Register
Am25LS373	Octal Transparent Latch, TS
Am25LS374	Octal D-Type Register, TS
Am25LS377	Octal D-Type Register
Am25LS378	6-Bit Register (Am25LS07)
Am25LS379	4-Bit Register (Am25LS08)
Am25LS381	ALU/Function Generator (20-Pin)
Am25LS399	Quad Two-Input 4-Bit Register (Am25LS09)
Am25LS2513	Priority Encoder, Three-State
Am25LS2516	8 x 8 Multiplier/Accumulator
Am25LS2617	4-Bit ALU/Function Generator (20-Pin)
Am25LS2518	4-Bit Register, Standard and TS
Am25LS2519	4-Bit Register, Standard and TS
Am25LS2520	Octal D-Type Flip-Flop, TS

Am25LS2521	8-Bit Comparator
***Am25LS2525	System Timing Element
Am25LS2535	8-Bit Multiplexer with Storage
Am25LS2536	8-Bit Decoder with Storage
Am25LS2537	1-of-10 TS Decoder
Am25LS2538	1-of-8 TS Decoder
Am25LS2539	Dual 1-of-4 TS Decoder
Am25LS2568	4-Bit, Up/Down Counter, TS
Am25LS2569	4-Bit, Up/Down Counter, TS

STANDARD LOW-POWER SCHOTTKY TTL/MSI • LSI

Am54LS/74LS138	1-of-8 Decoder/Demultiplexer
Am54LS/74LS139	Dual 1-of-4 Decoder/Demultiplexer
Am54LS/74LS148	Priority Encoder
Am54LS/74LS151	Eight-Input Multiplexer
Am54LS/74LS153	Dual Four-Input Multiplexer
Am54LS/74LS157	Quad Two-Input Multiplexer, Non-Inverting
Am54LS/74LS158	Quad Two-Input Multiplexer, Inverting
Am54LS/74LS160	Synchronous BCD Decade Counter, Asynchronous Clear
Am54LS/74LS160A	Synchronous BCD Decade Counter, Asynchronous Clear
Am54LS/74LS161	Synchronous 4-Bit Binary Counter, Asynchronous Clear
Am54LS/74LS161A	Synchronous 4-Bit Binary Counter, Asynchronous Clear
Am54LS/74LS162	Synchronous BCD Decade Counter, Synchronous Clear
Am54LS/74LS162A	Synchronous BCD Decade Counter, Synchronous Clear
Am54LS/74LS163	Synchronous 4-Bit Binary Counter, Synchronous Clear
Am54LS/74LS163A	Synchronous 4-Bit Binary Counter, Synchronous Clear
Am54LS/74LS164	8-Bit Serial In/Parallel Out Shift Register
Am54LS/74LS168A	Synchronous 4-Bit Up/Down Counter
Am54LS/74LS169A	Synchronous 4-Bit Up/Down Counter
Am54LS/74LS174	6-Bit Register with Common Clear
Am54LS/74LS175	Quad Register with Common Clear
Am54LS/74LS181	4-Bit ALU/Function Generator
Am54LS/74LS190	Synchronous BCD Decade Up/Down Counter, Single Clock
Am54LS/74LS191	Synchronous 4-Bit Binary Up/Down Counter, Single Clock
Am54LS/74LS192	Synchronous BCD Decade Up/Down Counter
Am54LS/74LS193	Synchronous 4-Bit Binary Up/Down Counter
Am54LS/74LS194A	4-Bit Register; Shift Right, Left or Parallel Load
Am54LS/74LS195A	4-Bit Register; Shift Right or Parallel Load
Am54LS/74LS240	Octal Bus Driver, Inverting
Am54LS/74LS241	Octal Bus Driver, Non-Inverting
Am54LS/74LS242	Octal Bus Transceiver
Am54LS/74LS243	Octal Bus Transceiver
Am54LS/74LS244	Octal Buffer, TS
Am54LS/74LS251	TS Eight-Input Multiplexer
Am54LS/74LS253	TS Dual Four-Input Multiplexer
Am54LS/74LS257	TS Quad Two-Input Multiplexer, Non-Inverting
Am54LS/74LS258	TS Quad Two-Input Multiplexer, Inverting
Am54LS/74LS273	Octal D-Type Register
Am54LS/74LS299	8-Bit Universal Shift/Storage Register
Am54LS/74LS322	See Am25LS22
Am54LS/74LS323	See Am25LS23
Am54LS/74LS373	Octal Transparent Latch
Am54LS/74LS374	Octal D-Type Flip-Flop
Am54LS/74LS377	Octal D-Type Flip-Flop
Am54LS/74LS378	See Am25LS07
Am54LS/74LS379	See Am25LS08
Am54LS/74LS381	ALU/Function Generator
Am54LS/74LS384	See Am25LS14
Am54LS/74LS385	See Am25LS15
Am54LS/74LS388	See Am25LS2518
Am54LS/74LS399	See Am25LS09
Am54LS/74LS424	See Am8224
Am54LS/74LS668	See Am54LS/74LS168A
Am54LS/74LS669	See Am54LS/74LS169A

HIGH-SPEED SCHOTTKY TTL/MSI

Am25S05	4 X 2-Bit Two's Complement Multiplier
Am25S07	6-Bit Register with Clock Enable
Am25S08	4-Bit Register with Clock Enable
Am25S09	4-Bit Register with Two-Input Multiplexer on Inputs
Am25S10	4-Bit, Four-Way Shifter
Am25S18	4-Bit Register with Standard and TS Outputs
Am54S/74S138	1-of-8 Decoder/Demultiplexer
Am54S/74S139	Dual 1-of-4 Decoder/Demultiplexer
Am54S/74S151	Eight-Input Multiplexer
Am54S/74S153	Dual Four-Input Multiplexer
Am54S/74S157	Quad Two-Input Multiplexer, Non-Inverting
Am54S/74S158	Quad Two-Input Multiplexer, Inverting
Am54S/74S160	Synchronous BCD Decade Counter, Asynchronous Clear
Am54S/74S161	Synchronous 4-Bit Binary Counter, Asynchronous Clear
Am54S/74S174	6-Bit Register with Clear
Am54S/74S175	Quad Register with Clear
Am54S/74S181	4-Bit ALU/Function Generator
Am54S/74S182	Carry Look-Ahead Generator
Am54S/74S194	4-Bit Register; Shift Right, Left or Parallel Load
Am54S/74S195	4-Bit Register; Shift Right or Parallel Load
Am54S/74S240	Octal Bus Driver, Inverting
Am54S/74S241	Octal Buffer, Non-inverting
Am54S/74S242	Octal Bus Transceiver, Inverting
Am54S/74S243	Octal Bus Transceiver, Non-inverting
Am54S/74S244	Octal Buffer, Inverting
Am54S/74S251	TS Eight-Input Multiplexer
Am54S/74S253	TS Dual Four-Input Multiplexer
Am54S/74S257	TS Quad Two-Input Multiplexer, Non-Inverting
Am54S/74S258	TS Quad Two-Input Multiplexer, Inverting
***Am54S/74S373	Octal Transparent Latch, TS
***Am54S/74S374	Octal D-Type Register, TS
Am54S/74S412	See Am8212
Am82S62	Nine-Input Parity Checker/Generator
Am93S10	Synchronous BCD Decade Counter, Asynchronous Clear
Am93S16	Synchronous 4-Bit Binary Counter, Asynchronous Clear
Am93S21	Dual 1-of-4 Decoder/Demultiplexer
Am93S22	Quad Two-Input Multiplexer
Am93S48	Twelve-Input/Parity Generator/Checker

STANDARD LOW-POWER TTL/MSI

Am25L02	8-Bit Successive Approximation Register with Serial Data Output
Am25L03	8-Bit Successive Approximation Register with Enable Input
Am25L04	12-Bit Successive Approximation Register
Am25L05	4 X 2-Bit Two's Complement Multiplier
Am25L06	4-Bit ALU with Latch
Am93L00	4-Bit Shift Register
Am93L01	1-of-10 Decoder/Demultiplexer
Am93L08	Dual 4-Bit Latch
Am93L09	Dual Four-Input Multiplexer
Am93L10	Synchronous BCD Decade Counter, Asynchronous Clear
Am93L11	1-of-16 Decoder/Demultiplexer
Am93L12	Eight-Input Multiplexer
Am93L14	4-Bit Latch
Am93L16	Synchronous 4-Bit Binary Counter, Asynchronous Clear
Am93L18	Eight-Input Priority Encoder
Am93L21	Dual 1-of-4 Decoder/Demultiplexer
Am93L22	Quad Two-Input Multiplexer
Am93L24	5-Bit Comparator
Am93L28	Dual 8-Shift Register
Am93L34	8-Bit Addressable Latch
Am93L38	8-Bit Multiple Port Register
Am93L40	4-Bit ALU, Carry Look-Ahead Generator
Am93L41	4-Bit ALU/Function Generator
Am93L60	Synchronous BCD Decade Up/Down Counter, Two Clocks
Am93L66	Synchronous 4-Bit Binary Up/Down Counter, Two Clocks

STANDARD TTL/MSI

Am2501	4-Bit Binary Synchronous Up/Down Counter
Am2502	8-Bit Successive Approximation Register with Serial Data Output
Am2503	8-Bit Successive Approximation Register with Enable Input
Am2504	12-Bit Successive Approximation Register
Am2505	4 X 2-Bit Two's Complement Multiplier
Am2506	4-Bit ALU with Latch
Am54/74123	Dual One-Shot
Am54/74153	Dual Four-Input Multiplexer
Am54/74154	1-of-16 Decoder/Demultiplexer
Am54/74157	Quad Two-Input Multiplexer, Non-Inverting
Am54/74160	Synchronous BCD Decade Counter, Asynchronous Clear
Am54/74161	Synchronous 4-Bit Binary Counter, Asynchronous Clear
Am54/74162	Synchronous BCD Decade Counter, Synchronous Clear
Am54/74163	Synchronous 4-Bit Binary Counter, Synchronous Clear
Am54/74164	8-Bit Serial In/Parallel Out Shift Register
Am54/74174	6-Bit Register with Clear
Am54/74175	Quad Register with Clear
Am54/74181	4-Bit ALU/Function Generator
Am54/74182	Look-Ahead Carry Generator
Am54/74192	Synchronous BCD Decade Up/Down Counter, Two Clocks
Am54/74193	Synchronous 4-Bit Binary Up/Down Counter, Two Clocks
Am54/74194	4-Bit Register; Shift Right, Left or Parallel Load
Am54/74195	4-Bit Register; Shift Right or Parallel Load
Am54/74221	Dual One-Shot with Schmitt Trigger
Am9300	4-Bit Shift Register
Am9301	1-of-10 Decoder/Demultiplexer
Am9304	Dual Full Adder
Am9306	Synchronous BCD Decade Up/Down Counter
Am9308	Dual 4-Bit Latch
Am9309	Dual Four-Input Multiplexer
Am9310	Synchronous BCD Decade Counter, Asynchronous Clear
Am9311	1-of-16 Decoder/Demultiplexer
Am9312	Eight-Input Multiplexer
Am9314	4-Bit Latch
Am9316	Synchronous 4-Bit Binary Counter, Asynchronous Clear
Am9318	Eight-Input Priority Encoder
Am9321	Dual 1-of-4 Decoder/Demultiplexer
Am9322	Quad Two-Input Multiplexer
Am9324	5-Bit Comparator
Am9328	Dual 8-Bit Shift Register
Am9334	8-Bit Addressable Latch
Am9338	8-Bit Multiple Port Register
Am9340	4-Bit ALU, Look-Ahead Carry Generator
Am9341	4-Bit ALU/Function Generator
Am9342	Look-Ahead Carry Generator
Am9360	Synchronous BCD Decade Up/Down Counter
Am9366	Synchronous 4-Bit Binary Up/Down Counter

**Available 2nd Qtr. 1979
***Available 3rd Qtr. 1979
****Available 4th Qtr. 1979

Microprocessors

Am2903
The Superslice™

DISTINCTIVE CHARACTERISTICS

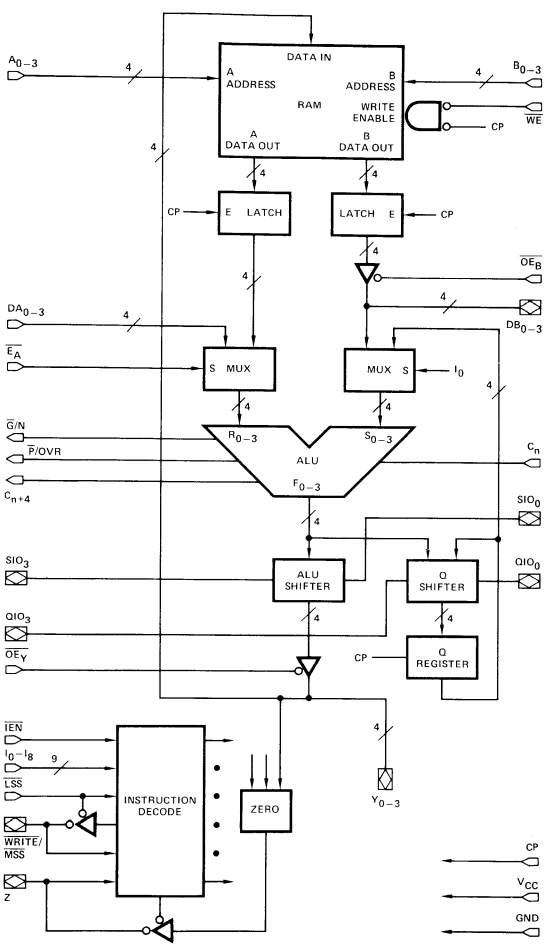
- Expandable Register File–
  Like the Am2901A, the Am2903 contains 16 internal working registers arranged in a two-address architecture. But the Am2903 includes the necessary "hooks" to expand the register file externally to any number of registers.
- Built-in Multiplication Logic–
  Performing multiplication with the Am2901A requires a few external gates--these gates are contained on-chip in the Am2903. Three special instructions are used for unsigned multiplication, two's complement multiplication, and the last cycle of a two's complement multiplication.
- Built-in Division Logic–
  The Am2903 contains all logic and interconnects for execution of a non-restoring, multiple-length division with correction of the quotient.
- Built-in Normalization Logic–
  The Am2903 can simultaneously shift the Q Register and count in a working register. Thus, the mantissa and exponent of a floating point number can be developed using a single microcycle per shift. Status flags indicate when the operaton is complete.
- Built-in Parity Generation Circuitry–
  The Am2903 can supply parity across the entire ALU output for use in error detection and CRC code generation.
- Built-in Sign Extension Circuitry–
  To facilitate operation on different length two's complement numbers, the Am2903 provides the capability to extend the sign at any slice boundary.

TABLE OF CONTENTS

GENERAL DESCRIPTION

The Am2903 is a four-bit expandable bipolar microprocessor slice. The Am2903 performs all functions performed by the industry standard Am2901A and, in addition, provides a number of significant enhancements that are especially useful in arithmetic-oriented processors. Infinitely expandable memory and three-port, three-address architecture are provided by the Am2903. In addition to its complete arithmetic and logic instruction set, the Am2903 provides a special set of instructions which facilitate the implementation of multiplication, division, normalization, and other previously time-consuming operations. The Am2903 is supplied in a 48 pin dual in-line package.

BLOCK DIAGRAM



Some Questions and Answers About the Am2903:

Why did AMD do a new slice?

Although the Am2901 is a very versatile product, it does have a few limitations. In particular, there is no easy way to expand the internal 16-word register file. This is a drawback in machines requiring more than 16 registers, or machines which need to switch rapidly between foreground and background operating levels. The Am2903 was designed to provide for easy file expansion with no loss of flexibility or speed.

Why is the 2903 only four-bits wide?

An eight-bit slice is within the ability of the technology. But it would be significantly slower than a four-bit device, because of power limitations within the package. An eight-bit part could not dissipate much more power than a four-bit part, so the average power per gate would be reduced by around 40%, significantly affecting speed.

What does the 2903 do that the 2901 can't do?

The only 2903 feature which can't be done with the 2901 is the register file expansion and an associated feature, three-address operation. The 2901 register file cannot be expanded without sacrificing the two-address architecture and shifting capability. External registers added to the 2903, on the other hand, are indistinguishable from the internal registers; moreover, the 2903 allows the operation A + B→C, where A, B, and C are all different registers. This isn't possible in the 2901.

What does the 2901 do that the 2903 can't do?

Nothing.

Can the 2901 do all the special functions like multiply and divide?

Yes, but the 2901 requires either additional external hardware or additional microinstructions or both to do the single cycle functions built-in to the 2903. For example, multiplication in either part uses a conditional add and shift algorithm. The LSB of the multiplier is tested and if it is a 1, the multiplicand is added to the partial product and the whole thing is shifted down one place. If it is a 0, the addition does not occur. In the 2901, extra hardware is needed to maintain the sign of the partial product during the down shift. Also, either there must be hardware to modify the instruction based on the LSB of multiplier or there must be two microinstructions, one to test the LSB and one to add. In the 2903, all this happens automatically on one instruction.

How does the 2903 compare with the 74S481?

Both parts perform special functions such as multiply and divide. Both use low-power Schottky technology. The most fundamental difference between the two parts is the approach to working registers. The S481 follows the TI990 minicomputer architecture, which has no hardware registers associated with the CPU (except accumulators), but rather puts the working registers in main memory. The advantage of this approach is that an "unlimited" number of registers are available and the software can set up any number of banks of registers for context switching. The disadvantage is that, since the registers are in memory, they are no faster than memory. The speed advantage of hardware working registers disappears. The 2903, on the other hand, is designed to use many fast registers intimately tied to the CPU in a multiple address architecture. This provides very rapid operations among these working registers, even though main memory consists of slower, less expensive RAM's. The result is more throughput for fewer dollars.

What packages are used for the 2903?

The 2903 is initially available in a 48-lead side-brazed hermetic DIP on 0.6 inch centers. It is just like the 2901 package, but a little bit longer. A plastic package and a hermetic flat pack are being developed. The Am2903 will not be offered in a "quad-in-line" package. Sockets for the 48-lead DIP are available from:

Vendor:	Textool Products, Inc. 1410 W. Pioneer Drive Irving, Texas 75061	Circuit Assembly Corp. 3169 Red Hill Ave. Costa Mesa, Ca. 92626	Aries Electronics, Inc. P.O. Box 231 Frenchtown, NJ 08825
Phone:	214-259-2676	714-540-5490	201-996-4096
Part No.:	248-0337-51-0605	CA-24SEL-10375WW (Gold Plate) CA-24SEL-T375WW (Tin Plate)	48-6503-32
Description:	Zip DIP (Zero Insertion Force Socket)	These are end-to-end stackable 24-lead sockets with wire-wrap leads. Put two together to make one 48-lead socket.	48-lead wire-wrap socket. Tin plated.

ARCHITECTURE OF THE Am2903

The Am2903 is a high-performance, cascadable, four-bit bipolar microprocessor slice designed for use in CPU's, peripheral controllers, microprogrammable machines, and numerous other applications. The microinstruction flexibility of the Am2903 allows the efficient emulation of almost any digital computing machine. The nine-bit microinstruction selects the ALU sources, function, and destination. The Am2903 is cascadable with full lookahead or ripple carry, has three-state outputs, and provides various ALU status flag outputs. Advanced Low-Power Schottky processing is used to fabricate this 48-pin LSI circuit.

All data paths within the device are four bits wide. As shown in the block diagram, the device consists of a 16-word by 4-bit, two-port RAM with latches on both output ports, a high-performance ALU and shifter, a multi-purpose Q Register with shifter input, and a nine-bit instruction decoder.

Two-Port RAM

Any two RAM words addressed at the A and B address ports can be read simultaneously at the respective RAM A and B output ports. Identical data appear at the two output ports when the same address is applied to both address ports. The latches at the RAM output ports are transparent when the clock input, CP, is HIGH and they hold the RAM output data when CP is LOW. Under control of the $\overline{OE}_B$ three-state output enable, RAM data can be read directly at the Am2903 DB I/O port.

External data at the Am2903 Y I/O port can be written directly into the RAM, or ALU shifter output data can be enabled onto the Y I/O port and entered into the RAM. Data is written into the RAM at the B address when the write enable input, $\overline{WE}$, is LOW and the clock input, CP, is LOW.

Arithmetic Logic Unit

The Am2903 high-performance ALU can perform seven arithmetic and nine logic operations on two 4-bit operands. Multiplexers at the ALU inputs provide the capability to select various pairs of ALU source operands. The $\overline{E}_A$ input selects either the DA external data input or RAM output port A for use as one ALU operand and the $\overline{OE}_B$ and I_0 inputs select RAM output port B, DB external data input, or the Q Register content for use as the second ALU operand. Also, during some ALU operations, zeroes are forced at the ALU operand inputs. Thus, the Am2903 ALU can operate on data from two external sources, from an internal and external source, or from two internal sources. Table I shows all possible pairs of ALU source operands as a function of the $\overline{E}_A$, $\overline{OE}_B$, and I_0 inputs.

When instruction bits I_4, I_3, I_2, I_1, and I_0 are LOW, the Am2903 executes special functions. Table 4 defines these special functions and the operation which the ALU performs for each. When the Am2903 executes instructions other than the nine special functions, the ALU operation is determined by instruction bits I_4, I_3, I_2, and I_1. Table 2 defines the ALU operation as a function of these four instruction bits.

Am2903's may be cascaded in either a ripple carry or lookahead carry fashion. When a number of Am2903's are cascaded, each slice must be programmed to be a most significant slice (MSS), intermediate slice (IS), or least significant slice (LSS) of the array. The carry generate, $\overline{G}$, and carry propagate, $\overline{P}$, signals required for a lookahead carry scheme are generated by the Am2903 and are available as outputs of the least significant and intermediate slices.

The Am2903 also generates a carry-out signal, C_{n+4}, which is generally available as an output of each slice. Both the carry-in, C_n, and carry-out, C_{n+4}, signals are active HIGH. The ALU generates two other status outputs. These are negative, N, and overflow, OVR. The N output is generally the most significant (sign) bit of the ALU output and can be used to determine positive or negative results. The OVR output indicates that the arithmetic operation being performed exceeds the available two's complement number range. The N and OVR signals are available as outputs of the most significant slice. Thus, the multi-purpose $\overline{G}$/N and $\overline{P}$/OVR outputs indicate $\overline{G}$ and $\overline{P}$ at the least significant and intermediate slices, and sign and overflow at the most significant slice. To some extent, the meaning of the C_{n+4}, $\overline{P}$/OVR, and $\overline{G}$/N signals vary with the ALU function being performed. Refer to Table 5 for an exact definition of these four signals as a function of the Am2903 instruction.

TABLE 1. ALU OPERAND SOURCES

$\overline{E}_A$	I_0	$\overline{OE}_B$	ALU Operand R	ALU Operand S
L	L	L	RAM Output A	RAM Output B
L	L	H	RAM Output A	DB_{0-3}
L	H	X	RAM Output A	Q Register
H	L	L	DA_{0-3}	RAM Output B
H	L	H	DA_{0-3}	DB_{0-3}
H	H	X	DA_{0-3}	Q Register

L = LOW H = HIGH X = Don't Care

TABLE 2. ALU FUNCTIONS

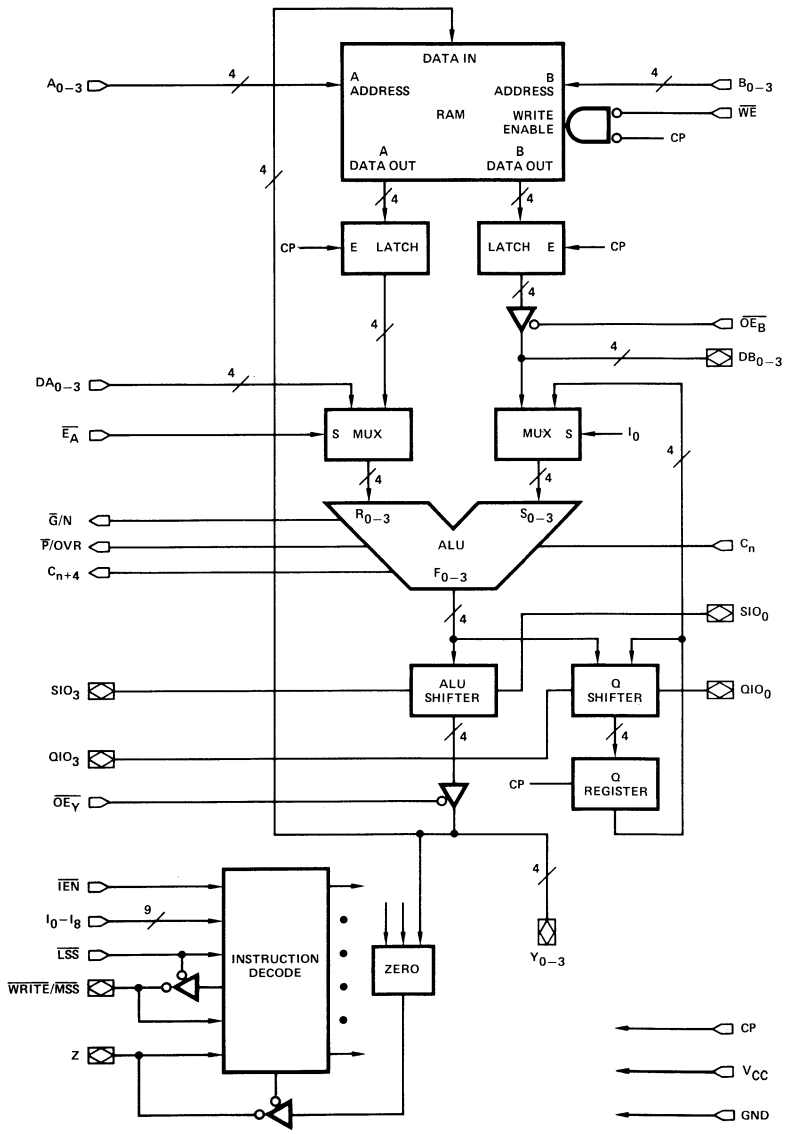
I_4	I_3	I_2	I_1	Hex Code	ALU Functions	
L	L	L	L	0	I_0 = L	Special Functions
					I_0 = H	F_i = HIGH
L	L	L	H	1	F = S Minus R Minus 1 Plus C_n	
L	L	H	L	2	F = R Minus S Minus 1 Plus C_n	
L	L	H	H	3	F = R Plus S Plus C_n	
L	H	L	L	4	F = S Plus C_n	
L	H	L	H	5	F = $\overline{S}$ Plus C_n	
L	H	H	L	6	F = R Plus C_n	
L	H	H	H	7	F = $\overline{R}$ Plus C_n	
H	L	L	L	8	F_i = LOW	
H	L	L	H	9	$F_i = \overline{R}_i$ AND S_i	
H	L	H	L	A	$F_i = R_i$ EXCLUSIVE NOR S_i	
H	L	H	H	B	$F_i = R_i$ EXCLUSIVE OR S_i	
H	H	L	L	C	$F_i = R_i$ AND S_i	
H	H	L	H	D	$F_i = R_i$ NOR S_i	
H	H	H	L	E	$F_i = R_i$ NAND S_i	
H	H	H	H	F	$F_i = R_i$ OR S_i	

L = LOW H = HIGH i = 0 to 3

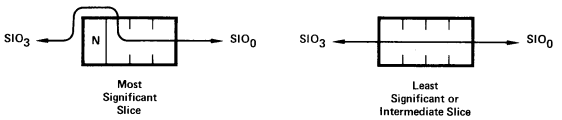
ALU Shifter

Under instruction control, the ALU shifter passes the ALU output (F) non-shifted, shifts it up one bit position (2F), or shifts it down one bit position (F/2). Both arithmetic and logical shift operations are possible. An arithmetic shift operation shifts data around the most significant (sign) bit position of the most significant slice, and a logical shift operation shifts data through this bit position (see Figure A). SIO_0 and SIO_3 are bidirectional serial shift inputs/outputs. During a shift-up operation, SIO_0 is generally a serial shift input and SIO_3 a serial shift output. During a shift-down operation, SIO_3 is generally a serial shift input and SIO_0 a serial shift output.

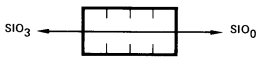
BLOCK DIAGRAM



MPR-030



Am2903 Arithmetic Shift Path



Am2903 Logical Shift Path

Figure A. MPR-031

To some extent, the meaning of the SIO_0 and SIO_3 signals is instruction dependent. Refer to Tables 3 and 4 for an exact definition of these pins.

The ALU shifter also provides the capability to sign extend at slice boundaries. Under instruction control, the SIO_0 (sign) input can be extended through Y_0, Y_1, Y_2, Y_3 and propagated to the SIO_3 output.

A cascadable, five-bit parity generator/checker is designed into the Am2903 ALU shifter and provides ALU error detection capability. Parity for the F_0, F_1, F_2, F_3 ALU outputs and SIO_3 input is generated and, under instruction control, is made available at the SIO_0 output. Refer to the Am2903 applications section for a more detailed description of the Am2903 sign extension and parity generation/checking capability.

The instruction inputs determine the ALU shifter operation. Table 4 defines the special functions and the operation the ALU shifter performs for each. When the Am2903 executes instructions other than the nine special functions, the ALU shifter operation is determined by instruction bits $I_8I_7I_6I_5$. Table 3 defines the ALU shifter operation as a function of these four bits.

Q Register

The Q Register is an auxiliary four-bit register which is clocked on the LOW-to-HIGH transition of the CP input. It is intended primarily for use in multiplication and division operations; however, it can also be used as an accumulator or holding register for some applications. The ALU output, F, can be loaded into the Q Register, and/or the Q Register can be selected as the source for the ALU S operand. The shifter at the input to the Q Register provides the capability to shift the Q Register contents up one bit position (2Q) or down one bit position (Q/2). Only logical shifts are performed. QIO_0 and QIO_3 are bidirectional shift serial inputs/outputs. During a Q Register shift-up operation, QIO_0 is a serial shift input and QIO_3 is a serial shift output. During a shift-down operation, QIO_3 is a serial shift input and QIO_0 is a serial shift output.

Double-length arithmetic and logical shifting capability is provided by the Am2903. The double-length shift is performed by connecting QIO_3 of the most significant slice to SIO_0 of the least significant slice, and executing an instruction which shifts both the ALU output and the Q Register.

The Q Register and shifter are controlled by the instruction inputs. Table 4 defines the Am2903 special functions and the operations which the Q Register and shifter perform for each. When the Am2903 executes instructions other than the nine special functions, the Q Register and shifter operation is controlled by instruction bits $I_8I_7I_6I_5$. Table 3 defines the Q Register and shifter operation as a function of these four bits.

Output Buffers

The DB and Y ports are bidirectional I/O ports driven by three-state output buffers with external output enable controls. The Y output buffers are enabled when the $\overline{OE_Y}$ input is LOW and are in the high-impedance state when $\overline{OE_Y}$ is HIGH. Likewise, the DB output buffers are enabled when the $\overline{OE_B}$ input is LOW and in the high-impedance state when $\overline{OE_B}$ is HIGH.

The zero, Z, pin is an open collector input/output that can be wire-OR'ed between slices. As an output it can be used as a zero detect status flag and generally indicates that the $Y_{0\text{-}3}$ pins are all LOW, whether they are driven from the Y output buffers or from an external source connected to the $Y_{0\text{-}3}$ pins. To some extent the meaning of this signal varies with the instruction being performed. Refer to Table 5 for an exact definition of this signal as a function of the Am2903 instruction.

TABLE 3. ALU DESTINATION CONTROL FOR I_0 OR I_1 OR I_2 OR I_3 OR I_4 = HIGH, $\overline{IEN}$ = LOW.

I_8	I_7	I_6	I_5	Hex Code	ALU Shifter Function	SIO_3		Y_3		Y_2		Y_1	Y_0	SIO_0	$\overline{Write}$	Q Reg & Shifter Function	QIO_3	QIO_0
						Most Sig. Slice	Other Slices	Most Sig. Slice	Other Slices	Most Sig. Slice	Other Slices							
L	L	L	L	0	Arith. F/2→Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Hold	Hi-Z	Hi-Z
L	L	L	H	1	Log. F/2→Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Hold	Hi-Z	Hi-Z
L	L	H	L	2	Arith. F/2→Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Log. Q/2→Q	Input	Q_0
L	L	H	H	3	Log. F/2→Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Log. Q/2→Q	Input	Q_0
L	H	L	L	4	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	L	Hold	Hi-Z	Hi-Z
L	H	L	H	5	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	H	Log. Q/2→Q	Input	Q_0
L	H	H	L	6	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	H	F→Q	Hi-Z	Hi-Z
L	H	H	H	7	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	L	F→Q	Hi-Z	Hi-Z
H	L	L	L	8	Arith. 2F→Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	L	L	H	9	Log. 2F→Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	L	H	L	A	Arith. 2F→Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log. 2Q→Q	Q_3	Input
H	L	H	H	B	Log. 2F→Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log. 2Q→Q	Q_3	Input
H	H	L	L	C	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	H	Hold	Hi-Z	Hi-Z
H	H	L	H	D	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	H	Log. 2Q→Q	Q_3	Input
H	H	H	L	E	SIO_0→Y_0, Y_1, Y_2, Y_3	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	H	H	H	F	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	L	Hold	Hi-Z	Hi-Z

Parity = $F_3 \forall F_2 \forall F_1 \forall F_0 \forall SIO_3$
$\forall$ = Exclusive OR

L = LOW
H = HIGH

Hi-Z = High Impedance

TABLE 4. SPECIAL FUNCTIONS: $I_0 = I_1 = I_2 = I_3 = I_4$ = LOW, $\overline{IEN}$ = LOW

I_8	I_7	I_6	I_5	Hex Code	Special Function	ALU Function	ALU Shifter Function	SIO_3 Most Sig. Slice	SIO_3 Other Slices	SIO_0	Q Reg & Shifter Function	QIO_3	QIO_0	$\overline{WRITE}$
L	L	L	L	0	Unsigned Multiply	F= S+C_n if Z=L F=R+S+C_n if Z=H	Log. F/2→Y (Note 1)	Hi-Z	Input	F_0	Log. Q/2→Q	Input	Q_0	L
L	L	H	L	2	Two's Complement Multiply	F=S+C_n if Z=L F=R+S+C_n if Z=H	Log. F/2→Y (Note 2)	Hi-Z	Input	F_0	Log. Q/2→Q	Input	Q_0	L
L	H	L	L	4	Increment by One or Two	F=S+1+C_n	F→Y	Input	Input	Parity	Hold	Hi-Z	Hi-Z	L
L	H	L	H	5	Sign/Magnitude-Two's Complement	F=$\overline{S}$+C_n if Z=L F=$\overline{S}$+C_n if Z=H	F→Y (Note 3)	Input	Input	Parity	Hold	Hi-Z	Hi-Z	L
L	H	H	L	6	Two's Complement Multiply, Last Cycle	F=S+C_n if Z=L F=S−R−1+C_n if Z=H	Log. F/2→Y (Note 2)	Hi-Z	Input	F_0	Log. Q/2→Q	Input	Q_0	L
H	L	L	L	8	Single Length Normalize	F=S+C_n	F→Y	F_3	F_3	Hi-Z	Log. 2Q→Q	Q_3	Input	L
H	L	H	L	A	Double Length Normalize and First Divide Op.	F=S+C_n	Log 2F→Y	$R_3 \forall F_3$	F_3	Input	Log. 2Q→Q	Q_3	Input	L
H	H	L	L	C	Two's Complement Divide	F=S+R+C_n if Z=L F=S−R−1+C_n if Z=H	Log. 2F→Y	$\overline{R_3 \forall F_3}$	F_3	Input	Log. 2Q→Q	Q_3	Input	L
H	H	H	L	E	Two's Complement Divide, Correction and Remainder	F=S+R+C_n if Z=L F=S−R−1+C_n if Z=H	F→Y	F_3	F_3	Hi-Z	Log. 2Q→Q	Q_3	Input	L

NOTES: 1. At the most significant slice only, the C_{n+4} signal is internally gated to the Y_3 output.
2. At the most significant slice only, $F_3 \forall$ OVR is internally gated to the Y_3 output.
3. At the most significant slice only, $S_3 \forall F_3$ is generated at the Y_3 output.
4. Op codes 1, 3, 7, 9, B, D, and F are reserved for future use.

L = LOW
H = HIGH
X = Don't Care

Hi-Z = High Impedance
$\forall$ = Exclusive OR
Parity = $SIO_3 \forall F_3 \forall F_2 \forall F_1 \forall F_0$

Instruction Decoder

The Instruction Decoder generates required internal control signals as a function of the nine Instruction inputs, I_{0-8}; the Instruction Enable input, $\overline{IEN}$; the $\overline{LSS}$ input; and the $\overline{WRITE}/\overline{MSS}$ input/output.

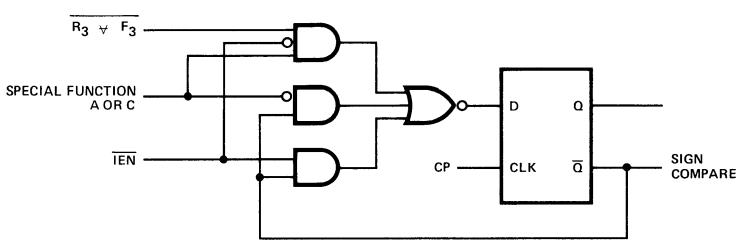
The $\overline{WRITE}$ output is LOW when an instruction which writes data into the RAM is being executed. Refer to Tables 3 and 4 for a definition of the $\overline{WRITE}$ output as a function of the Am2903 instruction inputs.

When $\overline{IEN}$ is HIGH, the $\overline{WRITE}$ output is forced HIGH and the Q Register and Sign Compare Flip-Flop contents are preserved.

When $\overline{IEN}$ is LOW, the $\overline{WRITE}$ output is enabled and the Q Register and Sign Compare Flip-Flop can be written according to the Am2903 instruction. The Sign Compare Flip-Flop is an on-chip flip-flop which is used during an Am2903 divide operation (see Figure B).

Programming the Am2903 Slice Position

Tying the $\overline{LSS}$ input LOW programs the slice to operate as a least significant slice (LSS) and enables the $\overline{WRITE}$ output signal onto the $\overline{WRITE}/\overline{MSS}$ bidirectional I/O pin. When $\overline{LSS}$ is tied HIGH, the $\overline{WRITE}/\overline{MSS}$ pin becomes an input pin; tying the $\overline{WRITE}/\overline{MSS}$ pin HIGH programs the slice to operate as an intermediate slice (IS) and tying it LOW programs the slice to operate as a most significant slice (MSS).



The sign compare signal appears at the Z output of the most significant slice during special functions C, D and E, F. Refer to Table 5.

Figure B. Sign Compare Flip-Flop.

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TABLE 5. Am2903 STATUS OUTPUTS

(Hex) $I_8I_7I_6I_5$	(Hex) $I_4I_3I_2I_1$	I_0	Gi (I=0 to 3)	Pi (I=0 to 3)	C_{n+4}	$\overline{P}$/OVR		$\overline{G}$/N		Z		
						Most Sig. Slice	Other Slices	Most Sig. Slice	Other Slices	Most Sig. Slice	Intermediate Slice	Least Sig. Slice
X	0	H	0	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	1	X	$\overline{R}_i \wedge S_i$	$\overline{R}_i \vee S_i$	G ∨ PC_n	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	2	X	$R_i \wedge \overline{S}_i$	$R_i \vee \overline{S}_i$	G ∨ PC_n	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	3	X	$R_i \wedge S_i$	$R_i \vee S_i$	G∨PC_n	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	4	X	0	S_i	G∨PC_n	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	5	X	0	$\overline{S}_i$	G∨PC_n	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	6	X	0	R_i	G∨PC_n	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	7	X	0	$\overline{R}_i$	G∨PC_n	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	8	X	0	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	9	X	$\overline{R}_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	A	X	$R_i \wedge S_i$	$R_i \vee S_i$	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	B	X	$\overline{R}_i \wedge S_i$	$\overline{R}_i \vee S_i$	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	C	X	$R_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	D	X	$\overline{R}_i \wedge \overline{S}_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	E	X	$R_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	F	X	$\overline{R}_i \wedge \overline{S}_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
0	0	L	0 if Z=L $R_i \wedge S_i$ if Z=H	S_i if Z=L $R_i \vee S_i$ if Z=H	G ∨ PC_n	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
2	0	L	0 if Z=L $R_i \wedge S_i$ if Z=H	S_i if Z=L $R_i \vee S_i$ if Z=H	G ∨ PC_n	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
4	0	L	See Note 1	See Note 2	G ∨ PC_n	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
5	0	L	0	S_i if Z=L $\overline{S}_i$ if Z=H	G ∨ PC_n	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3 if Z=L $F_3 \forall S_3$ if Z=H	$\overline{G}$	S_3	Input	Input
6	0	L	0 if Z=L $\overline{R}_i \wedge S_i$ if Z=H	S_i if Z=L $\overline{R}_i \vee S_i$ if Z=H	G ∨ PC_n	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
8	0	L	0	S_i	See Note 3	$Q_2 \forall Q_1$	$\overline{P}$	Q_3	$\overline{G}$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
A	0	L	0	S_i	See Note 4	$F_2 \forall F_1$	$\overline{P}$	F_3	$\overline{G}$	See Note 5	See Note 5	See Note 5
C	0	L	$R_i \wedge S_i$ if Z=L $\overline{R}_i \wedge S_i$ if Z=H	$\overline{R}_i \vee S_i$ if Z=L $\overline{R}_i \vee S_i$ if Z=H	G∨PC_n	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input
E	0	L	$R_i \wedge S_i$ if Z=L $\overline{R}_i \wedge S_i$ if Z=H	$R_i \vee S_i$ if Z=L $\overline{R}_i \vee S_i$ if Z=H	G∨PC_n	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input

L = LOW = 0
H = HIGH = 1
∨ = OR
∧ = AND
∀ = EXCLUSIVE OR
$P = P_3P_2P_1P_0$
$G = G_3 \vee G_2P_3 \vee G_1P_2P_3 \vee G_0P_1P_2P_3$
$C_{n+3} = G_2 \vee G_1P_2 \vee G_0P_1P_2 \vee C_nP_pP_1P_2$

NOTES:
1. If $\overline{LSS}$ is LOW, $G_0 = S_0$ and $G_{1,2,3} = 0$
   If $\overline{LSS}$ is HIGH, $G_{0,1,2,3} = 0$
2. If $\overline{LSS}$ is LOW, $P_0 = 1$ and $P_{1,2,3} = S_{1,2,3}$
   If $\overline{LSS}$ is HIGH, $P_i = S_i$
3. At the most significant slice, $C_{n+4} = Q_3 \forall Q_2$
   At other slices, $C_{n+4} = G \vee PC_n$
4. At the most significant slice, $C_{n+4} = F_3 \forall F_2$
   At other slices, $C_{n+4} = G \vee PC_n$
5. $Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3\overline{F}_0\overline{F}_1\overline{F}_2\overline{F}_3$

Am2903 SPECIAL FUNCTIONS

The Am2903 provides nine Special Functions which facilitate the implementation of the following operations:

- Single- and Double-Length Normalization
- Two's Complement Division
- Unsigned and Two's Complement Multiplication
- Conversion Between Two's Complement and Sign/Magnitude Representation
- Incrementation by One or Two

Table 4 defines these Special Functions.

The Single-Length and Double-Length Normalization functions can be used to adjust a single-precision or double-precision floating point number in order to bring its mantissa within a specified range.

Three Special Functions which can be used to perform a two's complement, non-restoring divide operation are provided by the Am2903. These functions provide both single- and double-precision divide operations and can be performed in "n" clock cycles, where "n" is the number of bits in the quotient.

The Unsigned Multiply Special Function and the two Two's Complement Multiply Special Functions can be used to multiply two n-bit, unsigned or two's complement numbers, respectively, in n clock cycles. These functions utilize the conditional add and shift algorithm. During the last cycle of the two's complement multiplication, a conditional subtraction, rather than addition, is performed because the sign bit of the multiplier carries negative weight.

The Sign/Magnitude-Two's Complement Special Function can be used to convert number representation systems. A number expressed in Sign/Magnitude representation can be converted to the Two's Complement representation, and vice-versa, in one clock cycle.

The Increment by One or Two Special Function can be used to increment an unsigned or two's complement number by one or two. This is useful in 16-bit word, byte-addressable machines, where the word addresses are multiples of two.

Refer to Am2903 applications section for a more detailed description of these Special Functions.

PIN DEFINITIONS

A_{0-3} Four RAM address inputs which contain the address of the RAM word appearing at the RAM A output port.

B_{0-3} Four RAM address inputs which contain the address of the RAM word appearing at the RAM B output port and into which new data is written when the $\overline{WE}$ input and the CP input are LOW.

$\overline{WE}$ The RAM write enable input. If $\overline{WE}$ is LOW, data at the Y I/O port is written into the RAM when the CP input is LOW. When $\overline{WE}$ is HIGH, writing data into the RAM is inhibited.

DA_{0-3} A four-bit external data input which can be selected as one of the Am2903 ALU operand sources; DA_0 is the least significant bit.

$\overline{EA}$ A control input which, when HIGH, selects DA_{0-3} and, when LOW, selects RAM output A as the ALU R operand.

DB_{0-3} A four-bit external data input/output. Under control of the $\overline{OE_B}$ input, RAM output port B can be directly read on these lines, or input data on these lines can be selected as the ALU S operand.

$\overline{OE_B}$ A control input which, when LOW, enables RAM output B onto the DB_{0-3} lines and, when HIGH, disables the RAM output B tri-state buffers.

C_n The carry-in input to the Am2903 ALU.

I_{0-8} The nine instruction inputs used to select the Am2903 operation to be performed.

$\overline{IEN}$ The instruction enable input which, when LOW, enables the $\overline{WRITE}$ output and allows the Q Register and the Sign Compare flip-flop to be written. When $\overline{IEN}$ is HIGH, the $\overline{WRITE}$ output is forced HIGH and the Q Register and Sign Compare flip-flop are in the hold mode.

C_{n+4} This output generally indicates the carry-out of the Am2903 ALU. Refer to Table 5 for an exact definition of this pin.

$\overline{G}$/N A multi-purpose pin which indicates the carry generate, $\overline{G}$, function at the least significant and intermediate slices, and generally indicates the sign, N, of the ALU result at the most significant slice. Refer to Table 5 for an exact definition of this pin.

$\overline{P}$/OVR A multi-purpose pin which indicates the carry propagate, $\overline{P}$, function at the least significant and intermediate slices, and indicates the conventional two's complement overflow, OVR, signal at the most significant slice. Refer to Table 5 for an exact definition of this pin.

Z An open-collector input/output pin which, when HIGH, generally indicates the Y_{0-3} outputs are all LOW. For some Special Functions, Z is used as an input pin. Refer to Table 5 for an exact definition of this pin.

SIO_0, SIO_3 Bidirectional serial shift inputs/outputs for the ALU shifter. During a shift-up operation, SIO_0 is an input and SIO_3 an output. During a shift-down operation, SIO_3 is an input and SIO_0 is an output. Refer to Tables 3 and 4 for an exact definition of these pins.

QIO_0, QIO_3 Bidirectional serial shift inputs/outputs for the Q shifter which operate like SIO_0 and SIO_3. Refer to Tables 3 and 4 for an exact definition of these pins.

$\overline{LSS}$ An input pin which, when tied LOW, programs the chip to act as the least significant slice (LSS) of an Am2903 array and enables the $\overline{WRITE}$ output onto the $\overline{WRITE}/\overline{MSS}$ pin. When $\overline{LSS}$ is tied HIGH, the chip is programmed to operate as either an intermediate or most significant slice and the $\overline{WRITE}$ output buffer is disabled.

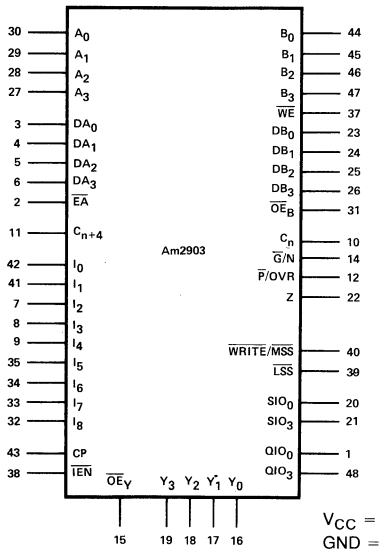
$\overline{WRITE}$/$\overline{MSS}$ When $\overline{LSS}$ is tied LOW, the $\overline{WRITE}$ output signal appears at this pin; the $\overline{WRITE}$ signal is LOW when an instruction which writes data into the RAM is being executed. When $\overline{LSS}$ is tied HIGH, $\overline{WRITE}/\overline{MSS}$ is an input pin; tying it HIGH programs the chip to operate as an intermediate slice (IS) and tying it LOW programs the chip to operate as the most significant slice (MSS).

Y_{0-3} Four data inputs/outputs of the Am2903. Under control of the $\overline{OE_Y}$ input, the ALU shifter output data can be enabled onto these lines, or these lines can be used as data inputs when external data is written directly into the RAM.

$\overline{OE_Y}$ A control input which, when LOW, enables the ALU shifter output data onto the Y_{0-3} lines and, when HIGH, disables the Y_{0-3} three-state output buffers.

CP The clock input to the Am2903. The Q Register and Sign Compare flip-flop are clocked on the LOW-to-HIGH transition of the CP signal. When enabled by $\overline{WE}$, data is written in the RAM when CP is LOW.

LOGIC SYMBOL



V_{CC} = Pin 36
GND = Pin 13

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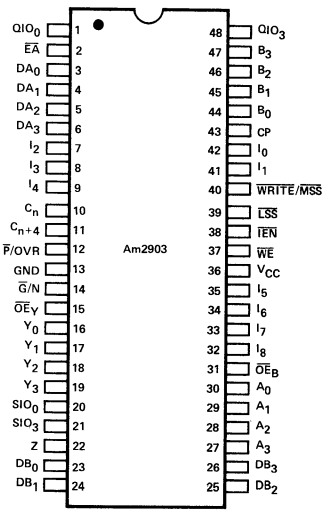
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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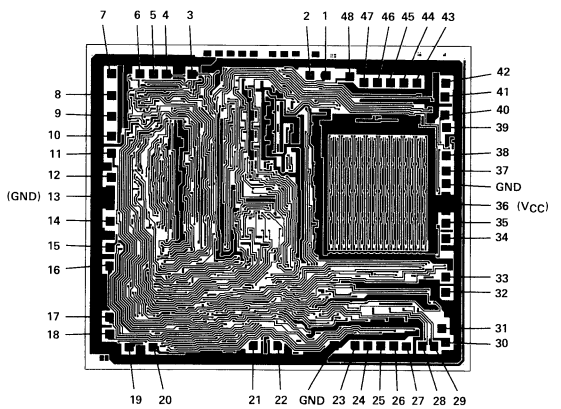
Metallization and Pad Layout



DIE SIZE 0.163" X 0.197"
Note: Pin numbers correspond to DIP package.

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2903DC	D-48	C	C-1
AM2903DC-B	D-48	C	B-1
AM2903DM	D-48	M	C-3
AM2903DM-B	D-48	M	B-3
AM2903FM	F-48	M	C-3
AM2903FM-B	F-48	M	B-3

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Am2903
OPERATING RANGE

P/N	Range	Temperature	V_{CC}	
Am2903PC, DC	COM'L	T_A = 0°C to +70°C	V_{CC}= 5.0V ±5%	(MIN. = 4.75V, MAX. = 5.25V)
Am2903DM, FM	MIL	T_C = −55°C to +125°C	V_{CC} = 5.0V ±10%	(MIN. = 4.50V, MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.6mA Y_0-Y_3, $\overline{G}$/N		2.4			Volts
			I_{OH} = −800μA DB_{0-3}, $\overline{P}$/OVR SIO_0, SIO_3, QIO_0, QIO_3, $\overline{WRITE}$, C_{n+4}		2.4			
I_{CEX}	Output Leakage Current for Z Output (Note 4)	V_{CC} = MIN., V_{OH} = 5.5V V_{IN} = V_{IH} or V_{IL}					250	μA
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} = or V_{IL}	Y_0, Y_1, Y_2 Y_3, Z	I_{OL} = 20mA (COM'L)			0.5	Volts
				I_{OL} = 16mA (MIL)				
			DB_0, DB_1, DB_2, DB_3	I_{OL} = 12mA (COM'L)			0.5	
				I_{OL} = 8.0mA (MIL)				
			$\overline{G}$/N	I_{OL} = 18mA			0.5	
			$\overline{P}$/OVR	I_{OL} = 10mA			0.5	
			C_{n+4}, SIO_0 SIO_3, QIO_0 QIO_3, $\overline{WRITE}$	I_{OL} = 8.0mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 6)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 6)					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V (Note 4)	C_n				−3.6	mA
			Y_0, Y_1, Y_2, Y_3				−1.08	
			I_0, I_1, I_2, I_3, I_4, DA_0, DA_1, DA_2, DA_3, SIO_0 SIO_3, QIO_0, QIO_3, $\overline{MSS}$, DB_0, DB_1, DB_2, DB_3				−0.72	
			All other inputs				−0.36	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V (Note 4)	C_n				120	μA
			Y_0, Y_1, Y_2, Y_3				110	
			I_0-I_4, DA_0-DA_3				40	
			SIO_0, SIO_3, QIO_0, QIO_3, DB_{0-3}, $\overline{MSS}$				90	
			All other inputs				20	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{OZH} I_{OZL}	Off State (HIGH Impedance) Output Current	V_{CC} = MAX., (Note 4)	Y_0-Y_3	V_O = 2.4V			110	μA
				V_O = 0.5V			−1130	
			DB_{0-3}, QIO_0, QIO_0, SIO_0, SIO_3, $\overline{MSS}$/IS	V_O = 2.4V			90	
				V_O = 0.5V			−770	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = MAX + 0.5V V_O = 0.5V			−30		−85	mA
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX.	T_A = 25°C			220	335	mA
			COM'L	T_A = 0 to 70°C			350	
				T_A = 70°C			291	
			MIL	T_C = −55 to 125°C			395	
				T_C = 125°C			258	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Y_{0-3}, DB_{0-3}, $SIO_{0,3}$, $QIO_{0,3}$ and WRITE/MSS are three state outputs internally connected to TTL inputs. Z is an open-collector output internally connected to a TTL input. Input characteristics are measured under conditions such that the outputs are in the OFF state.
5. Worst case I_{CC} is at minimum temperature.
6. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

SWITCHING CHARACTERISTICS (Typical Room Temperature Performance)

Tables I, II, and III define the nominal timing characteristics of the Am2903 at 25°C and 5.0V. The Tables divide the parameters into three types: pulse characteristics for the clock and write enable, combinational delays from input to output, and set-up and hold times relative to the clock and write pulse.

Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level.

TABLE I
Write Pulse and Clock Characteristics

Time	
Minimum Time CP and $\overline{WE}$ both LOW to write	30ns
Minimum Clock LOW Time	30ns
Minimum Clock HIGH Time	50ns

TABLE II
Combinational Propagation Delays, All in ns.
Outputs Fully Loaded. CL = 50pf (except output disable tests)

From Input \ To Output	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	QIO_0, QIO_3	SIO_0	SIO_3	SIO_3 (Parity)
A, B Addresses (Arith. Mode)	65	60	55	75	64	70	33	–	–	61	69	87
A, B Addresses (Logic Mode)	56	–	46	67	56	–	33	–	–	55	64	81
DA, DB Inputs (Logic Mode)	39	–	25	48	38	–	–	–	–	36	47	56
DA, DB Inputs (Arith. Mode)	39	37	26	52	38	51	–	–	–	36	47	60
$\overline{EA}$	44	38	29	54	44	53	–	–	–	42	52	
C_n	25	21	–	39	20	38	–	–	–	21	25	48
I_0	39	35	24	48	37	48	–	*15	–	41	46	
I_{4321}	45	43	32	55	44	55	–	*17	–	45	51	
I_{8765}	25	–	–	37	–	–	–	18	22	24	27	
$\overline{I_{EN}}$	–	–	–	–	–	–	–	10	–	–	–	–
$\overline{OEB}$ Enable/Disable	–	–	–	–	–	–	7	–	–	–	–	–
$\overline{OEY}$ Enable/Disable	10	–	–	–	–	–	–	–	–	–	–	–
SIO_0, SIO_3	13	–	–	–	–	–	–	–	–	–	12	18
Clock	58	52	40	72	56	72	24	–	28	55	63	76

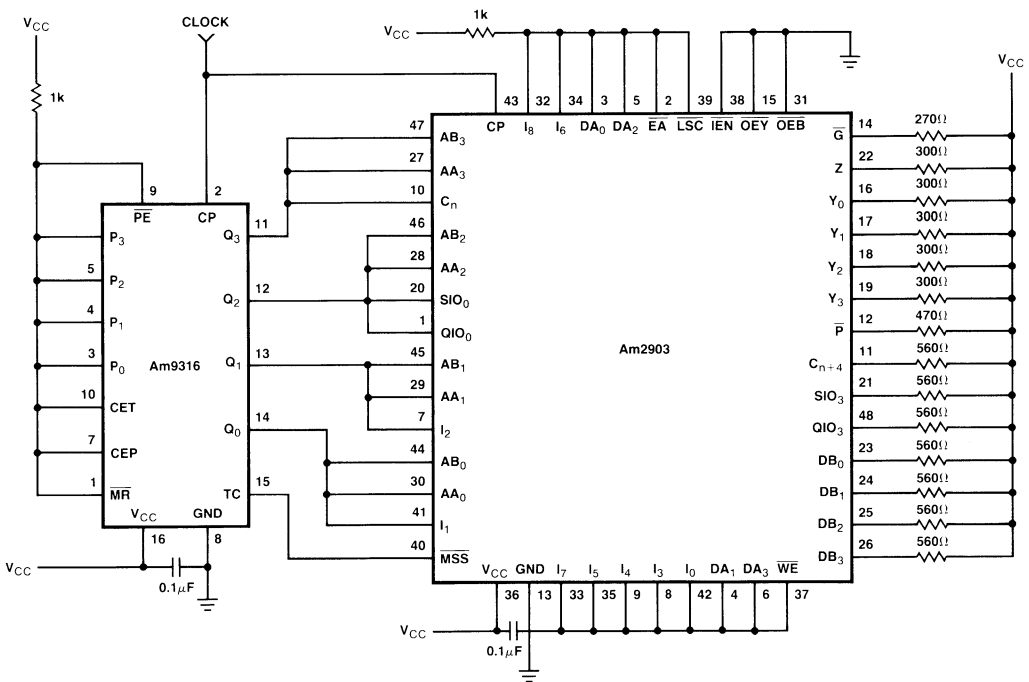
*Applies only when leaving special functions.

TABLE III
Set-Up and Hold Times (All in ns)
CAUTION: READ NOTES TO TABLE III.
NA = Not Applicable; no timing constraint.

Input	With Respect to to this Signal	HIGH-to-LOW		LOW-to-HIGH		Comment
		Set-up	Hold	Set-up	Hold	
Y	Clock	NA	NA	10	0	To store Y in RAM or Q
$\overline{WE}$ HIGH	Clock	5	Note 2	Note 2	0	To Prevent Writing
$\overline{WE}$ LOW	Clock	NA	NA	30	0	To Write into RAM
A,B as Sources	Clock	20	0	NA	NA	See Note 3
B as a Destination	Clock and $\overline{WE}$ both LOW	0	Note 4	Note 4	0	To Write Data only into the Correct B Address
QIO_0, QIO_3	Clock	NA	NA	10	0	To Shift Q
I_{8765}	Clock	30	Note 5	Note 5	0	
$\overline{IEN}$ HIGH	Clock	10	Note 2	Note 2	0	To Prevent Writing
$\overline{IEN}$ LOW	Clock	NA	NA	10	0	To Write into Q

Notes To Table III. (Set-up and Hold Times)

1. For set-up times from all inputs not specified in Table III, the set-up time is computed by calculating the delay to stable Y outputs and then allowing the Y set-up time. Even if the RAM is not being loaded, the Y set-up time is necessary to set-up the Q register. All unspecified hold times are less than or equal to zero relative to the clock LOW-to-HIGH edge.
2. $\overline{WE}$ controls writing into the RAM. $\overline{IEN}$ controls writing into Q and, indirectly, controls $\overline{WE}$ through the write output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must be HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
3. A and B addresses must be set-up prior to clock LOW transition to capture data in latches at RAM output.
4. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
5. Because I_{8765} control the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, preventing writing.



V_{CC} = 5.0V
Frequency = 100kHz
T_A = +125°C
All registers are 1/4 watt ±5%
This circuit conforms to MIL-STD-883, Methods 1005 and 1015, Condition D.
One Am9316 Can Drive Maximum of Five Am2903s.

Am2903 Burn-in and Life Test Circuit

USING THE Am2903

Am2903 APPLICATIONS

The Am2903 is designed to be used in microprogrammed systems. Figure 1 illustrates a recommended architecture. The control and data inputs to the Am2903 normally will all come from registers clocked at the same time as the Am2903. The register inputs come from a ROM or PROM – the "microprogram store". This memory contains sequences of microinstructions which apply the proper control signals to the Am2903's and other circuits to execute the desired operation.

The address lines of the microprogram store are driven from the Am2910 Microprogram Sequencer. This device has facilities for storing an address, incrementing an address, jumping to any address, and linking subroutines. The Am2910 is controlled by some of the bits coming from the microprogram store. Essentially, these bits are the "next instruction" control.

One Level Pipeline Based System

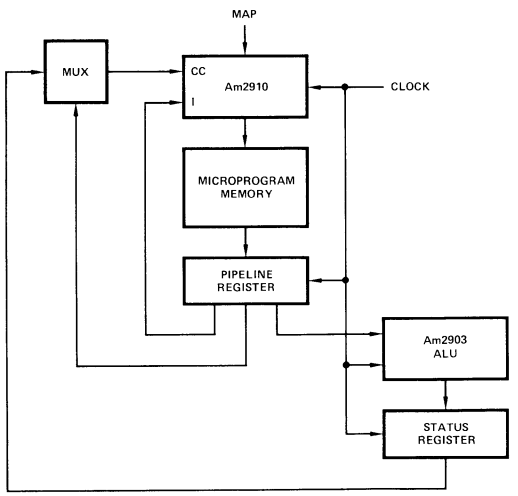


Figure 1. Typical Microprogram Architecture.

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Note that with the microprogram register in between the microprogram memory store and the Am2903's, a microinstruction accessed on one cycle is executed on the next cycle. As one microinstruction is executed, the next microinstruction is being read from microprogram memory. In this configuration, system speed is improved because the execution time in the Am2903's occurs in parallel with the access time of the microprogram store. Without the "pipeline register", these two functions must occur serially.

Expansion of the Am2903

The Am2903 is a four-bit CPU slice. Any number of Am2903's can be interconnected to form CPU's of 8, 16, 32, or more bits, in four-bit increments. Figure 2 illustrates the interconnection of four Am2903's to form a 16-bit CPU, using ripple carry.

With the exception of the carry interconnection, all expansion schemes are the same. The QIO_3 and SIO_3 pins are bidirectional left/right shift lines at the MSB of the device. For all devices except the most significant, these lines are connected to the QIO_0 and SIO_0 pins of the adjacent more significant device. These connections allow the Q Registers of all Am2903's to be shifted left or right as a contiguous n-bit register, and also allow the ALU output data to be shifted left or right as a contiguous n-bit word prior to storage in the RAM. At the LSB and MSB of the CPU, the shift pins should be connected to a shift multiplexer which can be controlled by the microcode to select the appropriate input signals to the shift inputs.

Device 1 has been defined as the least significant slice (LSS) and its $\overline{LSS}$ pin has accordingly been grounded. The Write/Most Significant Slice ($\overline{WRITE}/\overline{MSS}$) pin of device 1 is now defined as being the Write output, which may now be used to drive the write enable ($\overline{WE}$) signal common to the four devices. Devices 2 and 3 are designated as intermediate slices and hence the $\overline{LSS}$ and $\overline{WRITE}/\overline{MSS}$ pins are tied HIGH. Device 4 is designated the most significant slice ($\overline{MSS}$) with the $\overline{LSS}$ pin tied HIGH and the $\overline{WRITE}/\overline{MSS}$ pin held LOW. The open collector, bidirectional Z pins are tied together for detecting zero or for inter-chip communication for some special instruction. The Carry-Out (C_{n+4}) is connected to the Carry-In (C_n) of the next chip in the case of ripple carry. For a faster carry scheme, an Am2902 may be employed (as shown in Figure 3) such that the $\overline{G}$ and $\overline{P}$ outputs of the Am2903 are connected to the appropriate $\overline{G}$ and $\overline{P}$ inputs of the Am2902, while the C_{n+x}, C_{n+y}, and C_{n+z} outputs of the Am2902 are connected to the C_n input of the appropriate Am2903. Note that $\overline{G}$/N and $\overline{P}$/OVR pin functions are device dependent. The most significant slice outputs N and OVR while all other slices output $\overline{G}$ and $\overline{P}$.

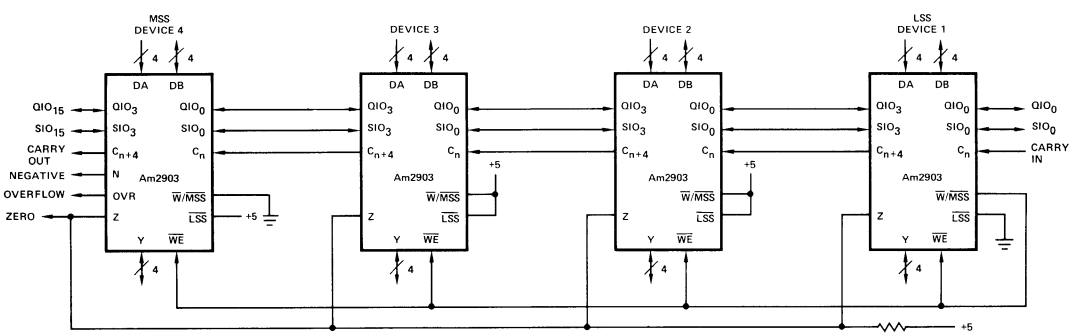

Figure 2. 16-Bit CPU with Ripple Carry.

MPR-036

The $\overline{IEN}$ pin of the Am2903 allows the option of conditional instruction execution. If $\overline{IEN}$ is LOW, all internal clocking is enabled, allowing the latches, RAM, and Q Register to function. If $\overline{IEN}$ is HIGH, the RAM and Q Register are disabled. The RAM is controlled by $\overline{IEN}$ if $\overline{WE}$ is connected to the $\overline{WRITE}$ output.

It would be appropriate at this point to mention that the Am2903 may be microcoded to work in either two-or three-address architecture modes. The two-address modes allow A+B→B while the three-address mode makes possibleA+B→C. Implementation of a three-address architecture is made possible by varying the timing of $\overline{IEN}$ in relationship to the external clock and changing the B address as shown in Figure 4. This technique is discussed in more detail under Memory Expansion.

Parity

The Am2903 computes parity on a chosen word when the instruction bits I_{5-8} have the values of 4_{16} to 7_{16} as shown in Table 3. The computed parity is the result of the exclusive OR of the individual ALU outputs and SIO_3. Parity output is found on SIO_0. Parity between devices may be cascaded by the interconnection of the SIO_0 and SIO_3 ports of the devices as shown in Figure 3. The equation for the parity output at SIO_0 port of device 1 is given by $SIO_0 = F_{15} \forall F_{14} \forall F_{13} \forall \ldots \forall F_1 \forall F_0 \forall SIO_{15}$.

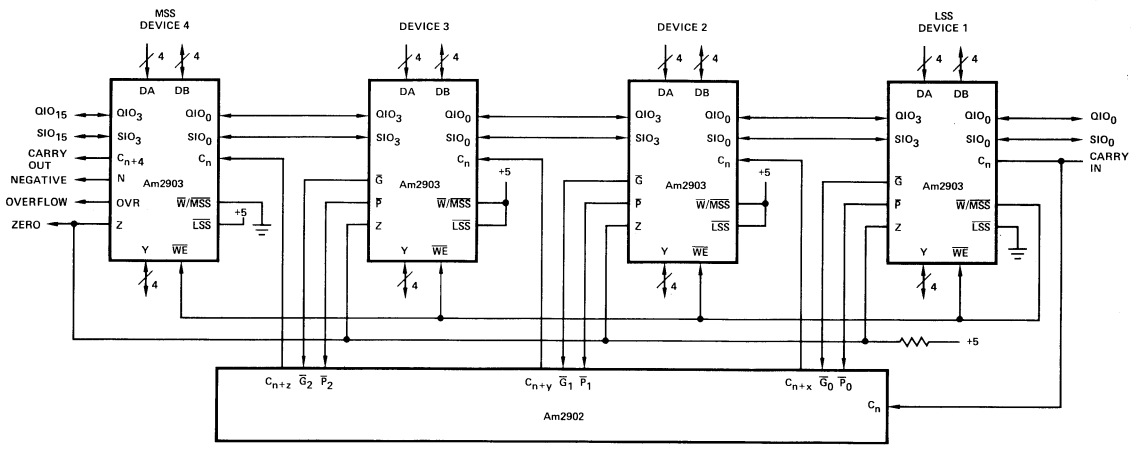

Figure 3. 16-Bit CPU with Carry Look Ahead.

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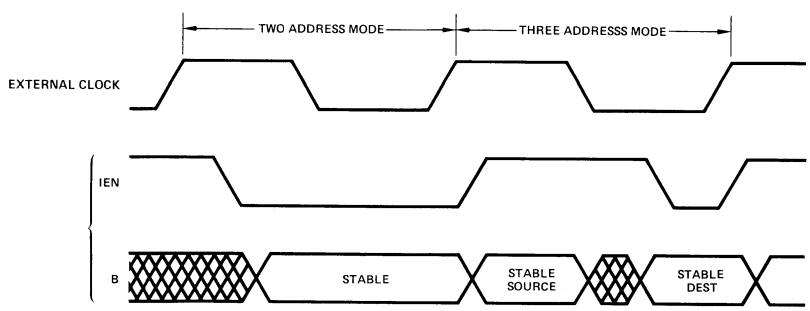


Figure 4. Relationship of $\overline{IEN}$ and Clock During Two Address and Three Address Modes.

MPR-038

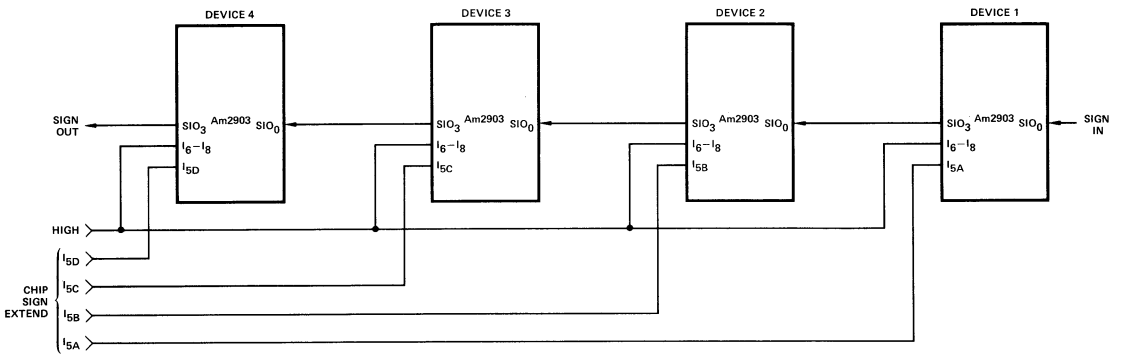


Figure 5. Sign Extend. MPR-039

Sign Extend

Sign extension across any number of Am2903 devices can be done in one microcycle. Referring again to the table of instructions (Table 3), the sign extend instruction (Hex instruction E) on I_{5-8} causes the sign present at the SIO_0 port of a device to be extended across the device and appear at the SIO_3 port and at the Y outputs. If the least significant bit of the instruction (bit I_5) is HIGH, Hex instruction F is present on I_{5-8}, commanding a shifter pass instruction. At this time, F_3 of the ALU is present on the SIO_3 output pin. It is then possible to control the extension of the sign across chip boundaries by controlling the state of I_5 when I_{6-8} are HIGH. Figure 5 outlines the Am2903 in sign extend mode. With I_{6-8} held HIGH, the individual chip sign extend is controlled by $I_{5A\text{-}D}$. If, for example, I_{5A} and I_{5B} are HIGH while I_{5C} and I_{5D} are LOW, the signal present at the boundaries of devices 2 and 3 (F_3 of device 2) will be extended across devices 3 and 4 at the SIO_3 pin of device 4. The output of the four devices will be available at their respective Y data ports. The next positive edge of the clock will load the Y outputs into the address selected by the B port. Hence, the results of the sign extension is stored in the RAM.

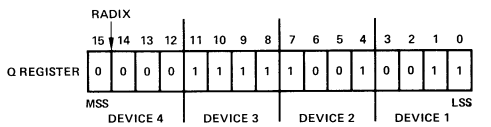
SPECIAL FUNCTIONS

When $I_{0-4} = 0$; the Am2903 is in the Special Function mode. In this mode, both the source and destination are controlled by I_{5-8}. The Special Functions are in essence special microinstructions that are used to reduce the number of microcycles needed to execute certain functions in the Am2903.

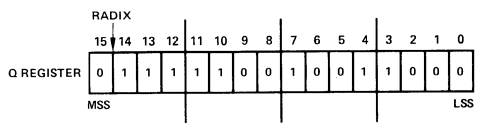
Normalization, Single- and Double-Length

Normalization is used as a means of referencing a number to a fixed radix point. Normalization strips out all leading sign bits such that the two bits immediately adjacent to the radix point are of opposite polarity.

Normalization is commonly used in such operations as fixed-to-floating point conversion and division. The Am2903 provides for normalization by using the Single-Length and Double-Length Normalize commands. Figure 6a represents the Q Register of a 16-bit processor which contains a positive number. When the Single-Length Normalize command is applied, each positive edge of the clock will cause the bits to shift toward the most significant bit (bit 15) of the Q Register. Zeros are shifted in via the QIO_0 port. When the bits on either side of the radix point (bits 14 and 15) are of opposite value, the number is considered to be normalized as shown in Figure 6b. The event of normalization is externally indicated by a HIGH level on the C_{n+4} pin of the most significant slice (C_{n+4} MSS = Q_3 MSS $\forall$ Q_2 MSS).



a) Unnormalized Positive Number.



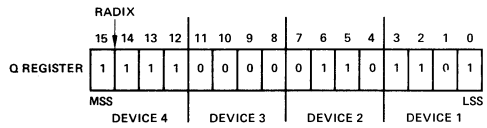
b) Normalized Positive Number.

Figure 6. MPR-040

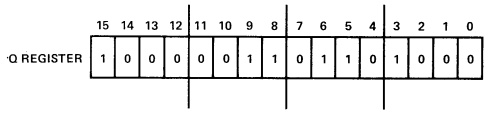
There are also provisions made for a normalization indication via the OVR pin one microcycle before the same indication is available on the C_{n+4} pin (OVR = Q_2 MSS $\forall$ Q_1 MSS). This is for use in applications that require a stage of register buffering of the normalization indication.

Since a number comprised of all zeros is not considered for normalization, the Am2903 indicates when such a condition arises. If the Q Register is zero and the Single-Length Normalization command is given, a HIGH level will be present on the Z line. The sign output, N, indicates the sign of the number stored in the Q register, Q_3 MSS. An unnormalized negative number (Figure 7a) is normalized in the same manner as a positive number. The results of single-length normalization are shown in Figure 7b. The device interconnection for single-length normalization is outlined in Figure 8. During single length normalization, the number of shifts performed to achieve normalization can be counted and stored in one of the working registers. This can be achieved by forcing a HIGH at the C_n input of the least significant slice, since during this special function the ALU performs the function $[B] + C_n$ and the result is stored in B.

Normalizing a double-length word can be done with the Double-Length Normalize command which assumes that a user-selected RAM Register contains the most significant portion of the word to be normalized while the Q Register holds the least significant half (Figure 9). The device interconnection for double-length normalization is shown in Figure 10. The C_{n+4}, OVR, N, and Z outputs of the most significant slice perform the same functions in double-length normalization as they did in single-length normalization except that C_{n+4}, OVR, and N are derived from the output of the ALU of the most significant slice in the case of double-length normalization, instead of the Q Register of the most significant



a) Unnormalized Negative Single Length Number.



b) Normalized Negative Single Length Number.

Figure 7.

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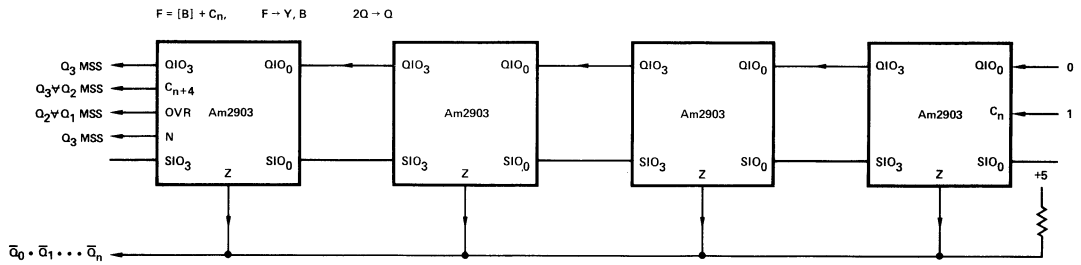


Figure 8. Single Length Normalize.

MPR-042

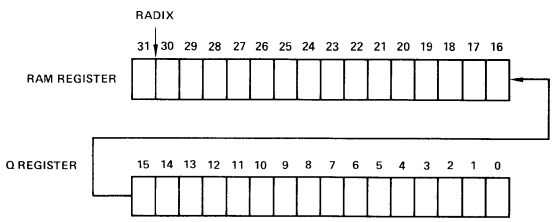


Figure 9. Double Length Word.

MPR-043

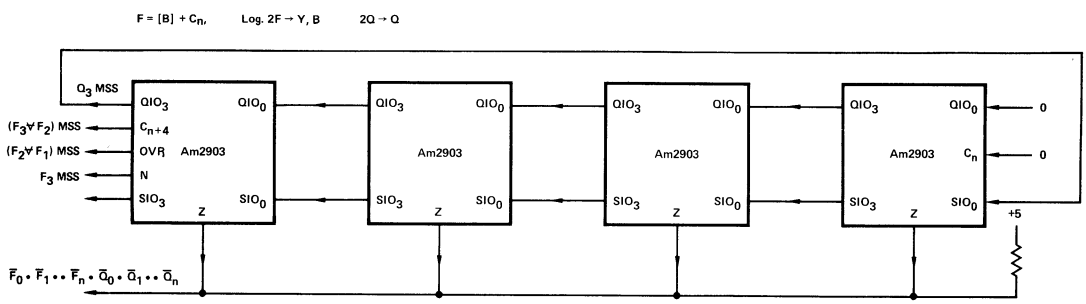


Figure 10. Double Length Normalize.

MPR-044

slice as in single-length normalization. A high-level Z line in double-length normalization reveals that the outputs of the ALU and Q Register are both zero, hence indicating that the double-length word is zero.

When double-length normalization is being performed, shift counting is done either with an extra microcycle or with an external counter.

Sign Magnitude, Two's Complement Conversion

As part of the special instruction set, the Am2903 can convert between two's complement and sign/magnitude representations. Figure 11 illustrates the interconnection needed for sign magnitude/two's complement conversion. The word to be converted is applied to the S input port of the ALU (from the RAM B port or the DB I/O port). The C_n input of device 1 is connected to the Z pin. The sign bit (S_3MSS) is brought out on the Z line and informs the other ALU's if the conversion is being performed on a negative or positive number. If the number to be converted is the most negative number in two's complement [i.e., 100 . . . 00 (-2^n)], an overflow indication will occur. This is because -2^n is one greater than any number that can be represented in sign magnitude notation and hence an attempted conversion to sign magnitude from -2^n will cause an overflow. When minus zero in sign magnitude notation (100 . . . 0) is converted to two's complement notation, the correct result is obtained (0 . . .0).

Increment by One or Two

Incrementation by One or Two is made possible by the Special Function of the same name. This command is quite useful in the case of byte addressable words. Referencing Figure 12, a word may be incremented by one if C_n is LOW or incremented by two if C_n is HIGH.

Unsigned Multiply

This Special Function allows for easy implementation of unsigned multiplication. Figure 13 is the unsigned multiply flow chart. The algorithm requires that initially the RAM word addressed by Address port B be zero, that the multiplier be in the Q Register, and that the multiplicand be in the register addressed by Address port A. The initial conditions for the execution of the algorithm are that: 1) register R_0 be reset to zero; 2) the multiplicand be in R_1; and 3) the multiplier be in R_2. The first operation transfers the multiplier, R_2, to the Q Register. The Unsigned Multiply instruction is then executed 16 times. During the Unsigned Multiply instruction, R_0 is addressed by RAM address port B and the multiplicand is addressed by RAM address port A.

When the unsigned Multiply command is given, the Z pin of device 1 becomes an output while the Z pins of the remaining devices are specified as inputs as shown in Figure 15. The Z output of device 1 is the same state as the least significant bit of the multiplier in the Q Register. The Z output of device 1 informs the ALU's of all the slices, via their Z pins, to add the partial product (referenced by the B address port) to the mul-

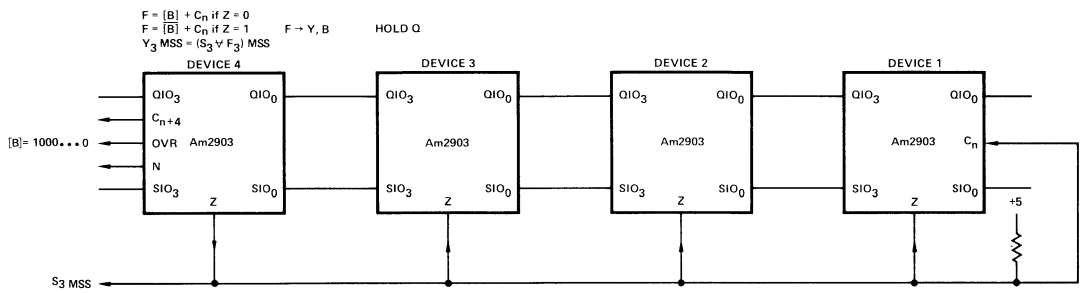


Figure 11. 2's Complement ⟷ Sign/Magnitude.

MPR-045

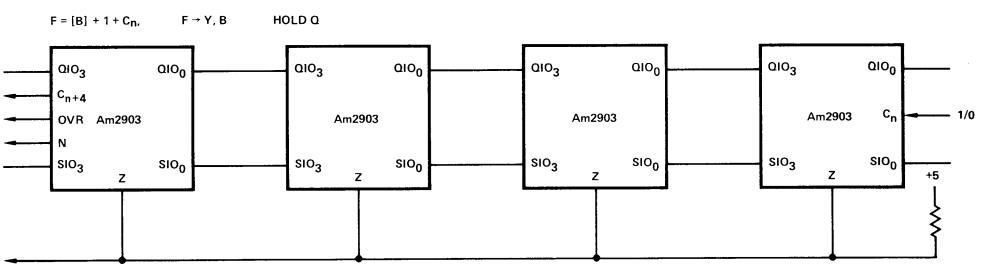


Figure 12. Increment by 2/1.

MPR-046

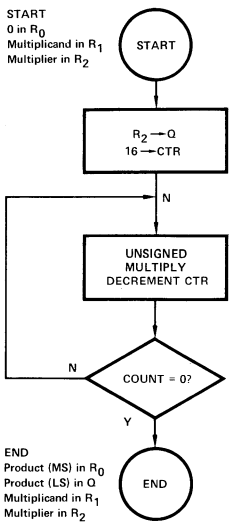


Figure 13. Unsigned 16 X 16 Multiply Flowchart.

tiplicand (referenced by the A address port) if Z = 1. If Z = 0, the output of the ALU is simply the partial product (referenced by the B address port). Since C_n is held LOW, it is not a factor in the computation. Each positive-going edge of the clock will internally shift the ALU outputs toward the least significant bit and simultaneously store the shifted results in the register selected by the B address port, thus becoming the new partial sum. During the down shifting process, the C_{n+4} generated in device 4 is internally shifted into the Y_3 position of device 4. At this time, one bit of the multiplier will down shift out of the QIO_0 ports of each device into the QIO_3 port of the next less significant slice. The partial product is shifted down between chips in a like manner, between the SIO_0 and SIO_3 ports, with SIO_0 of device 1 being connected to QIO_3 of device 4 for purposes of constructing a 32-bit long register to hold the 32-bit product. At the finish of the 16 x 16 multiply, the most significant 16 bits of the product will be found in the register referenced by the B address lines while the least significant 16 bits are stored in the Q Register. Using a typical Computer Control Unit (CCU), as shown in Figure 16, the unsigned multiply operation requires only two lines of microcode, as shown in Figure 17, and is executed in 17 microcycles.

Two's Complement Multiplication

The algorithm for two's complement multiplication is illustrated by Figure 14. The initial conditions for two's complement multiplication are the same as for the unsigned multiply operation. The Two's Complement Multiply Command is applied for 15 clock cycles in the case of a 16 x 16 multiply. During the down shifting process the term N∀OVR generated in device 4 is internally shifted into the Y_3 position of device 4. The data flow shown in Figure 15 is still valid. After 15 cycles, the sign bit of the multiplier is present at the Z output of device 1. At this time, the user must place the Two's Complement Multiply Last cycle command on the instruction lines. The interconnection for this instruction is shown in Figure 18. On the next positive edge of the clock, the Am2903 will adjust the partial product, if the sign of the multiplier is negative, by subtracting out the two's complement representation of the multiplicand. If the sign bit is positive, the partial product is not adjusted. At this point, two's complement multiplication is completed. Using a typical CCU, as shown in Figure 16, the two's complement multiply operation requires only three lines of microcode, as shown in Figure 19, and is executed in 17 microcycles.

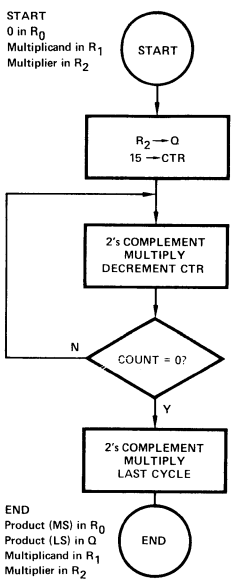
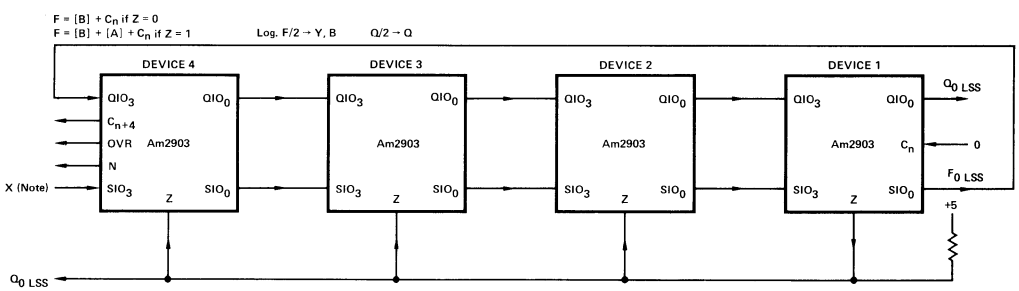


Figure 14. 2's Complement 16 X 16 Multiply.



Note: For unsigned multiply, C_{n+4} MSS is internally shifted into position Y_3 MSS; 2's complement multiply N∀OVR is internally shifted into position Y_3 MSS.

Figure 15. Multiply.

MPR-049

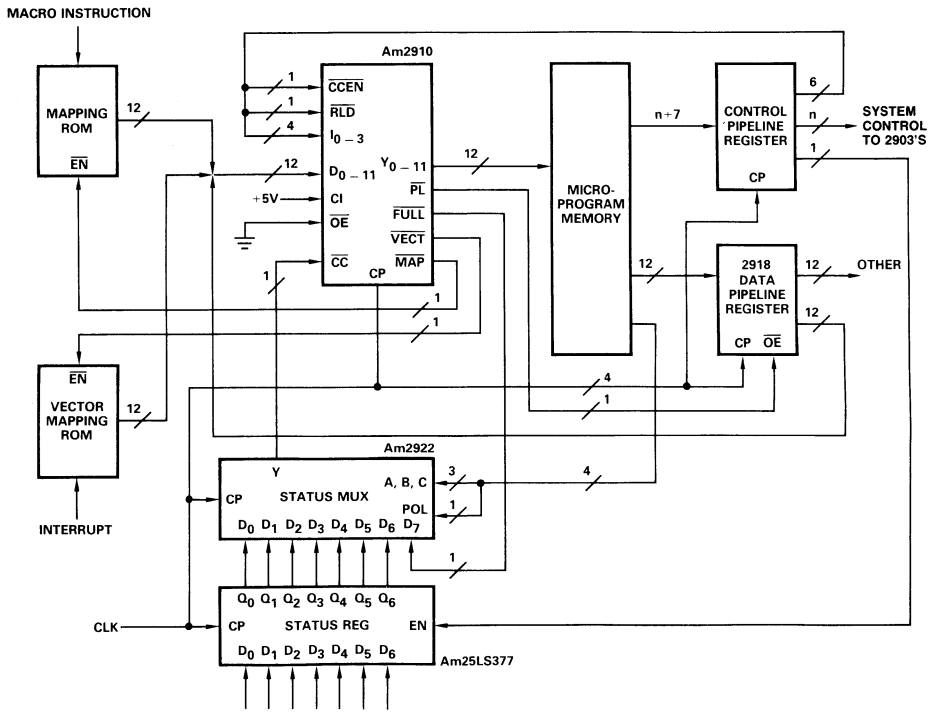
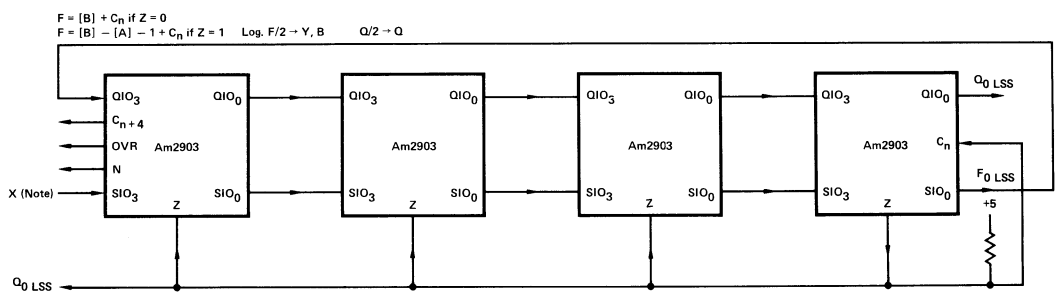


Figure 16. Typical Computer Control Unit (CCU).

MPR-050

Micro Memory Address	Am2910 Inst	Data Pipeline Reg.	I_0	I_4-I_1	I_8-I_5	$\overline{OEB}$	$\overline{OEY}$	A_3-A_0	B_3-B_0	C_n	Comment
n	LDCT	$00F_{16}$	X	6	6	X	X	R_2	X	0	Load Counter & $R_2 \rightarrow Q$
n+1	RPCT	n+1	0	0	0	0	0	R_1	R_0	0	Unsigned Multiply

Figure 17. Micro Code for Unsigned 16 X 16 Multiply.



Note: N ∀ OVR is internally shifted into position Y_3 MSS.

Figure 18. 2's Complement Multiply, Last Cycle.

MPR-051

Memory Address	Am2910 Inst	Data Pipeline Reg.	I_0	$I_4 - I_1$	$I_8 - I_5$	$\overline{OEB}$	$\overline{OEY}$	$A_3 - A_0$	$B_3 - B_0$	C_n	Comment
n	LDCT	$00E_{16}$	X	6	6	X	X	R_2	X	0	Load Counter & $R_2 \rightarrow Q$
n+1	RPCT	n+1	0	0	2	0	0	R_1	R_0	0	2's Complement Multiply
n+2	X	X	0	0	6	0	0	R_1	R_0	Z	2's Complement Multiply (Last Cycle)

Figure 19. Microcode for 2's Complement 16 x 16 Multiply.

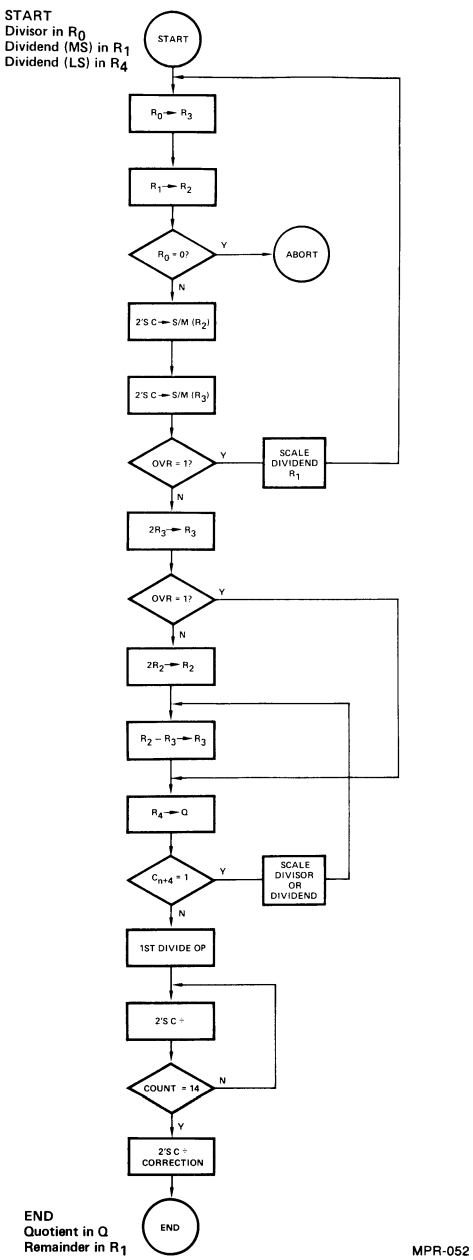


Figure 20. Division Flow Chart — Double Precision Divide.

TWO'S COMPLEMENT DIVISION

The division process is accomplished using a four quadrant non-restoring algorithm which yields an algebraically correct answer such that the divisor times the quotient plus the remainder equals the dividend. The algorithm works for both single precision and multi-precision divide operations. The only condition that needs to be met is that the absolute magnitude of the divisor be greater than the absolute magnitude of the dividend. For multi-precision divide operations the least significant bit of the dividend is truncated. This is necessary if the answer is to be algebraically correct. Bias correction is automatically provided by forcing the least significant bit of the quotient to a one, yet an algebraically correct answer is still maintained. Once the algorithm is completed, the answer may be modified to meet the user's format requirements, such as rounding off or converting the remainder so that its sign is the same as the dividend. These format modifications are accomplished using the standard Am2903 instructions.

The true value of the remainder is equal to the value stored in the working register times 2^{n-1} when n is the number of quotient digits.

The following paragraphs describe a double precision divide operation. The double precision flow chart is based upon the use of the architecture detailed in Figure 16.

Referring to the flow chart outlined in Figure 20, we begin the algorithm with the assumption that the divisor is contained in R_0, while the most significant and least significant halves of the dividend reside in R_1 and R_4 respectively. The first step is to duplicate the divisor by copying the contents of R_0 into R_3. Next the most significant half of the dividend is copied by transferring the contents of R_1 into R_2 while simultaneously checking to ascertain if the divisor (R_0) is zero. If the divisor is zero then division is aborted. If the divisor is not zero, the copy of the most significant half of the dividend in R_2 is converted from its two's complement to its sign magnitude representation. The divisor in R_3 is converted in like manner in the next step, while testing to see if the results of the dividend conversion yielded an indication on the overflow pin of the Am2903. If the output of the overflow pin is a 'one' then the dividend is -2^n and hence is the largest possible number, meaning that it cannot be less than the divisor. What must be done in this case is to scale the dividend by down shifting the upper and lower halves stored in R_1 and R_4 respectively. After scaling, the routine requires that the algorithm be reinitiated at the beginning.

Conversely, if the output of the overflow pin is not a one, the sign magnitude representation of the divisor (R_3) is shifted up in the Am2903, removing the sign while at the same time testing the results of two's complement to sign magnitude conversion of the divisor in the Am2910. If the results of the test indicate that the divisor is -2^n i.e., overflow equals one, then the lower half of the dividend is placed in the Q register

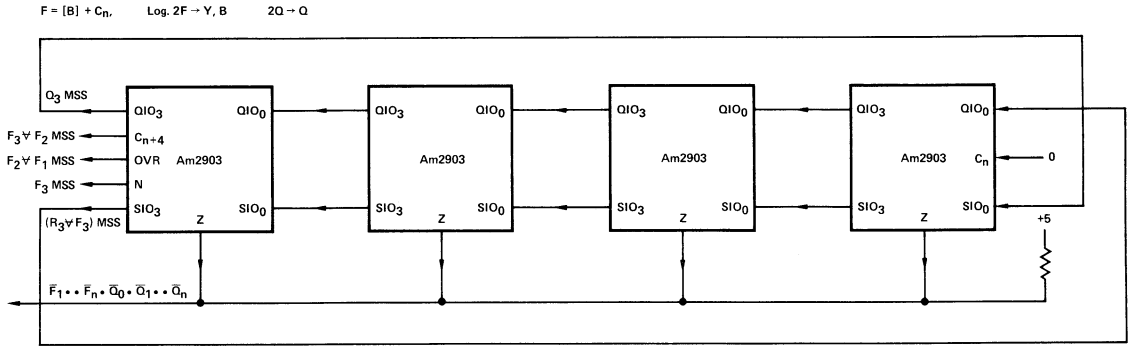


Figure 21. Double Length Normalize/First Divide Operation.

MPR-053

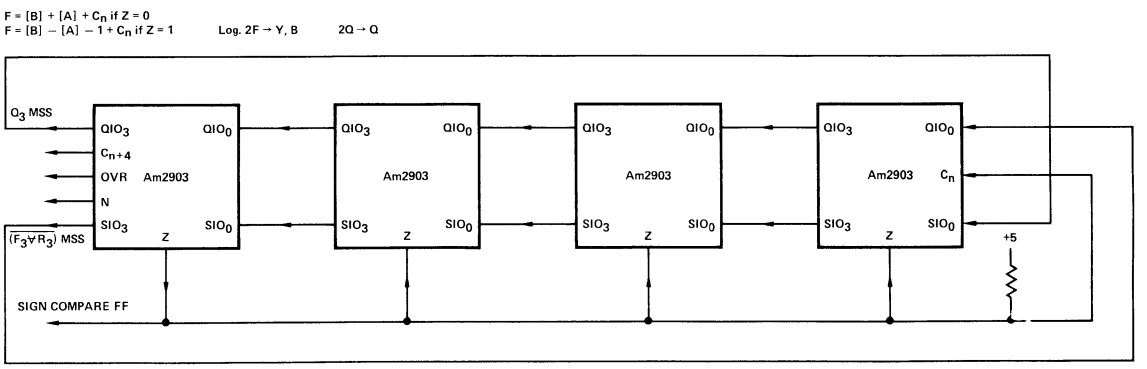


Figure 22. 2's Complement Divide.

MPR-054

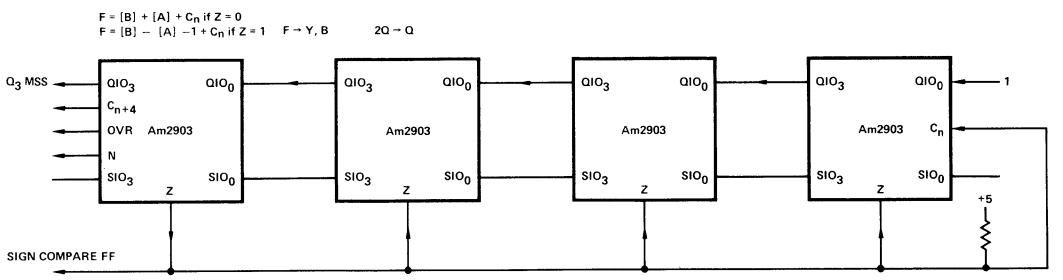


Figure 23. 2's Complement Divide Correction.

MPR-055

and division may proceed. This is possible because the divisor is now guaranteed to be greater than the dividend. If overflow is not a one then we must proceed by shifting out the sign of the sign magnitude representation of the dividend stored in R_2. At this point we are able to check if the divisor is greater than the dividend by subtracting the absolute value of the divisor (R_3) from the absolute value of the upper half of the dividend (R_2) and storing the results in R_3. Next, the least significant half of the dividend is transferred from R_4 to the Q register while simultaneously testing the carry from the result of the divisor/dividend subtraction. If the carry (C_{n+4}) is one, indicating the divisor is not greater than the dividend then a scaling operation must occur. This involves either shifting up the divisor or shifting down the dividend. If the carry is not one then the divisor is greater than the dividend and division may now begin.

Micro Memory Address	Am2910 Inst.	Data Pipeline Reg.	Am2903 I_0	I_4-I_1	I_8-I_5	$\overline{EA}$	A_3-A_0	B_3-B_0	C_n	Am2922 SEL	POL	Am29LS18 $\overline{E}$	Comment
n	CONT	X	0	6	4	0	R_0	R_3	0	X	X	0	$R_0 \rightarrow R_3$
n+1	CJP	Abort	0	6	4	0	R_1	R_2	0	Z	1	X	$R_1 \rightarrow R_2$, if $R_0 = 0$ Abort
n+2	CONT	X	0	0	5	X	X	R_2	0	X	X	0	2's C to S/M (R_2)
n+3	CJP	Scale Dividend	0	0	5	X	X	R_3	0	OVR	1	0	2's C to S/M (R_3), if OVR ≥ 1, scale
n+4	CJP	n+7	0	4	9	X	X	R_2	0	OVR	1	X	Shift out sign of divisor
n+5	CONT	X	0	4	9	X	X	R_3	0	X	X	X	Shift out sign of divisor
n+6	CONT	X	0	2	F	0	R_2	R_3	1	X	X	0	Dividend − Divisor $\rightarrow R_3$
n+7	CJP	Scale Dividend or Divisor	0	6	6	0	R_4	X	0	C_{n+4}	0	X	$R_4 \rightarrow Q$, if Carry = 1, scale
n+8	PUSH	$00D_{16}$	0	0	A	0	R_0	R_1	0	0	1	X	Loop set up & First Divide Operation
n+9	RFCT	X	0	0	C	0	R_0	R_1	Z	X	X	X	Test Loop Count & 2's C Divide
n+A	CONT	X	0	0	E	0	R_0	R_1	Z	X	X	X	2's C Divide Correction

Figure 24. Microcode for Double Precision Divide.

The first divide operation is used to ascertain the sign bit of the quotient. The two's complement divide instruction is then executed repetitively, fourteen times in the case of a sixteen bit divisor and a thirty-two bit dividend. The final step is the two's complement correction command which adjusts the quotient by allowing the least significant bit of the quotient to be set to one. At the end of the division algorithm the sixteen bit quotient is found in the Q register while the remainder now replaces the most significant half of the dividend in R_1. It should be noted that the remainder must be shifted down fifteen places to represent its true value. The interconnections for these instructions are shown in Figures 21, 22, 23. Using a typical CCU as shown in Figure 16, the double precision divide operation requires only eleven lines of microcode, as shown in Figure 24.

For those applications that require truncation instead of bias correction, the same algorithm as above should be implemented except one additional Two's Complement Divide instruction should be used in lieu of the Two's Complement Divide Correction and Remainder instruction. However, this technique results in an invalid remainder.

It is possible to do multiple-precision divide operations beyond the double precision divide shown above. For example, to do a triple precision divide for a 16-bit CPU, the upper two thirds of the dividend are stored in R_1 and Q as in the case for double precision divide. The lower third of the dividend is stored in a scratch register, R_5. After checking that the magnitude of the divisor is greater than the magnitude of the dividend, using the same tests as defined in Figure 20, the procedure is as follows:

1. Execute a Double Length Normalize/First Divide Operation instruction.
2. Execute the Two's Complement Divide instruction fifteen times.
3. Transfer the contents of Q, the most significant half of the quotient, to R_2.
4. Transfer R_5 to Q.
5. Execute the Two's Complement Divide instruction fifteen times.
6. Execute the Two's Complement Divide Correction and Remainder instruction.

The upper half of the quotient is then in R_2, the lower half of the quotient is in Q and the remainder is in R_1. The flow chart for this is shown in Figure 25. This technique can be expanded for any precision which is required.

Byte Swap

The multi-port architecture of the Am2903 allows for easy implementation of high- and low-order byte swapping. Figure 26 outlines a byte swap implementation utilizing two data ports. Initially, the lower order 8-bit byte is stored in devices 1 and 2, while the high-order byte is in devices 3 and 4. When the user wishes to exchange the two bytes, the register location of the desired word is placed on the B address port. When the byte swap line is brought LOW, the bytes to be swapped will be flowing from the DB ports of the Am2903 through the Am25LS240/244 Three-state Buffers. The outputs of the

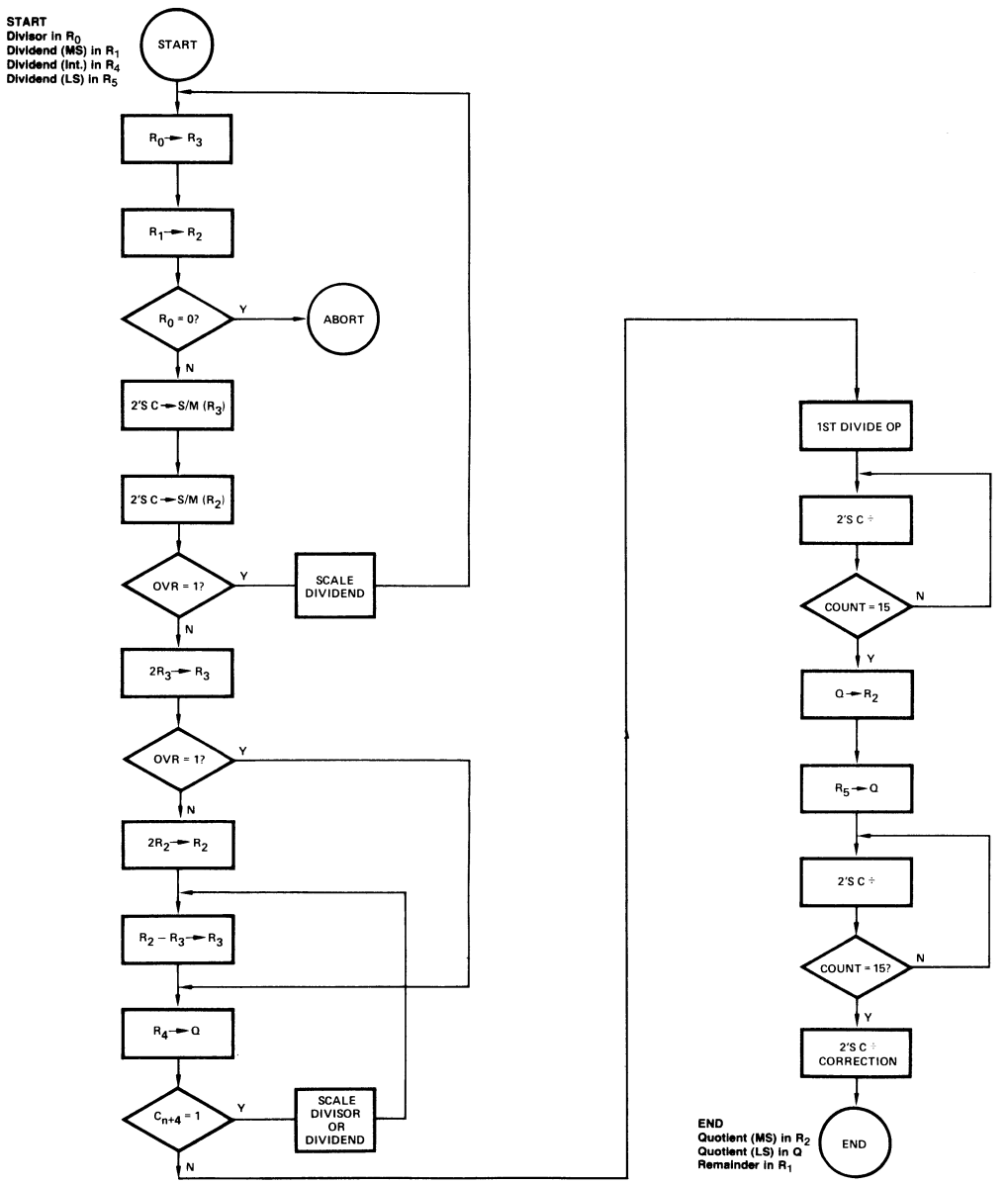


Figure 25. Division Flow Chart – Triple Precision Divide.

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three-state buffers are permuted such that the byte swap is achieved. The resultant permuted data is presented to the DA ports of the Am2903 where it is re-loaded into the memories of the Am2903 on the next positive edge of CP using the source and function commands of $F = \overline{A}$ plus C_n (C_n = 0) for the Am25LS240 or F = A plus C_n (C_n = 0) for the Am25LS244 and the destination command F→Y, B.

A higher speed technique for achieving the byte swap operation is illustrated in Figure 27. Instead of inputting the permuted data via the DA ports, the permuted data is inputted via the Y input/output ports with $\overline{OE}_Y$ held HIGH. This technique bypasses the ALU, thus allowing faster operation. The Am2903 destination command F → Y, B should be used.

Memory Expansion

The Am2903 allows for a theoretically infinite memory expansion. Figure 28 pictures a 4-bit slice of a system which has 48 words of RAM and 16 words of ROM. RAM storage is provided by the Am2903 and the Am29705's. The Am29705 RAM is functionally identical to the Am2903 RAM. The Am29751A is used to store constants and masks and is addressable from address port A only. The system is organized around five data buses. Inter-bus communication may be done through the Am29705's or the Am2903. The memory addressing scheme specifies the data source for the R input of the ALU eminating from the register locations specified by address field A. A_{0-3} addresses 16 memory locations in each chip while address bits A_{4-6} are decoded and used for the output enable for the desired chip. The B address field is used to select the S input of the ALU and the C field is used to specify the register location where the result of the ALU operation is to be stored.

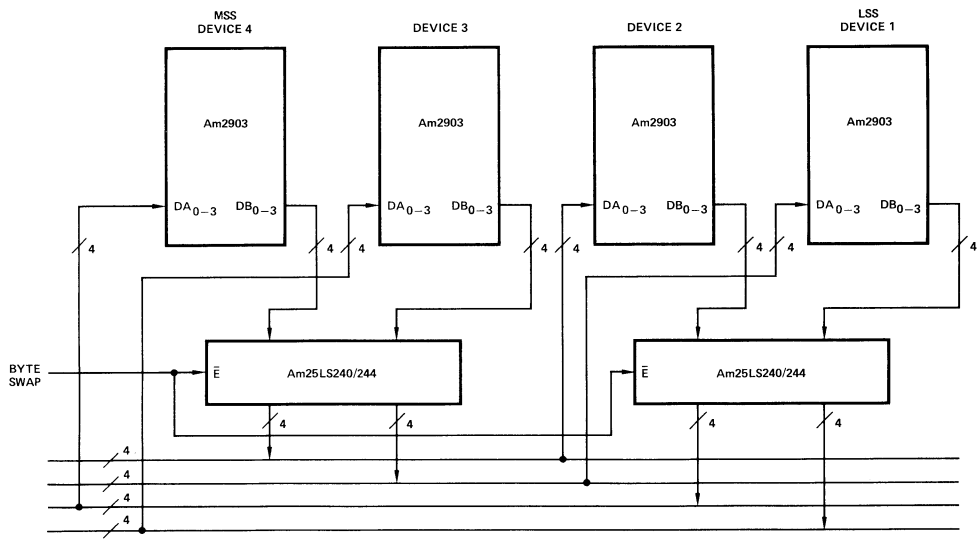

Figure 26. Byte Swap.

MPR-057

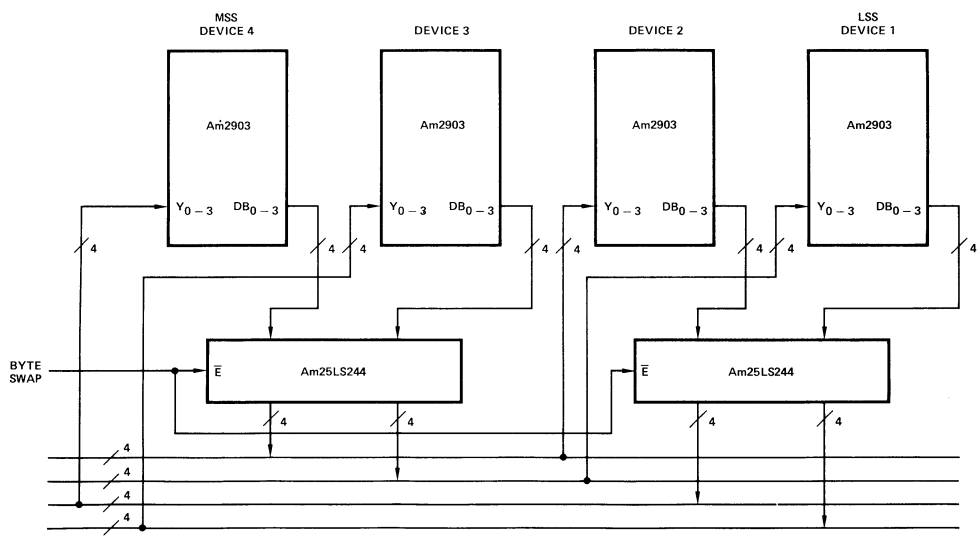

Figure 27. High Speed Byte Swap.

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Bits B_{0-3} are for source register addressing in each chip. Bits B_4 and B_5 are used for chip output enable selection. C_{0-3} access the 16 destination addresses on each chip while bits C_4 and C_5 control the Write Enable of the desired chip. The source and destination register address are multiplexed such that when the clock is HIGH, the source register address is presented to the B address ports of the RAM's. The Instruction Enable ($\overline{IEN}$) is HIGH at this time. The data flows from the Y port or the internal B port as selected by the decoder whose inputs are B_4 and B_5. When the clock goes LOW, the data eminating from the selected Y outputs of the Am29705's and the RAM outputs of the Am2903 are latched and the destination address is now selected for use by the RAM address lines. When the destination address stabilizes on the address lines, the $\overline{IEN}$ pin is brought LOW. The $\overline{WRITE}$ output of the Am2903 will now go LOW, enabling the decoder sourced by address bits C_4 and C_5. The selected decoder line will go LOW, allowing the desired memory location to be written into. To switch between two- and three-address architecture, the user simply makes the source and destination addresses the same; i.e., $B_{0-3} = C_{0-3}$ and $B_{4-5} = C_{4-5}$. For two-address architecture, the MUX is removed from the circuit.

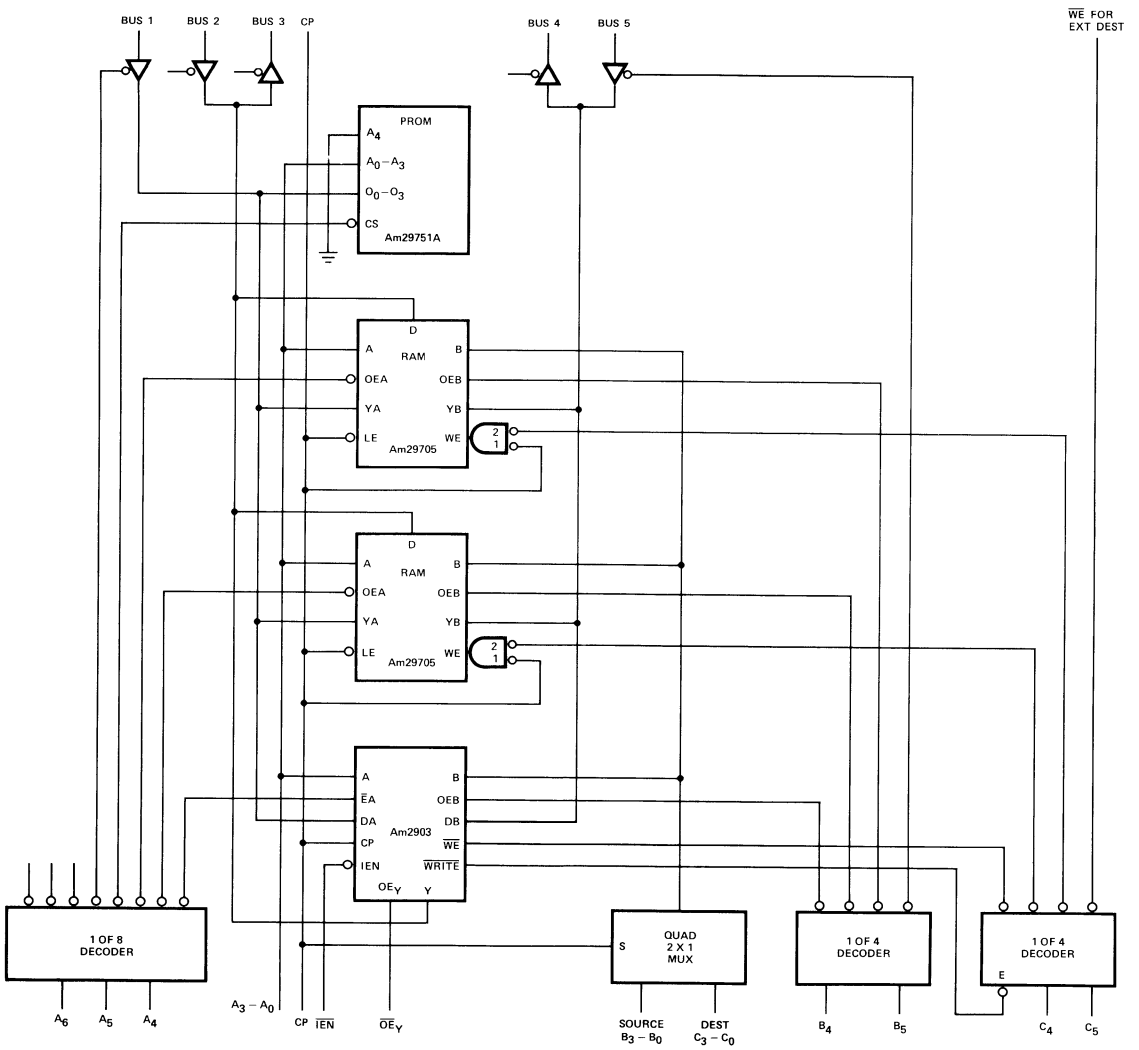

Figure 28. Expanded Memory.

MPR-059

Am2940 – DMA Address Generator
Am2942 – Timer/Counter

Revised December, 1978

viously called the
sheet contained
rect pin-out has

Am2942
Programmable Timer/Counter
DMA Address Generator
ADVANCED INFORMATION

ERISTICS
40 –
Address and Data lines plus addi-
and Instruction Enable pins.
DMA Address Generator or Pro-

lus eight Timer/Counter instruc-

programmable 8-bit up/down

to form single-chip 16-bit

from on-chip

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GENERAL DESCRIPTION
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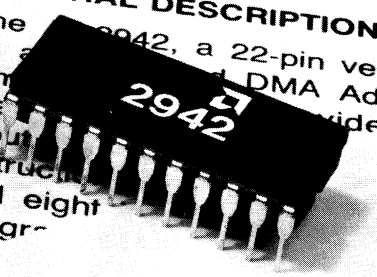


Am2940
DMA Address Generator
PRELIMINARY DATA

S

count and DONE sig

larger

ERAL DESCRIPTION
a 28-pin membe
Low-Power
dable, eig
or slice. A
arger add
function
The pin
memory addresses f
memory. It
sig

ADVANCED MICRO DEVICES INC.,
901 Thompson Place, Sunnyvale, California 94085 (408) 732-2400 TWX: 910-339-9280 TELEX: 34-6306 TOLL FREE: (800) 538-8450

Introducing the Am2940 and Am2942: Two 8-bit up-down counters in a single chip.

The Am2940: The perfect part for High-speed DMA Controllers

The Am2940 provides both an address counter and a word counter for DMA applications. Each counter can be preset and can be incremented, decremented, or held on each clock. The 2940 is a cascadable 8-bit slice and it includes "transfer complete" logic for four different DMA modes. The Am2940 is available at your local AMD distributor.

The Am2942: Counters go LSI

The Am2942 is designed to replace up to four general purpose MSI counters with a single LSI part. Each 2942 contains two independent 8-bit presettable up-down counters. They can be cascaded with other 2942s or the two counters in one chip can be cascaded to form a 16-bit counter in one part. The Am2942 is available at your local AMD distributor.

AM-PUB076 Rev. 1

Am2940
DMA Address Generator

DISTINCTIVE CHARACTERISTICS

- DMA Address Generation
  Generates memory address, word count and DONE signal for DMA transfer operation.
- Expandable Eight-bit Slice
  Any number of Am2940's can be cascaded to form larger memory addresses – three devices address 16 megawords.
- Repeat Data Transfer Capability
  Initial memory address and word count are saved so that the data transfer can be repeated.
- Programmable Control Modes
  Provides four types of DMA transfer control plus memory address increment/decrement.
- High Speed, Bipolar LSI
  Advanced Low-Power Schottky TTL technology provides typical CLOCK to DONE propagation delay of 50ns and 24mA output current sink capability.
- Microprogrammable
  Executes 8 different instructions.

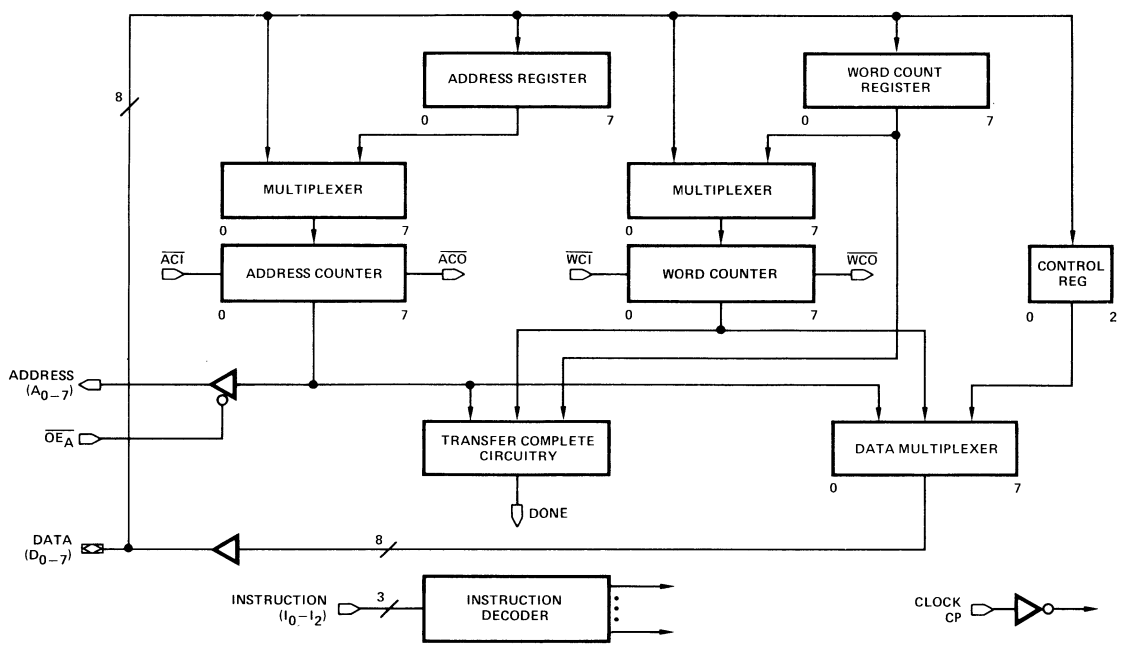
GENERAL DESCRIPTION

The Am2940, a 28-pin member of Advanced Micro Devices Am2900 family of Low-Power Schottky bipolar LSI chips, is a high-speed, cascadable, eight-bit wide Direct Memory Access Address Generator slice. Any number of Am2940's can be cascaded to form larger addresses.

The primary function of the device is to generate sequential memory addresses for use in the sequential transfer of data to or from a memory. It also maintains a data word count and generates a DONE signal when a programmable terminal count has been reached. The device is designed for use in peripheral controllers with DMA capability or in any other system which transfers data to or from sequential locations of a memory.

The Am2940 can be programmed to increment or decrement the memory address in any of four control modes, and executes eight different instructions. The initial address and word count are saved internally by the Am2940 so that they can be restored later in order to repeat the data transfer operation.

BLOCK DIAGRAM



Am2940 DMA Address Generator

MPR-226

Am2940 ARCHITECTURE

As shown in the Block Diagram, the Am2940 consists of the following:

- A three-bit Control Register.
- An eight-bit Address Counter with input multiplexer.
- An eight-bit Address Register.
- An eight-bit Word Counter with input multiplexer.
- An eight-bit Word Count Register.
- Transfer complete circuitry.
- An eight-bit wide data multiplexer with three-state output buffers.
- Three-state address output buffers with external output enable control.
- An instruction decoder.

Control Register

Under instruction control, the Control Register can be loaded or read from the bidirectional DATA lines D_0-D_7. Control Register bits 0 and 1 determine the Am2940 Control Mode, and bit 2 determines whether the Address Counter increments or decrements. Figure 1 defines the Control Register format.

Address Counter

The Address Counter, which provides the current memory address, is an eight-bit, binary, up/down counter with full look-ahead carry generation. The Address Carry input ($\overline{ACI}$) and Address Carry Output ($\overline{ACO}$) allow cascading to accommodate larger addresses. Under instruction control, the Address Counter can be enabled, disabled, and loaded from the DATA inputs, D_0-D_7, or the Address Register. When enabled and the $\overline{ACI}$ input is LOW, the Address Counter increments/decrements on the LOW to HIGH transition of the CLOCK input, CP. The Address Counter output can be enabled onto the three-state ADDRESS outputs A_0-A_7 under control of the Output Enable input, $\overline{OE}_A$.

Address Register

The eight-bit Address Register saves the initial address so that it can be restored later in order to repeat a transfer operation. When the LOAD ADDRESS instruction is executed, the Address Register and Address Counter are simultaneously loaded from the DATA inputs, D_0-D_7.

Word Counter and Word Count Register

The Word Counter and Word Count Register, which maintain and save a word count, are similar in structure and operation to the Address Counter and Address Register, with the exception that the Word Counter increments in Control Modes 1 and 3, decrements in Control Mode 0, and is disabled in Control Mode 2. The LOAD WORD COUNT instruction simultaneously loads the Word Counter and Word Count Register.

Transfer Complete Circuitry

The Transfer Complete Circuitry is a combinational logic network which detects the completion of the data transfer operation in three Control Modes and generates the DONE output signal. The DONE signal is a open-collector output, which can be dot-anded between chips.

Data Multiplexer

The Data Multiplexer is an eight-bit wide, 3-input multiplexer which allows the Address Counter, Word Counter, and Control Register to be read at the DATA lines, D_0-D_7. The Data Multiplexer and three-state Data output buffers are instruction controlled.

Address Output Buffers

The three-state Address Output Buffers allow the Address Counter output to be enabled onto the ADDRESS lines, A_0-A_7, under external control. When the Output Enable input, $\overline{OE}_A$, is LOW, the Address output buffers are enabled; when $\overline{OE}_A$ is HIGH, the ADDRESS lines are in the high-impedance state. The address and Data Output Buffers can sink 24mA output current over the commercial operating range.

Instruction Decoder

The Instruction Decoder generates required internal control signals as a function of the INSTRUCTION inputs, I_0-I_2 and Control Register bits 0 and 1.

Clock

The CLOCK input, CP is used to clock the Address Register, Address Counter, Word Count Register, Word Counter, and Control Register, all on the LOW to HIGH transition of the CP signal.

Control Register

CR_2	CR_1	CR_0

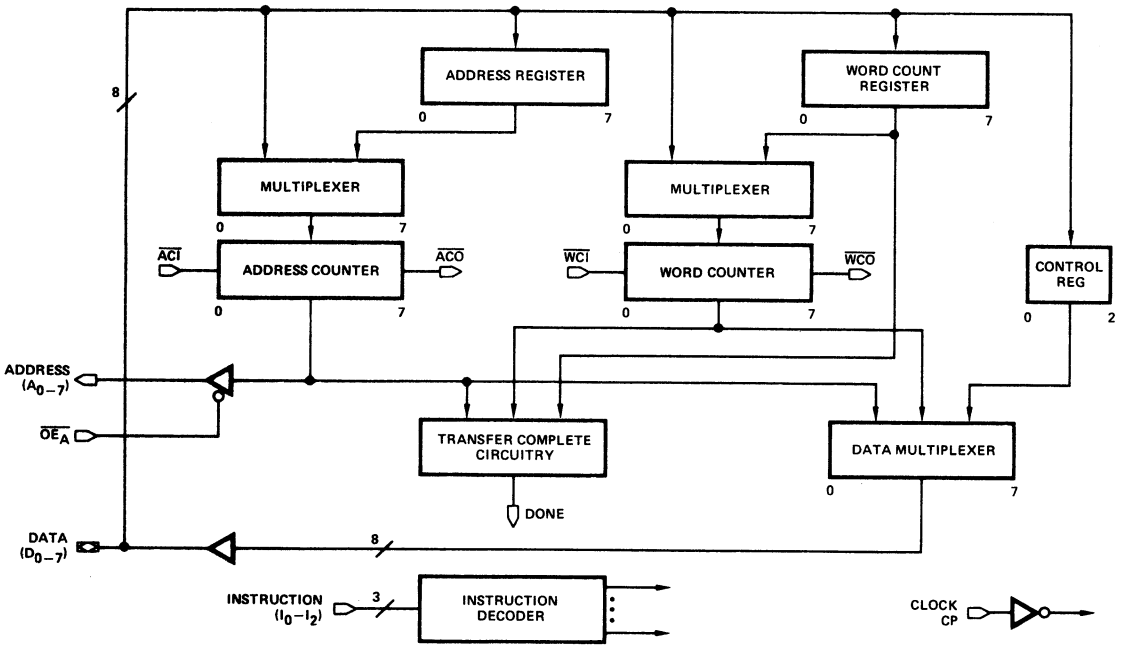
CR_1	CR_0	Control Mode Number	Control Mode Type	Word Counter	DONE Output Signal	
					$\overline{WCI}$ = LOW	$\overline{WCI}$ = HIGH
L	L	0	Word Count Equals Zero	Decrement	HIGH when Word Counter = 1	HIGH when Word Counter = 0
L	H	1	Word Count Compare	Increment	HIGH when Word Counter + 1 = Word Count Reg.	HIGH when Word Counter = Word Count Reg.
H	L	2	Address Compare	Hold	HIGH when Word Counter = Address Counter	
H	H	3	Word Counter Carry Out	Increment	Always LOW	

CR_2	Address Counter
L	Increment
H	Decrement

H = HIGH
L = LOW

Figure 1. Control Register Format Definition.

BLOCK DIAGRAM



Am2940 DMA Address Generator

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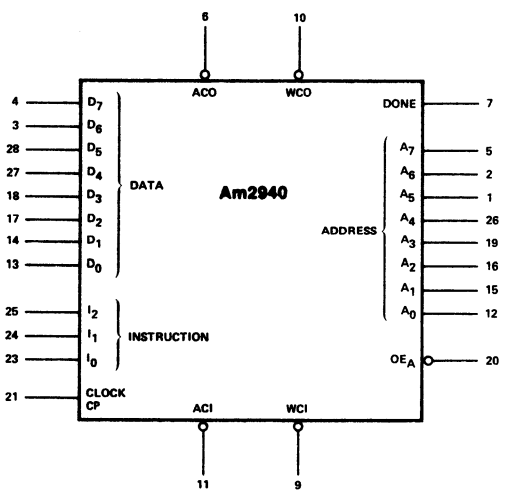
LOGIC SYMBOL



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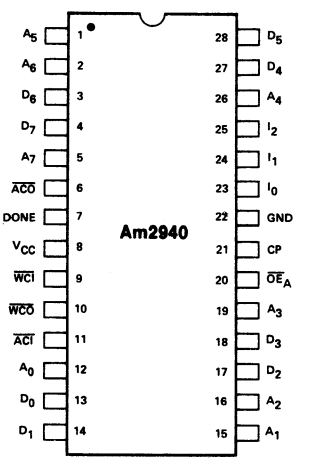
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation

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Am2940 CONTROL MODES

Control Mode 0 – Word Count Equals Zero Mode

In this mode, the LOAD WORD COUNT instruction loads the word count into the Word Count Register and Word Counter. When the Word Counter is enabled and the Word Counter Carry-in, $\overline{WCI}$, is LOW, the Word Counter increments on the LOW to HIGH transition of the clock input, CP. Figure 1 specifies when the DONE signal is generated.

Control Mode 1 – Word Count Compare Mode

In this mode the LOAD WORD COUNT instruction loads the word count into the Word Count Register and clears the Word Counter. When the Word Counter is enabled and the Word Counter Carry-in $\overline{WCI}$, is LOW, the Word Counter increments on the LOW to HIGH transition of the clock input, CP. Figure 1 specifies when the DONE signal is generated.

Control Mode 2 – Address Compare Mode

In this mode, only an initial and final memory address need be specified. The initial Memory Address is loaded into the Address Register and Address Counter and the final memory address is loaded into the Word Count Register and Word Counter. The Word Counter is always disabled in this mode and serves as a holding register for the final memory address. When the Address Counter is enabled and the $\overline{ACI}$ input is LOW, the Address Counter increments or decrements (depending on Control Register bit 2) on the LOW to HIGH transition of the CLOCK input, CP. The Transfer Complete Circuitry compares the Address Counter with the Word Counter and generates the DONE signal during the last word transfer, i.e. when the Address Counter equals the Word Counter.

Control Mode 3 – Word Counter Carry Out Mode

For this mode of operation, the user can load the Word Count Register and Word Counter with the two's complement of the number of data words to be transferred. When the Word Counter is enabled and the $\overline{WCI}$ input is LOW, the Word Counter increments on the LOW to HIGH transition of the CLOCK input, CP. A Word Counter Carry Out signal, $\overline{WCO}$, indicates the last data word is being transferred. The DONE signal is not required in this mode and, therefore, is always LOW.

Am2940 INSTRUCTIONS

The Am2940 instruction set consists of eight instructions. Six instructions load and read the Address Counter, Word Counter and Control Register, one instruction enables the Address and Word counters, and one instruction reinitializes the Address and Word Counters. The function of the REINITIALIZE COUNTERS, LOAD WORD COUNT, and ENABLE COUNTERS instructions varies with the Control Mode being utilized. Table 1 defines the Am2940 Instructions as a function of Instruction inputs I_0-I_2 and the four Am2940 Control Modes.

The WRITE CONTROL REGISTER instruction writes DATA input D_0-D_2 into the Control Register; DATA inputs D_3-D_7 are "don't care" inputs for this instruction. The READ CONTROL REGISTER instruction gates the Control Register outputs to DATA lines, D_0-D_2. DATA lines D_3-D_7 are in the HIGH state during this instruction.

The Word Counter can be read using the READ WORD COUNTER instruction, which gates the Word Counter outputs to DATA lines D_0-D_7. The LOAD WORD COUNT instruction is Control Mode dependent. In Control Modes 0, 2, and 3, DATA inputs D_0-D_7 are written into both the Word Count Register and Word Counter. In Control Mode 1, DATA inputs D_0-D_7 are written into the Word Count Register and the Word Counter is cleared.

The READ ADDRESS COUNTER instruction gates the Address Counter outputs to DATA lines D_0-D_7, and the LOAD ADDRESS instruction writes DATA inputs D_0-D_7 into both the Address Register and Address Counter.

In Control Modes 0, 1, and 3, the ENABLE COUNTERS instruction enables both the Address and Word Counters; in Control Mode 2, the Address Counter is enabled and the Word Counter holds its contents. When enabled and the carry input is active, the counters increment on the LOW to HIGH transition of the CLOCK input, CP. Thus, with this instruction applied, counting can be controlled by the carry inputs.

The REINITIALIZE COUNTERS instruction also is Control Mode dependent. In Control Modes 0, 2, and 3, the contents of the Address Register and Word Count Register are transferred to the respective Address Counter and Word Counter; in Control Mode 1, the content of the Address Register is transferred to the Address Counter and the Word Counter is cleared. The REINITIALIZE COUNTERS instruction allows a data transfer operation to be repeated without reloading the address and word count from the DATA lines.

TABLE I. Am2940 INSTRUCTIONS

I_2 I_1 I_0	Octal Code	Function	Mnemonic	Control Mode	Word Reg.	Word Counter	Address Reg.	Address Counter	Control Register	Data D_0-D_7
L L L	0	WRITE CONTROL REGISTER	WRCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	D_0-D_2→CR	INPUT
L L H	1	READ CONTROL REGISTER	RDCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	CR→D_0-D_2 (Note 1)
L H L	2	READ WORD COUNTER	RDWC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	WC→D
L H H	3	READ ADDRESS COUNTER	RDAC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	AC→D
H L L	4	REINITIALIZE COUNTERS	REIN	0, 2, 3	HOLD	WCR→WC	HOLD	AR→AC	HOLD	Z
				1	HOLD	ZERO→WC	HOLD	AR→AC	HOLD	Z
H L H	5	LOAD ADDRESS	LDAD	0, 1, 2, 3	HOLD	HOLD	D→AR	D→AC	HOLD	INPUT
H H L	6	LOAD WORD COUNT	LDWC	0, 2, 3	D→WR	D→WC	HOLD	HOLD	HOLD	INPUT
				1	D→WR	ZERO→WC	HOLD	HOLD	HOLD	INPUT
H H H	7	ENABLE COUNTERS	ENCT	0, 1, 3	HOLD	ENABLE COUNT	HOLD	ENABLE COUNT	HOLD	Z
				2	HOLD	HOLD	HOLD	ENABLE COUNT	HOLD	Z

CR = Control Reg.
AR = Address Reg.
AC = Address Counter
WCR = Word Count Reg.
WC = Word Counter
D = Data
L = LOW
H = HIGH
Z = High Impedance

Note 1:
Data Bits D_3-D_7 are high during this instruction.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

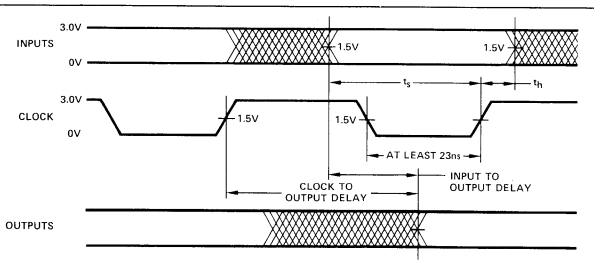
OPERATING RANGE

P/N	Range	Temperature	V_{CC}	
Am2940PC, DC	COM'L	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5%	(MIN. = 4.75V MAX. = 5.25V)
Am2940DM, FM	MIL	T_C = −55° to +125°C	V_{CC} = 5.0V ±10%	(MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}		MIL I_{OH} = −1.0mA COM'L I_{OH} = −2.6mA	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL} (Note 5)	WCO, ACO	MIL I_{OL} = 8.0mA COM'L I_{OL} = 12mA			0.5	Volts
			A_{0-7}, D_{0-7} DONE	MIL I_{OL} = 16mA COM'L I_{OL} = 24mA				
V_{IH}	Input HIGH Level (Note 4)	Guaranteed Input Logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Note 4)	Guaranteed Input Logical LOW voltage for all inputs					0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V		D_{0-7} All Others			−0.15 −0.8	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V		D_{0-7} All Others			150 40	μA
I_{CEX}	Output Leakage on DONE	V_{CC} = MAX., V_O = 5.5V					250	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX. + 0.5V, V_O = 0.5V			−30		−85	mA
I_{OZL} I_{OZH}	Output OFF Current	V_{CC} = MAX. $\overline{OE}$ = 2.4V	V_{OUT} = 0.5V	A_{0-7} D_{0-7}			−50 −150	μA
			V_{OUT} = 2.4V	A_{0-7} D_{0-7}			50 150	
I_{CC}	Power Supply Current	V_{CC} = MAX.		T_A = 25°C		170	275	mA
			Am2940PC, DC	T_A = 0°C to +70°C			290	
				T_A = +70°C			235	
			Am2940DM, FM	T_C = −55°C to +125°C			315	
				T_C = +125°C			225	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide no guaranteed noise immunity and should only be tested in a static-, noise-free environment.
5. I_{OL} limit on A_i and D_i (i = 0 to 7) applies to either output individually, but not both at the same time. The sum of the loading on A_i plus D_i is limited to 24mA MIL or 32mA COM'L.



See Tables A for t_s and t_h for various inputs. See Tables B for combinational delays from clock and other inputs to outputs.

Figure 2. Switching Waveforms.

PRELIMINARY SWITCHING CHARACTERISTICS

The tables below define the Am2940 switching characteristics. Tables A are set-up and hold times relative to the clock LOW-to-HIGH transition. Tables B are combinational delays. Tables C are clock requirements. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns with C_L = 50pF except output disable times ($\overline{OE}$ to A and I to D) which are specified for a 5pF load. All times are in ns.

I. TYPICAL ROOM TEMPERATURE CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	13	3
I_{012}	33	2
$\overline{ACI}$	15	2
$\overline{WCI}$ (Note 1)	15	1

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	A_{0-7}	DONE	D_{0-7}
$\overline{ACI}$	12	–	–	–	–
$\overline{WCI}$ (Note 2)	–	12	–	27	–
I_{0-2}	–	–	–	–	21
CP (Note 3)	35	35	35	50	–

C. Clock Requirements

Minimum Clock LOW Time	20	ns
Minimum Clock HIGH Time	25	ns
Maximum Clock Frequency	22	MHz

D. Enable/Disable Times

From	To	Disable	Enable	
I_{012}	D_{0-7}	25	19	ns
$\overline{OE}$	A_{0-7}	19	13	ns

II. GUARANTEED ROOM TEMPERATURE CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	21	4
I_{012}	41	3
$\overline{ACI}$	27	3
$\overline{WCI}$ (Note 1)	27	3

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	A_{0-7}	DONE	D_{0-7}
$\overline{ACI}$	18	–	–	–	–
$\overline{WCI}$ (Note 2)	–	18	–	41	–
I_{0-2}	–	–	–	–	34
CP (Note 3)	50	50	48	77	–

C. Clock Requirements

Minimum Clock LOW Time	23	ns
Minimum Clock HIGH Time	30	ns
Maximum Clock Frequency	18	MHz

D. Enable/Disable Times

From	To	Disable	Enable	
I_{012}	D_{0-7}	30	30	ns
$\overline{OE}$	A_{0-7}	23	23	ns

III. GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE
Am2940PC, DC (T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	24	5
I_{012}	46	4
$\overline{ACI}$	30	4
$\overline{WCI}$ (Note 1)	30	3

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	A_{0-7}	DONE	D_{0-7}
$\overline{ACI}$	20	–	–	–	–
$\overline{WCI}$ (Note 2)	–	20	–	46	–
I_{0-2}	–	–	–	–	37
CP (Note 3)	58	58	54	85	–

C. Clock Requirements

Minimum Clock LOW Time	23	ns
Minimum Clock HIGH Time	34	ns
Maximum Clock Frequency	17	MHz

D. Enable/Disable Times

From	To	Disable	Enable	
I_{012}	D_{0-7}	35	35	ns
$\overline{OE}$	A_{0-7}	25	25	ns

IV. GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE
Am2940DM, FM (T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	27	6
I_{012}	49	5
$\overline{ACI}$	34	5
$\overline{WCI}$ (Note 1)	34	5

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	A_{0-7}	DONE	D_{0-7}
$\overline{ACI}$	21	–	–	–	–
$\overline{WCI}$ (Note 2)	–	21	–	54	–
I_0-I_2	–	–	–	–	41
CP (Note 3)	64	64	62	88	–

C. Clock Requirements

Minimum Clock LOW Time	23	ns
Minimum Clock HIGH Time	35	ns
Maximum Clock Frequency	16	MHz

D. Enable/Disable Times

From	To	Disable	Enable	
I_{012}	D_{0-7}	42	42	ns
$\overline{OE}$	A_{0-7}	30	30	ns

Notes: 1. Control modes 0, 1, and 3 only.
2. WCI to Done occurs only in control modes 0 and 1.
3. CP to Done occurs only in control modes 0, 1, and 2.

APPLICATIONS

The Am2940 is designed for use in peripheral controllers with DMA capability or in any other system which transfers data to or from sequential locations of a memory. One or more Am2940's can be used in each peripheral controller of a distributed DMA system to provide the memory address and word count required for DMA operation.

Figure 3 shows a block diagram of an example microprogrammed DMA peripheral controller.. The Am2910 Microprogram Sequencer, Microprogram Memory, and the Microinstruction Register form the microprogram control portion of this peripheral controller. The Am2940 generates the memory address and maintains the word count required for DMA operation. An internal three-state bus provides the communication path between the Microinstruction Register, the Am2917 Data Transceivers, the Am2940, the Am2901A Microprocessor, and the Device Interface Circuitry.

The Am2940 interconnections are shown in detail in Figure 4. Two Am2940's are cascaded to generate a sixteen-bit address. The Am2940 ADDRESS and DATA output current sink capability is 24mA over the commercial operating range. This allows the Am2940's to drive the System Address Bus and Internal Three-State Bus directly, thereby eliminating the need for separate bus drivers. Three-bits in the Microinstruction Register provide the Am2940 Instruction Inputs, I_0-I_2. The microprogram clock is used to clock the Am2940's and, when the ENABLE COUNTERS instruction is applied, address and word counting is controlled by the CNT bit of the Microinstruction Register.

Asynchronous interface control circuitry generates System Bus control signals and enables the Am2940 Address onto the System Address Bus at the appropriate time. The open-collector DONE outputs are dot-anded and used as a test input to the Am2910 Microprogram Sequencer.

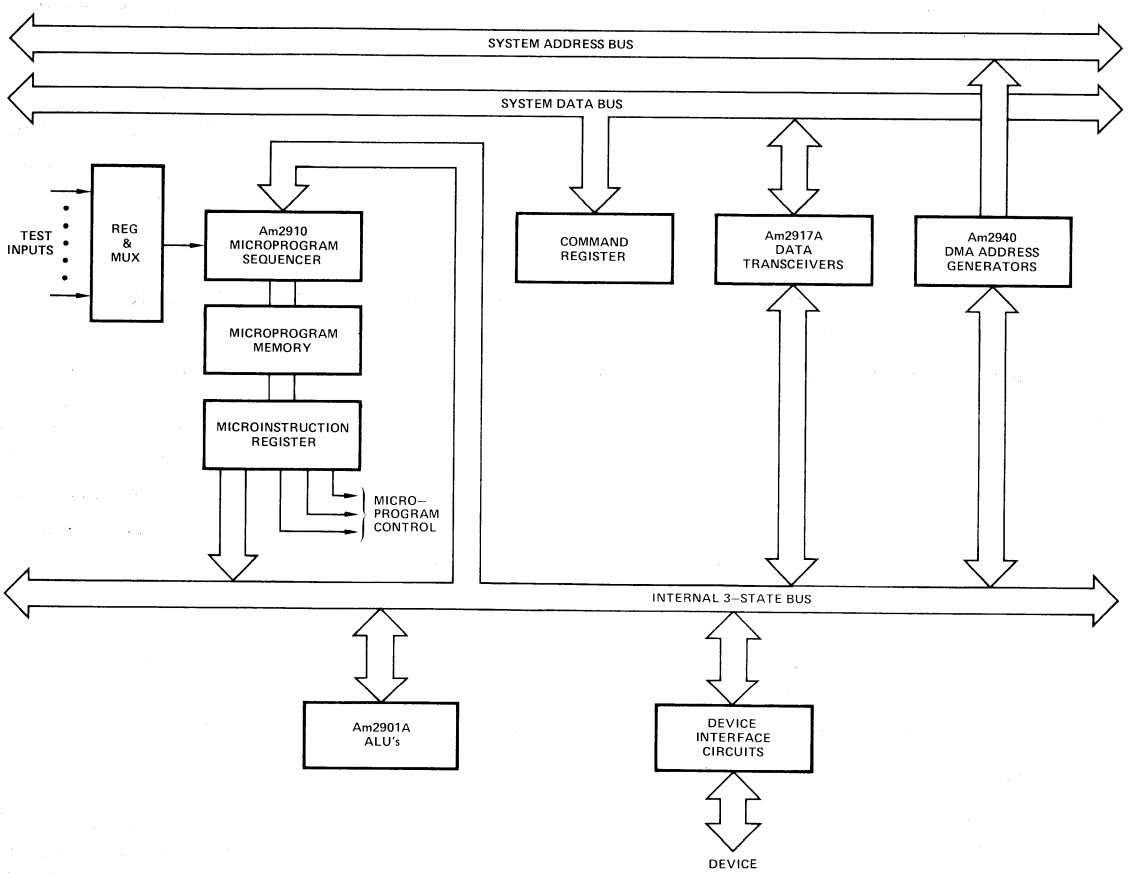


Figure 3. DMA Peripheral Controller Block Diagram.

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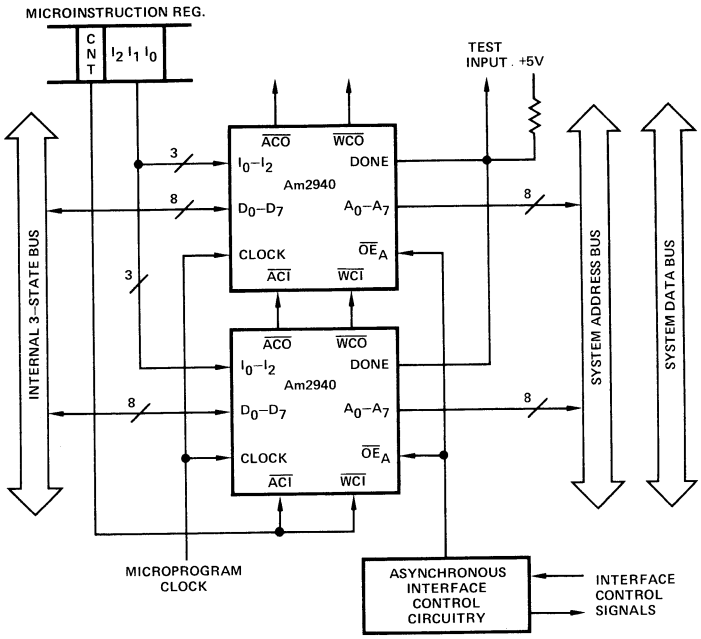

Figure 4. Am2940 Interconnections.

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ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2940PC	P-28	C	C-1
AM2940DC	D-28	C	C-1
AM2940DC-B	D-28	C	B-1
AM2940DM	D-28	M	C-3
AM2940DM-B	D-28	M	B-3
AM2940FM	F-28	M	C-3
AM2940FM-B	F-28	M	B-3
AM2940XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2940XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Am2942

Programmable Timer/Counter
DMA Address Generator

DISTINCTIVE CHARACTERISTICS

- 22-pin version of Am2940 –
  Provides multiplexed Address and Data lines plus additional Instruction Input and Instruction Enable pins.
- Can be used as either DMA Address Generator or Programmable Timer Counter.
- Executes 16 instructions –
  Eight DMA instructions plus eight Timer/Counter instructions
- Provides two independent programmable 8-bit up/down counters in a 22-pin package –
  Counters can be cascaded to form single-chip 16-bit up/down counter.
- Reinitialize capability –
  Counters can be reinitialized from on-chip registers.
- Expandable eight-bit slice –
  Any number of Am2942s can be cascaded. Three devices provide a 48 bit counter.
- Programmable control modes –
  Provide four types of control.
- High speed bipolar LSI –
  Advanced Low-Power Schottky TTL technology provides typical count frequency of 25MHz and 24mA output current sink capability.

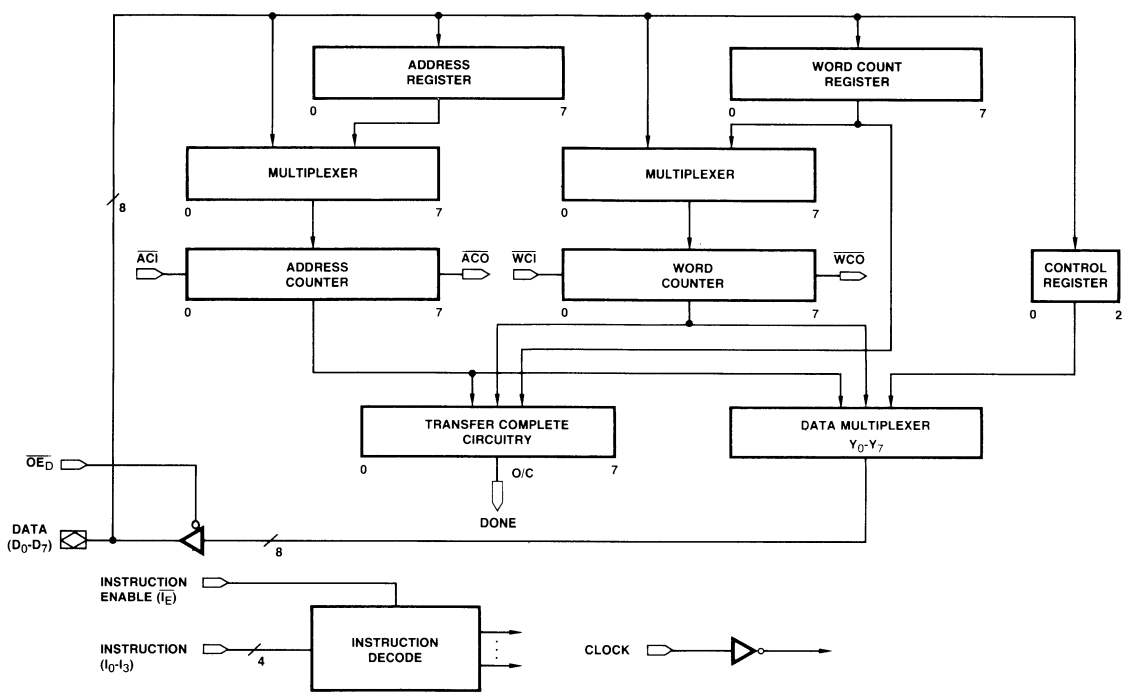
GENERAL DESCRIPTION

The Am2942, a 22-pin version of the Am2940, can be used as a high-speed DMA Address Generator or Programmable Timer/Counter. It provides multiplexed Address and Data lines, for use with a common bus, and additional Instruction Input and Instruction Enable pins. The Am2942 executes 16 instructions; eight are the same as the Am2940 instructions, and eight instructions facilitate the use of the Am2942 as a Programmable Timer/Counter. The Instruction Enable input allows the sharing of the Am2942 instruction field with other devices.

When used as a Timer/Counter, the Am2942 provides two independent, programmable, eight-bit, up-down counters in a 22-pin package. The two on-chip counters can be cascaded to form a single chip, 16-bit counter. Also, any number of chips can be cascaded – for example three cascaded Am2942s form a 48-bit timer/counter.

Reinitialization instructions provide the capability to reinitialize the counters from on-chip registers. Am2942 Programmable Control Modes, identical to those of the Am2940, offer four different types of programmable control.

BLOCK DIAGRAM



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Am2942 ARCHITECTURE

As shown in the Block Diagram, the Am2942 consists of the following:

- A three-bit Control Register.
- An eight-bit Address Counter with input multiplexer.
- An eight-bit Address Register.
- An eight-bit Word Counter with input multiplexer.
- An eight-bit Word Count Register.
- Transfer complete circuitry.
- An eight-bit wide data multiplexer with three-state output buffers.
- An instruction decoder.

Control Register

Under instruction control, the Control Register can be loaded or read from the bidirectional DATA lines D_0-D_7. Control Register bits 0 and 1 determine the Am2942 Control Mode, and bit 2 determines whether the Address Counter increments or decrements. Figure 1 defines the Control Register format.

Address Counter

The Address Counter, which provides the current memory address, is an eight-bit, binary, up/down counter with full look-ahead carry generation. The Address Carry input ($\overline{ACI}$) and Address Carry Output ($\overline{ACO}$) allow cascading to accommodate larger addresses. Under instruction control, the Address Counter can be enabled, disabled, and loaded from the DATA inputs, D_0-D_7, or the Address Register. When enabled and the $\overline{ACI}$ input is LOW, the Address Counter increments/decrements on the LOW to HIGH transition of the CLOCK input, CP.

Address Register

The eight-bit Address Register saves the initial address so that it can be restored later in order to repeat a transfer operation. When the LOAD ADDRESS instruction is executed, the Address Register and Address Counter are simultaneously loaded from the DATA inputs, D_0-D_7.

Word Counter and Word Count Register

The Word Counter and Word Count Register, which maintain and save a word count, are similar in structure and operation to the Address Counter and Address Register, with the exception that the Word Counter increments in Control Modes 1 and 3, and decrements in Control Modes 0 and 2. The LOAD WORD COUNT instruction simultaneously loads the Word Counter and Word Count Register.

Transfer Complete Circuitry

The Transfer Complete Circuitry is a combinational logic network which detects the completion of the data transfer operation in three Control Modes and generates the DONE output signal. The DONE signal is a open-collector output, which can be dot-anded between chips.

Data Multiplexer

The Data Multiplexer is an eight-bit wide, three-input multiplexer which allows the Address Counter, Word Counter and Control Register to be read at DATA lines D_0-D_7. The Data Multiplexer output, Y_0-Y_7, is enabled onto DATA lines D_{0-7} if and only if the Output Enable input, $\overline{OE_D}$, is LOW. (Refer to Figure 2.)

Instruction Decoder

The Instruction Decoder generates required internal control signals as a function of the INSTRUCTION inputs, I_0-I_3 Control Register bits 0 and 1, and the INSTRUCTION ENABLE input, $\overline{I_E}$.

Clock

The CLOCK input, CP is used to clock the Address Register, Address Counter, Word Count Register, Word Counter, and Control Register, all on the LOW to HIGH transition of the CP signal.

Control Register

CR_2	CR_1	CR_0

CR_1	CR_0	Control Mode Number	Control Mode Type	Word Counter	DONE Output Signal	
					$\overline{WCI}$ = LOW	$\overline{WCI}$ = HIGH
L	L	0	Word Count Equals Zero	Decrement	HIGH when Word Counter = 1	HIGH when Word Counter = 0
L	H	1	Word Count Compare	Increment	HIGH when Word Counter + 1 = Word Count Reg.	HIGH when Word Counter = Word Count Reg.
H	L	2	Address Compare	Decrement	HIGH when Word Counter = Address Counter	
H	H	3	Word Counter Carry Out	Increment	Always LOW	

H = HIGH
L = LOW

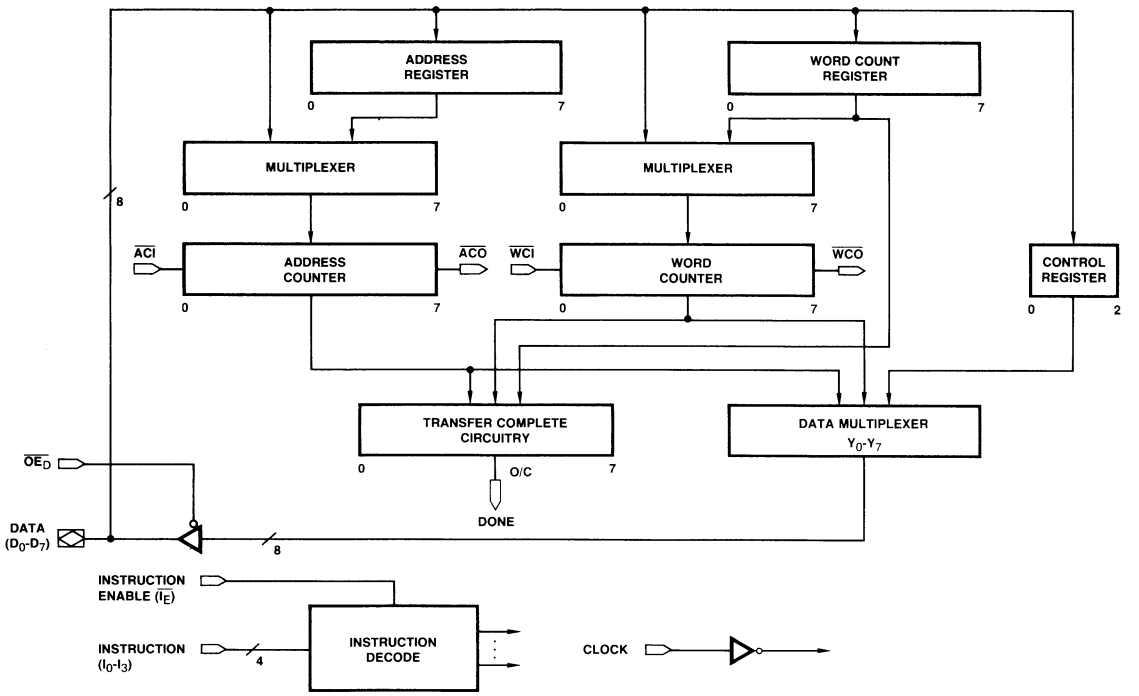
CR_2	Address Counter
L	Increment
H	Decrement

Figure 1. Control Register Format Definition.

$\overline{OE_D}$	D_0-D_7
L	DATA MULTIPLEXER OUTPUT, Y_0-Y_7
H	HIGH Z

Figure 2. Data Bus Output Enable Function.

BLOCK DIAGRAM



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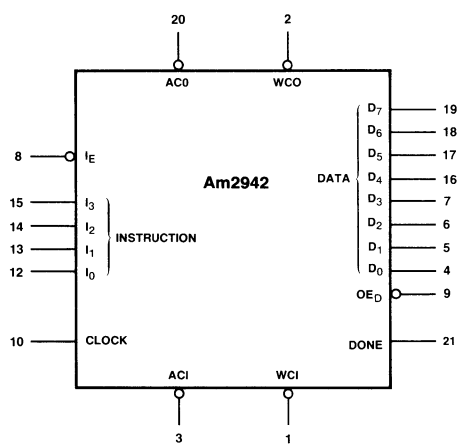
LOGIC SYMBOL



V_{CC} = Pin 22
GND = Pin 11

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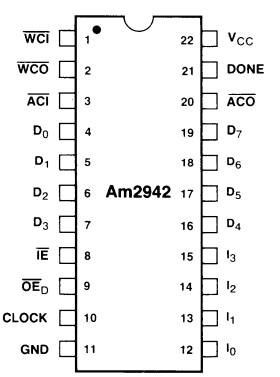
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation

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Am2942 CONTROL MODES

Control Mode 0 – Word Count Equals Zero Mode

In this mode, the LOAD WORD COUNT instruction loads the word count into the Word Count Register and Word Counter. When the Word Counter is enabled and the Word Counter Carry-in, $\overline{WCI}$, is LOW, the Word Counter decrements on the LOW to HIGH transition of the CLOCK input, CP. Figure 1 specifies when the DONE signal is generated in this mode.

Control Mode 1 – Word Count Compare Mode

In this mode the LOAD WORD COUNT instruction loads the word count into the Word Count Register and clears the Word Counter. When the Word Counter is enabled and the Word Counter Carry-in, $\overline{WCI}$, is LOW, the Word Counter increments on the LOW to HIGH transition of the clock input, CP. Figure 1 specifies when the DONE signal is generated.

Control Mode 2 – Address Compare Mode

In this mode, only an initial and final memory address need to be specified. The initial Memory Address is loaded into the Address Register and Address Counter and the final memory address is loaded into the Word Count Register and Word Counter. The Word Counter is always disabled in this mode and serves as a holding register for the final memory address. When the Address Counter is enabled and the $\overline{ACI}$ input is LOW, the Address Counter increments or decrements (depending on Control Register bit 2) on the LOW to HIGH transition of the CLOCK input, CP. The Transfer Complete Circuitry compares the Address Counter with the Word Counter and generates the DONE signal during the last word transfer, i.e. when the Address Counter equals the Word Counter.

Control Mode 3 – Word Counter Carry Out Mode

For this mode of operation, the user can load the Word Count Register and Word Counter with the two's complement of the number of data words to be transferred. When the Word Counter is enabled and the $\overline{WCI}$ input is LOW, the Word Counter increments on the LOW to HIGH transition of the CLOCK input, CP. A Word Counter Carry Out signal, $\overline{WCO}$, indicates the last data word is being transferred. The DONE signal is not required in this mode and, therefore, is always LOW.

Am2942 INSTRUCTIONS

The Am2942 instruction set consists of sixteen instructions. Eight are DMA Instructions and are similar to the Am2940 instructions. The remaining eight instructions are designed to facilitate the use of the Am2942 as a Programmable Timer/Counter. Figures 3 and 4 define the Am2942 Instructions.

Instructions 0-7 are DMA instructions. The WRITE CONTROL REGISTER instruction writes DATA input D_0-D_2 into the Control Register; DATA inputs D_3-D_7 are "don't care" inputs for this instruction. The READ CONTROL REGISTER instruction gates the Control Register to Data Multiplexer outputs Y_0-Y_2. Outputs Y_3-Y_7 are HIGH during this instruction.

The Word Counter can be read using the READ WORD COUNTER instruction, which gates the Word Counter to Data Multiplexer outputs, Y_0-Y_7. The LOAD WORD COUNT instruction is Control Mode dependent. In Control Modes 0, 2, and 3, DATA inputs D_0-D_7 are written into both the Word Count Register and Word Counter. In Control Mode 1, DATA inputs D_0-D_7 are written into the Word Count Register and the Word Counter is cleared.

The READ ADDRESS COUNTER instruction gates the Address Counter to Data Multiplexer outputs, Y_0-Y_7, and the LOAD ADDRESS instruction writes DATA inputs D_0-D_7 into both the Address Register and Address Counter.

In Control Modes 0, 1, and 3, the ENABLE COUNTERS instruction enables both the Address and Word Counters; in Control Mode 2, the Address Counter is enabled and the Word Counter holds its contents. When enabled and the carry input is active, the counters increment on the LOW to HIGH transition of the CLOCK input, CP. Thus, with this instruction applied, counting can be controlled by the carry inputs.

The REINITIALIZE COUNTERS instruction also is Control Mode dependent. In Control Modes 0, 2, and 3, the contents of the Address Register and Word Count Register are transferred to the respective Address Counter and Word Counter; in Control Mode 1, the content of the Address Register is transferred to the Address Counter and the Word Counter is cleared. The REINITIALIZE COUNTERS instruction allows a data transfer operation to be repeated without reloading the address and word count from the DATA lines.

When $\overline{I_E}$ is HIGH, Instruction inputs, I_0-I_2, are disabled. If I_3 is LOW, the function performed is identical to that of the ENABLE COUNTERS instruction. Thus, counting can be controlled by the carry inputs with the ENABLE COUNTERS instruction applied or with Instruction Inputs I_0-I_2 disabled.

Instructions 8-F facilitate the use of the Am2942 as a Programmable Timer/Counter. They differ from instructions 0-7 in that they provide independent control of the Address Counter, Word Counter and Control Register.

The WRITE CONTROL REGISTER, T/C instruction writes DATA input D_0-D_2 into the Control Register. DATA inputs D_3-D_7 are "don't care" inputs for this instruction. The Address and Word Counters are enabled, and the Control Register contents appear at the Data Multiplexer output.

The REINITIALIZE ADDRESS COUNTER instruction allows the independent reinitialization of the Address Counter. The Word Counter is enabled and the contents of the Address Counter appear at the Data Multiplexer output.

$\overline{I_E}$	I_3	I_2	I_1	I_0	HEX CODE		
0	0	0	0	0	0	WRITE CONTROL REGISTER	DMA INSTRUCTIONS
0	0	0	0	1	1	READ CONTROL REGISTER	
0	0	0	1	0	2	READ WORD COUNTER	
0	0	0	1	1	3	READ ADDRESS COUNTER	
0	0	1	0	0	4	REINITIALIZE COUNTERS	
0	0	1	0	1	5	LOAD ADDRESS	
0	0	1	1	0	6	LOAD WORD COUNT	
0	0	1	1	1	7	ENABLE COUNTERS	
1	0	X	X	X	0-7	INSTRUCTION DISABLE	
0	1	0	0	0	8	WRITE CONTROL REGISTER, T/C	TIMER/COUNTER INSTRUCTIONS
0	1	0	0	1	9	REINITIALIZE ADDRESS COUNTER	
0	1	0	1	0	A	READ WORD COUNTER, T/C	
0	1	0	1	1	B	READ ADDRESS COUNTER, T/C	
0	1	1	0	0	C	REINITIALIZE ADDRESS & WORD COUNTERS	
0	1	1	0	1	D	LOAD ADDRESS, T/C	
0	1	1	1	0	E	LOAD WORD COUNT, T/C	
0	1	1	1	1	F	REINITIALIZE WORD COUNTER	
1	1	X	X	X	8-F	INSTRUCTION DISABLE, T/C	

0 = LOW 1 = HIGH X = DON'T CARE

Notes: 1. When I_3 is tied LOW, the Am2942 acts as a DMA circuit: When I_3 is tied HIGH, the Am2942 acts as a Timer/Counter circuit.
2. Am2942 instructions 0 through 7 are the same as Am2940 instructions.

Figure 3. Am2942 Instructions.

The Word Counter can be read, using the READ WORD COUNTER, T/C instruction. Both counters are enabled when this instruction is executed.

When the READ ADDRESS COUNTER, T/C instruction is executed, both counters are enabled and the address counter contents appear at the Data Multiplexer output.

The REINITIALIZE ADDRESS and WORD COUNTERS instruction provides the capability to reinitialize both counters at the same time. The Address Counter contents appear at the Data Multiplexer output.

DATA inputs D_0-D_7 are loaded into both the Address Register and Counter when the LOAD ADDRESS, T/C instruction is executed. The Word Counter is enabled and its contents appear at the Data Multiplexer output.

The LOAD WORD COUNT, T/C instruction is identical to the LOAD WORD COUNT instruction with the exception that Address Counter is enabled.

The Word Counter can be independently reinitialized using the REINITIALIZE WORD COUNTER instruction. The Address Counter is enabled and the Word Counter contents appear at the Data Multiplexer output.

When the $\overline{I_E}$ input is HIGH, Instruction inputs, I_0-I_2, are disabled. The function performed when I_3 is HIGH is identical to that performed when I_3 is LOW, with the exception that the Word Counter contents appear at the Data Multiplexer output.

$\overline{I_E}$	$I_3I_2I_1I_0$ (Hex)	Function	Mnemonic	Control Mode	Word Reg.	Word Counter	Adr. Reg.	Adr. Counter	Control Reg.	Data Multiplexer Output
L	0	WRITE CONTROL REGISTER	WRCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	$D_{0-2} \rightarrow$ CR	FORCED HIGH
L	1	READ CONTROL REGISTER	RDCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	CONTROL REG.
L	2	READ WORD COUNTER	RDWC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	WORD COUNTER
L	3	READ ADDRESS COUNTER	RDAC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	ADR. COUNTER
L	4	REINITIALIZE COUNTERS	REIN	0, 2, 3	HOLD	WR → WC	HOLD	AR → AC	HOLD	ADR. CNTR.
				1	HOLD	ZERO → WC	HOLD	AR → AC	HOLD	ADR. CNTR.
L	5	LOAD ADDRESS	LDAD	0, 1, 2, 3	HOLD	HOLD	D → AR	D → AC	HOLD	WORD COUNTER
L	6	LOAD WORD COUNT	LDWC	0, 2, 3	D → WR	D → WC	HOLD	HOLD	HOLD	FORCED HIGH
				1	D → WR	ZERO → WC	HOLD	HOLD	HOLD	FORCED HIGH
L	7	ENABLE COUNTERS	ENCT	0, 1, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	ADR. CNTR.
				2	HOLD	HOLD	HOLD	ENABLE	HOLD	ADR. CNTR.
H	0-7	INSTRUCTION DISABLE	–	0, 1, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	ADR. CNTR.
				2	HOLD	HOLD	HOLD	ENABLE	HOLD	ADR. CNTR.
L	8	WRITE CONTROL REGISTER, T/C	WCRT	0, 1, 2, 3	HOLD	ENABLE	HOLD	ENABLE	$D_{0-2} \rightarrow$ CR	CONTROL REG.
L	9	REINITIALIZE ADR. COUNTER	REAC	0, 1, 2, 3	HOLD	ENABLE	HOLD	AR → AC	HOLD	ADR. COUNTER
L	A	READ WORD COUNTER, TC	RWCT	0, 1, 2, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	WORD COUNTER
L	B	READ ADDRESS COUNTER, T/C	RACT	0, 1, 2, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	ADR. COUNTER
L	C	REINITIALIZE ADDRESS AND WORD COUNTERS	RAWC	0, 2, 3	HOLD	WR → WC	HOLD	AR → AC	HOLD	ADR. CNTR.
				1	HOLD	ZERO → WC	HOLD	AR → AC	HOLD	ADR. CNTR.
L	D	LOAD ADDRESS, T/C	LDAT	0, 1, 2, 3	HOLD	ENABLE	D → AR	D → AC	HOLD	WORD COUNTER
L	E	LOAD WORD COUNT, T/C	LWCT	0, 2, 3	D → WR	D → WC	HOLD	ENABLE	HOLD	FORCED HIGH
				1	D → WR	ZERO → WC	HOLD	ENABLE	HOLD	FORCED HIGH
L	F	REINITIALIZE WORD COUNTER	REWC	0, 2, 3	HOLD	WR → WC	HOLD	ENABLE	HOLD	WD. CNTR.
				1	HOLD	ZERO → WC	HOLD	ENABLE	HOLD	WD. CNTR.
H	8-F	INSTRUCTION DISABLE, T/C	–	0, 1, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	WD. CNTR.
				2	HOLD	HOLD	HOLD	ENABLE	HOLD	WD. CNTR.

WR = WORD REGISTER
WC = WORD COUNTER
AR = ADDRESS REGISTER
AC = ADDRESS COUNTER
CR = CONTROL REGISTER
D = DATA

Figure 4. Am2942 Function Table.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

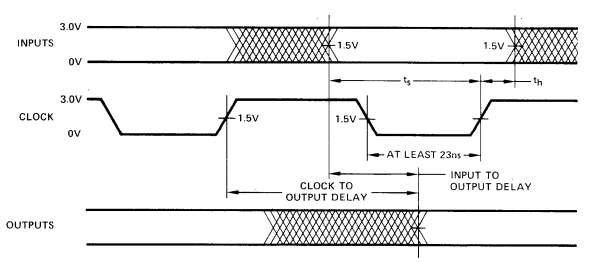
OPERATING RANGE

P/N	Range	Temperature	V_{CC}	
Am2942PC, DC	COM'L	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5%	(MIN. = 4.75V MAX. = 5.25V)
Am2942DM, FM	MIL	T_C = −55° to +125°C	V_{CC} = 5.0V ±10%	(MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}		MIL I_{OH} = −1.0mA COM'L I_{OH} = −2.6mA	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL} (Note 5)	WCO, ACO	MIL I_{OL} = 8.0mA COM'L I_{OL} = 12mA			0.5	Volts
			D_{0-7}, DONE	MIL I_{OL} = 16mA COM'L I_{OL} = 24mA				
V_{IH}	Input HIGH Level (Note 4)	Guaranteed Input Logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Note 4)	Guaranteed Input Logical LOW voltage for all inputs					0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V		D_{0-7} All Others			−0.15 −0.8	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V		D_{0-7} All Others			150 40	µA
I_{CEX}	Output Leakage on DONE	V_{CC} = MAX., V_0 = 5.5V					250	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX. + 0.5V, V_O = 0.5V			−30		−85	mA
I_{OZL} I_{OZH}	Output OFF Current	V_{CC} = MAX. $\overline{OE}$ = 2.4V	V_{OUT} = 0.5V V_{OUT} = 2.4V	D_{0-7} D_{0-7}			−150 150	µA
I_{CC}	Power Supply Current	V_{CC} = MAX.		T_A = 25°C		155	250	mA
			Am2942PC, DC	T_A = 0°C to +70°C			265	
				T_A = +70°C			220	
			Am2942DM, FM	T_C = −55°C to +125°C			285	
				T_C = +125°C			205	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide no guaranteed noise immunity and should only be tested in a static-, noise-free environment.
5. I_{OL} limit on A_i and D_i (i = 0 to 7) applies to either output individually, but not both at the same time. The sum of the loading on A_i plus D_i is limited to 24mA MIL or 32mA COM'L.



See Tables A for t_s and t_h for various inputs. See Tables B for combinational delays from clock and other inputs to outputs.

Figure 5. Switching Waveforms.

PRELIMINARY SWITCHING CHARACTERISTICS

The tables below define the Am2942 switching characteristics. Tables A are set-up and hold times relative to the clock LOW-to-HIGH transition. Tables B are combinational delays. Tables C are clock requirements. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns with C_L = 50pF except output disable times (I to D) which are specified for a 5pF load. All times are in ns.

I. TYPICAL ROOM TEMPERATURE CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	13	3
I_{012}	33	2
$\overline{ACI}$	15	2
$\overline{WCI}$	15	1

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	DONE	D_{0-7}
$\overline{ACI}$	12	–	–	–
$\overline{WCI}$ (Note 1)	–	12	27	–
I_{0-2}	–	–	–	21
CP (Note 2)	35	35	50	–

C. Clock Requirements

Minimum Clock LOW Time	20	ns
Minimum Clock HIGH Time	30	ns
Maximum Clock Frequency	28	MHz

D. Enable/Disable Times

From	To	Disable	Enable	
$\overline{OE}$	D_{0-7}	19	13	ns

II. GUARANTEED ROOM TEMPERATURE CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	24	6
I_{012}	46	5
$\overline{ACI}$	30	4
$\overline{WCI}$	30	3

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	DONE	D_{0-7}
$\overline{ACI}$	18	–	–	–
$\overline{WCI}$ (Note 1)	–	18	41	–
I_{0-2}	–	–	–	34
CP (Note 2)	50	50	77	–

C. Clock Requirements

Minimum Clock LOW Time	23	ns
Minimum Clock HIGH Time	30	ns
Maximum Clock Frequency	22	MHz

D. Enable/Disable Times

From	To	Disable	Enable	
$\overline{OE}$	D_{0-7}	23	23	ns

III. GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

Am2942PC, DC (T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	21	4
I_{012}	41	3
$\overline{ACI}$	27	3
$\overline{WCI}$	27	3

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	DONE	D_{0-7}
$\overline{ACI}$	20	–	–	–
$\overline{WCI}$ (Note 1)	–	20	46	–
I_{0-2}	–	–	–	37
CP (Note 2)	58	58	85	–

C. Clock Requirements

Minimum Clock LOW Time	23	ns
Minimum Clock HIGH Time	34	ns
Maximum Clock Frequency	20	MHz

D. Enable/Disable Times

From	To	Disable	Enable	
$\overline{OE}$	D_{0-7}	25	25	ns

IV. GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

Am2942DM, FM (T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	27	7
I_{012}	49	5
$\overline{ACI}$	34	5
$\overline{WCI}$	34	5

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	DONE	D_{0-7}
$\overline{ACI}$	21	–	–	–
$\overline{WCI}$ (Note 1)	–	21	54	–
I_{0-2}	–	–	–	41
CP (Note 2)	64	64	88	–

C. Clock Requirements

Minimum Clock LOW Time	23	ns
Minimum Clock HIGH Time	35	ns
Maximum Clock Frequency	15	MHz

D. Enable/Disable Times

From	To	Disable	Enable	
$\overline{OE}$	D_{0-7}	30	30	ns

Notes: 1. $\overline{WCI}$ to Done occurs only in control modes 0 and 1.
2. CP to Done occurs only in control modes 0, 1, and 2.

APPLICATIONS

Figure 6 shows an Am2942 used as two independent, programmable eight-bit timer/counters. In this example, an Am2910 Microprogram Sequencer provides an address to Am29775 512 x 8 Registered PROMs. The on-chip PROM output register is used as the Microinstruction Register.

The Am2942 Instruction input, I_3, is tied HIGH to select the eight Timer/Counter instructions. The $\overline{I_E}$, I_0-I_2, and $\overline{OE_D}$ inputs are provided by the microinstruction, and the D_0-D_7 data lines are connected to a common Data Bus. GATE WC and GATE AC are separate enable controls for the respective Word Counter and Address Counter. The DONE, $\overline{ACO}$ and $\overline{WCO}$ output signals indicate that a pre-programmed time or count has been reached.

Figure 7 shows an Am2942 used as a single 16-bit programmable timer/counter. In this example, the Word Counter carry-out, $\overline{WCO}$, is connected to the Address Counter carry-in, $\overline{ACI}$, to form a single 16-bit counter which is enabled by the GATE signal.

Figure 8 shows two Am2942s cascaded to form a 32-bit programmable timer/counter. The two Word Counters form the low order 16 bits, and the two Address Counters form the high order bits. This allows the timer/counter to be loaded and read 16 bits at a time.

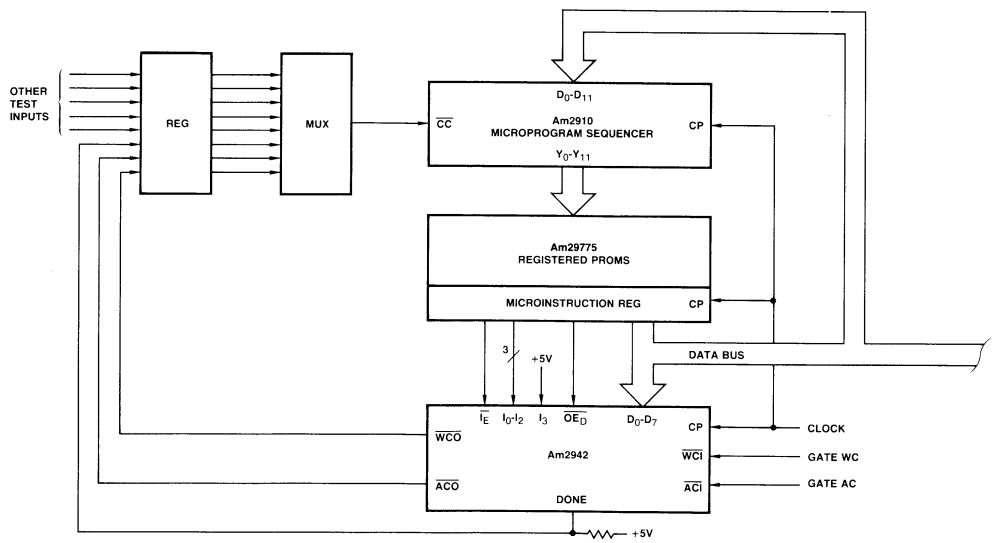


Figure 6. Two 8-Bit Programmable Counters/Timers in a 22-Pin Package.

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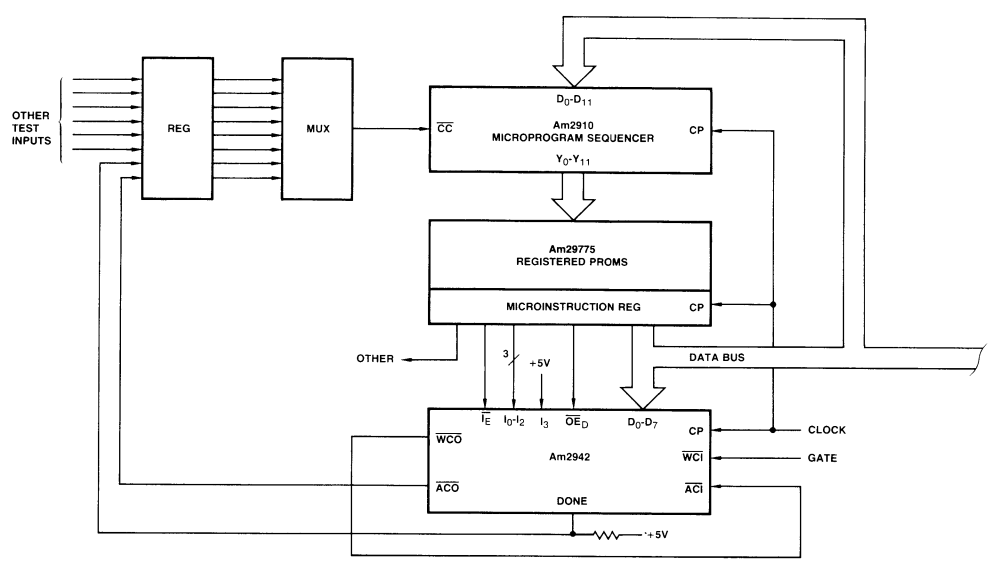

Figure 7. 16-Bit Programmable Counter/Timer Using a Single Am2942.

MPR-235

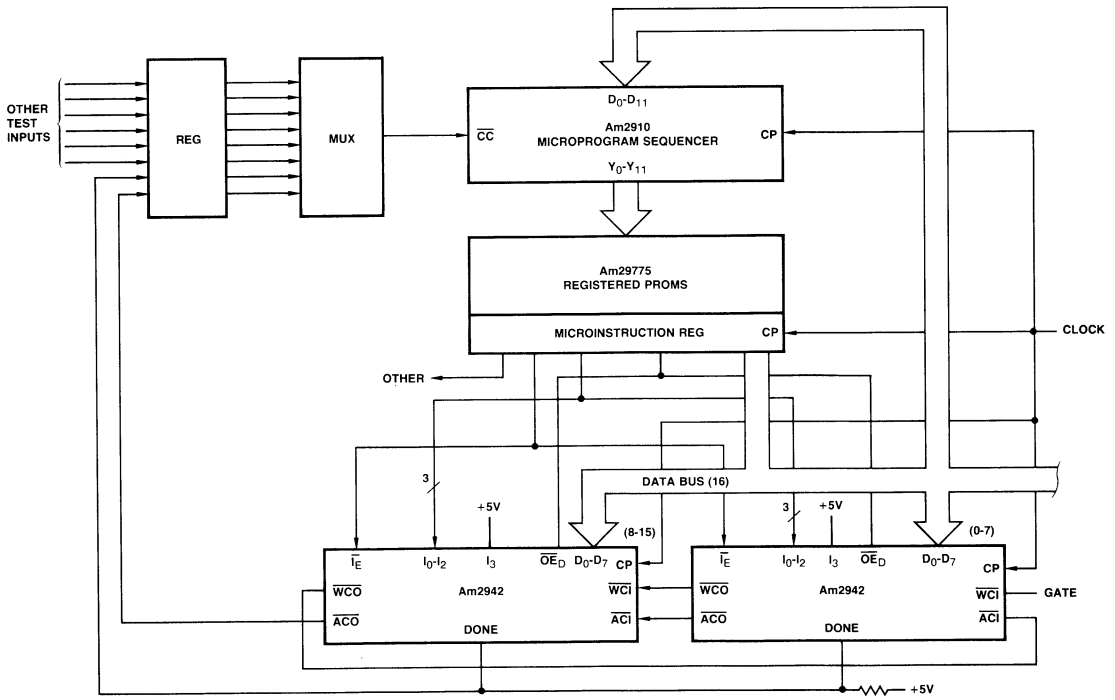

Figure 8. 32-Bit Programmable Counter/Timer Using Two Am2942s.

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ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
Am2942PC	P-22	C	C-1
Am2942DC	D-22	C	C-1
Am2942DC-B	D-22	C	B-1
Am2942DM	D-22	M	C-3
Am2942DM-B	D-22	M	B-3
Am2942FM	F-22	M	C-3
Am2942FM-B	F-22	M	B-3
Am2942XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
Am2942XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Am8085A

Single Chip 8-Bit N-Channel Microprocessor

DISTINCTIVE CHARACTERISTICS

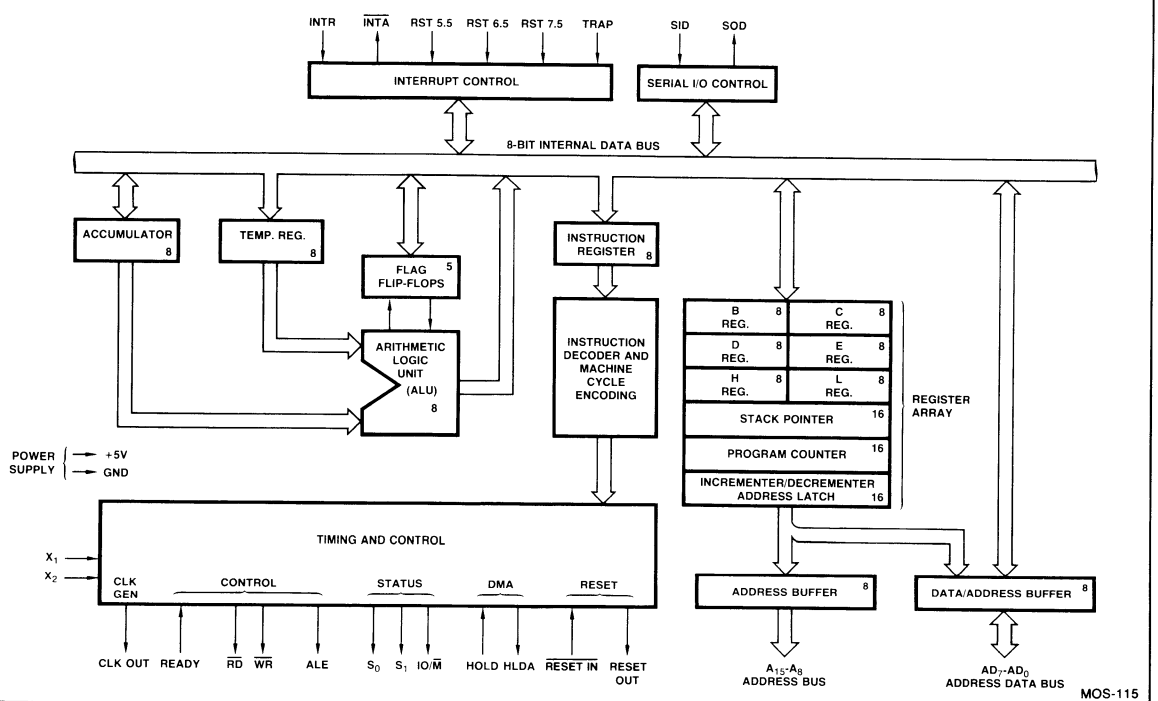
- 1.3μs instruction cycle; 3MHz internal clock
- Single +5V power supply
- 100% software compatible with Am8080A
- On-chip clock generator (with external crystal or RC network)
- On-chip system controller; advanced cycle status information available for large system control
- Four vectored interrupts (one is non-maskable)
- Serial in/serial out port
- Decimal, binary and double precision arithmetic
- Direct addressing capability to 64K bytes of memory
- 100% MIL-STD-883, Level C processing

GENERAL DESCRIPTION

The Am8085A is a new generation, complete 8-bit parallel central processing unit (CPU). Its instruction set is 100% software compatible with the Am8080A microprocessor. Its high level of system integration allows a minimum system of three ICs: Am8085A (CPU), Am8155/56 (RAM), and Am8355 (ROM). Specifically, the Am8085A incorporates all of the features that the Am8224 (clock generator) and Am8228 (system controller) provided for the Am8080A.

The Am8085A uses a multiplexed Data Bus. The address is split between the 8-bit address bus and the 8-bit data bus. The on-chip address latches of Am8155/8355 memory products allows a direct interface with Am8085A. The Am8085A components, including various timing compatible support chips, allow system speed optimization.

BLOCK DIAGRAM

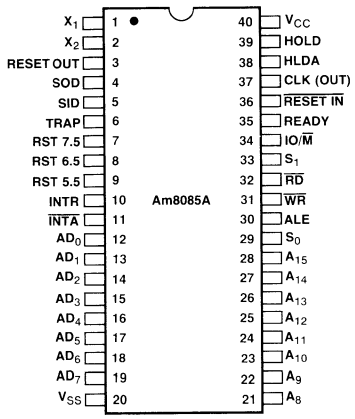


ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP*	$0°C \leq T_A \leq +70°C$	Am8085ADC or Am8085ACC
Molded DIP		Am8085APC

*DC = Side-Brazed Ceramic
CC = Cerdip

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

Figure 1.

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Am8085A FUNCTIONAL PIN DEFINITION

The following describes the function of each pin:

A_8-A_{15} (Output 3-State)

Address Bus – the most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes.

AD_0-AD_7 (Input/Output 3-State)

Multiplexed Address/Data Bus – lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle of a machine state. It then becomes the data bus during the second and third clock cycles.

3-stated during Hold and Halt modes.

ALE (Output)

Address Latch Enable – it occurs during the first clock cycle of a machine state and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. ALE can also be used to strobe the status information. ALE is never 3-stated.

S_0, S_1 (Output)

Data Bus Status. Encoded status of the bus cycle.

S_1	S_0	
0	0	HALT
0	1	WRITE
1	0	READ
1	1	FETCH

S_1 can be used as an advanced R/$\overline{W}$ status.

$\overline{RD}$ (Output 3-state)

READ – indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer. 3-stated during Hold and Halt.

$\overline{WR}$ (Output 3-state)

WRITE – indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$. 3-stated during Hold and Halt modes.

READY (Input)

If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If Ready is low, the CPU will wait for Ready to go high before completing the read or write cycle.

HOLD (Input)

HOLD – indicates that another Master is requesting the use of the Address and Data Buses. The CPU, upon receiving the Hold request, will relinquish the use of buses as soon as the completion of the current machine cycle. Internal processing can continue. The processor can regain the buses only after the Hold is removed. When the Hold is acknowledged, the Address, Data, $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines are 3-stated.

HLDA (Output)

HOLD ACKNOWLEDGE – indicates that the CPU has received the Hold request and that it will relinquish the buses in the next clock cycle. HLDA goes low after the Hold request is removed. The CPU takes the buses one half clock cycle after HLDA goes low.

INTR (Input)

INTERRUPT REQUEST – is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of the instruction. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.

$\overline{\text{INTA}}$ (Output)

INTERRUPT ACKNOWLEDGE – is used instead of (and has the same timing as) $\overline{\text{RD}}$ during the Instruction cycle after an INTR is accepted. It can be used to activate the Am8259 Interrupt chip or some other interrupt port.

RST 5.5
RST 6.5 — (Inputs)
RST 7.5

RESTART INTERRUPTS – these three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted.

RST 7.5 → Highest Priority
RST 6.5
RST 5.5 → Lowest Priority

The priority of these interrupts is ordered as shown above. These interrupts have a higher priority than the INTR.

TRAP (Input)

Trap interrupt is a nonmaskable restart interrupt. It is recognized at the same time as INTR. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt.

$\overline{\text{RESET IN}}$ (Input)

Reset sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. None of the other flags or registers (except the instruction register) are affected. The CPU is held in the reset condition as long as Reset is applied.

RESET OUT (Output)

Indicates CPU is being reset. Can be used as a system RESET. The signal is synchronized to the processor clock.

X_1, X_2 (Input)

Crystal or R/C network connections to set the internal clock generator. X_1 can also be an external clock input instead of a crystal. The input frequency is divided by 2 to give the internal operating frequency.

CLK (Output)

Clock Output for use as a system clock when a crystal or R/C network is used as an input to the CPU. The period of CLK is twice the X_1, X_2 input period.

IO/$\overline{\text{M}}$ (Output)

IO/$\overline{\text{M}}$ indicates whether the Read/Write is to memory or I/O. Tri-stated during Hold and Halt modes.

SID (Input)

Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.

SOD (Output)

Serial output data line. The output SOD is set or reset as specified by the SIM instruction.

V_{CC}

+5 volt supply.

V_{SS}

Ground reference.

FUNCTIONAL DESCRIPTION

The Am8085A is a complete 8-bit parallel central processor. It is designed with N-channel depletion loads and requires a single +5 volt supply. Its basic clock speed is 3MHz thus improving on the present Am8080's performance with higher system speed. Also it is designed to fit into a minimum system of three ICs: The CPU, a RAM/IO, and a ROM or PROM/IO chip.

The Am8085A uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first cycle the address is sent out. The lower 8-bits are latched into the peripherals by the Address Latch Enable (ALE). During the rest of the machine cycle the Data Bus is used for memory or I/O data.

The Am8085A provides $\overline{\text{RD}}$, $\overline{\text{WR}}$, and IO/$\overline{\text{Memory}}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{\text{INTA}}$) is also provided. Hold, Ready, and all Interrupts are synchronized. The Am8085A also provides serial input data (SID) and serial output data (SOD) lines for simple serial interface.

In addition to these features, the Am8085A has three maskable, restart interrupts and one nonmaskable trap interrupt.

Am8085A vs. Am8080A

The Am8085A includes the following features on-chip in addition to all of the Am8080A functions.

a. Internal clock generator
b. Clock output
c. Fully synchronized Ready
d. Schmitt action on $\overline{\text{RESET IN}}$
e. $\overline{\text{RESET}}$ OUT pin
f. $\overline{\text{RD}}$, $\overline{\text{WR}}$, and IO/$\overline{\text{M}}$ Bus Control Signals
g. Encoded Status information
h. Multiplexed Address and Data
i. Direct Restarts and nonmaskable Interrupt
j. Serial Input/Output lines.

The internal clock generator requires an external crystal or R/C network. It will oscillate at twice the basic CPU operating frequency. A 50% duty cycle, two phase, nonoverlapping clock is generated from this oscillator internally and one phase of the clock ($\phi 2$) is available as an external clock. The Am8085A directly provides the external RDY synchronization previously provided by the Am8224. The $\overline{\text{RESET IN}}$ input is provided with a Schmitt action input so that power-on reset only requires a resistor and capacitor. RESET OUT is provided for System RESET.

The Am8085A provides $\overline{\text{RD}}$, $\overline{\text{WR}}$ and IO/$\overline{\text{M}}$ signals for Bus control. An $\overline{\text{INTA}}$ which was previously provided by the Am8228 in Am8080A systems is also included in Am8085A.

STATUS INFORMATION

Status information is directly available from the Am8085A. ALE serves as a status strobe. The status is partially encoded, and provides the user with advanced timing of the type of bus transfer being done. IO/$\overline{\text{M}}$ cycle status signal is provided directly also. Decoded S_0, S_1 carries the following status information:

S_1	S_0	
0	0	HALT
0	1	WRITE
1	0	READ
1	1	FETCH

S_1 can be interpreted as R/$\overline{\text{W}}$ in all bus transfers.

In the Am8085A the 8 LSB of address are multiplexed with the data instead of status. The ALE line is used as a strobe to enter the lower half of the address into the memory or peripheral address latch. This also frees extra pins for expanded interrupt capability.

MAXIMUM RATINGS above which useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{CC} with Respect to V_{SS}	−0.5V to +7.0V
All Signal Voltages with Respect to V_{SS}	−0.5V to +7.0V
Power Dissipation	1.5W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

DC CHARACTERISTICS (T_A = 0°C to +70°C; V_{CC} = 5.0V ±5%; V_{SS} = 0V; unless otherwise specified)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{IL}	Input Low Voltage		−0.5		+0.8	Volts
V_{IH}	Input High Voltage		2.0		V_{CC}+0.5	Volts
V_{OL}	Output Low Voltage	I_{OL} = 2.0mA			0.45	Volts
V_{OH}	Output High Voltage	I_{OH} = −400μA	2.4			Volts
I_{CC}	Power Supply Current				170	mA
I_{IL}	Input Leakage	V_{IN} = V_{CC}			±10	μA
I_{LO}	Output Leakage	0.45V ≤ V_{OUT} ≤ V_{CC}			±10	μA
V_{ILR}	Input Low Level, RESET		−0.5		+0.8	Volts
V_{IHR}	Input High Level, RESET		2.4		V_{CC}+0.5	Volts
V_{HY}	Hysteresis, RESET		0.25			Volts

BUS TIMING SPECIFICATION AS A T_{CYC} DEPENDENT

Parameters	Description	Min.	Typ.	Max.	Units
t_{AL}	Address Valid before Trailing Edge of ALE	(1/2)T−50			ns
t_{LA}	Address Hold Time after ALE	(1/2)T−60			ns
t_{LL}	ALE Width	(1/2)T−20			ns
t_{LCK}	ALE Low During CLK High	(1/2)T−60			ns
t_{LC}	Trailing Edge of ALE to Leading Edge of Control	(1/2)T−30			ns
t_{AD}	Valid Address to Valid Data In			(5/2+N)T−225	ns
t_{RD}	READ (or INTA) to Valid Data			(3/2+N)T−180	ns
t_{RAE}	Trailing Edge of READ to Re-Enabling of Address	(1/2)T−10			ns
t_{CA}	Address (A_8-A_{15}) Valid After Control	(1/2)T−40			ns
t_{DW}	Data Valid to Trailing Edge of WRITE	(3/2+N)T−60			ns
t_{WD}	Data Valid after Trailing Edge of WRITE	(1/2)T−60			ns
t_{CC}	Width of Control LOW (RD, WR, INTA)	(3/2+N)T−80			ns
t_{CL}	Trailing Edge of Control to Leading Edge of ALE	(1/2)T−110			ns
t_{ARY}	READY Valid from Address Valid			(3/2)T−260	ns
t_{HACK}	HLDA Valid to Trailing Edge of CLK	(1/2)T−50			ns
t_{HABF}	Bus Float after HLDA			(1/2)T+50	ns
t_{HABE}	HLDA to Bus Enable			(1/2)T+50	ns
t_{AC}	Address Valid to Leading Edge of Control	(2/2)T−50			ns
t_1	CLK Low Time	(1/2)T−80			ns
t_2	CLK High Time	(1/2)−40			ns
t_{RV}	Control Trailing Edge to Leading Edge of Next Control	(3/2)T−80			ns

Notes: 1. N is equal to the total WAIT states.
2. T = t_{CYC}.

AC CHARACTERISTICS (T_A = 0°C to +70°C; V_{CC} = 5.0V ±5%; V_{SS} = 0V)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{CYC}	CLK Cycle Period	See Notes 1-5	320		2000	ns
t_1	CLK Low Time		80			ns
t_2	CLK High Time		120			ns
t_r, t_f	CLK Rise and Fall Time				30	ns
t_{AL}	Address Valid Before Trailing Edge of ALE		110			ns
t_{LA}	Address Hold Time After ALE		100			ns
t_{LL}	ALE Width		140			ns
t_{LCK}	ALE Low During CLK High		100			ns
t_{LC}	Trailing Edge of ALE to Leading Edge of Control		130			ns
t_{AFR}	Address Float After Leading Edge of $\overline{READ}$ ($\overline{INTA}$)				0	ns
t_{AD}	Valid Address to Valid Data In				575	ns
t_{RD}	$\overline{READ}$ (or $\overline{INTA}$) to Valid Data				300	ns
t_{RDH}	Data Hold Time After $\overline{READ}$ ($\overline{INTA}$)		0			ns
t_{RAE}	Trailing Edge of $\overline{READ}$ to Re-Enabling of Address		150			ns
t_{CA}	Address (A_8-A_{15}) Valid After Control		120			ns
t_{DW}	Data Valid to Trailing Edge of $\overline{WRITE}$	t_{CYC} = 320ns;	420			ns
t_{WD}	Data Valid After Trailing Edge of $\overline{WRITE}$	C_L = 150pF	100			ns
t_{CC}	Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$)		400			ns
t_{CL}	Trailing Edge of Control to Leading Edge of ALE		50			ns
t_{ARY}	READY Valid from Address Valid				220	ns
t_{RYS}	READY Setup Time to Leading Edge of CLK		110			ns
t_{RYH}	READY Hold Time		0			ns
t_{HACK}	HLDA Valid to Trailing Edge of CLK		110			ns
t_{HABF}	Bus Float After HLDA				210	ns
t_{HABE}	HLDA to Bus Enable				210	ns
t_{LDR}	ALE to Valid Data In				460	ns
t_{RV}	Control Trailing Edge to Leading Edge of Next Control		400			ns
t_{AC}	Address Valid to Leading Edge of Control		270			ns
t_{HDS}	HOLD Setup Time to Trailing Edge of CLK		170			ns
t_{HDH}	HOLD Hold time		0			ns
t_{INS}	INTR Setup Time to Falling Edge of CLK, also RST and TRAP		160			ns
t_{INH}	INTR Hold Time		0			ns

Notes: 1. A_8-A_{15} Address Specs apply to IO/$\overline{M}$, S_0 and S_1.
2. For all output timing where $C_L \neq$ 150pF use the following correction factors:
   25pF < C_L < 150pF: −.10ns/pF
   150pF < C_L < 300pF: +.30ns/pF
3. Output timings are measured with purely capacitive load.
4. All timings are measured at output voltage V_L = 0.8V, V_H = 2.0V, and 1.5V with 20ns rise and fall time on inputs.
5. To calculate timing specifications at other values of t_{CYC} use the table in Table 2.

INTERRUPT AND SERIAL I/O

The Am8085A has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5 and TRAP. INTR is identical in function to the Am8080A INT. Each of three RESTART inputs, 5.5, 6.5, 7.5, has a programmable mask. TRAP is also a RESTART interrupt except it is non-maskable.

The three RESTART interrupts cause the internal execution of RST (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RST independent of the state of the interrupt enable or masks.

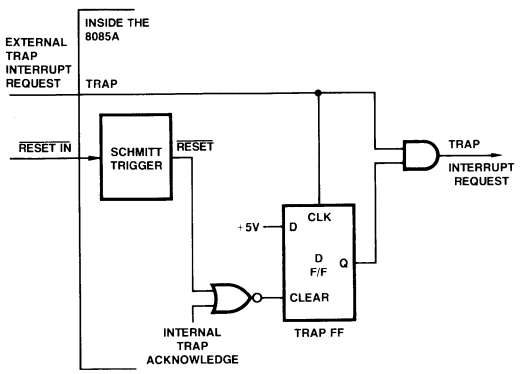
Name	RESTART Address (Hex)
TRAP	24_{16}
RST 5.5	$2C_{16}$
RST 6.5	34_{16}
RST 7.5	$3C_{16}$

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are high level-sensitive like INTR (and INT on the Am8080A) and are recognized with the same timing as INTR. RST 7.5 is rising edge-sensitive. For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request. The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a RESET IN to the Am8085A. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The status of the three RST interrupt masks can only be affected by the SIM instruction and RESET IN.

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP – highest priority, RST 7.5, RST 6.5, RST 5.5, INTR – lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt a RST 7.5 routine if the interrupts were re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic errors such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both edge and level sensitive. The TRAP input must go high and remain high to be acknowledged, but will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. The following diagram illustrates the TRAP interrupt request circuitry within the Am8085A.



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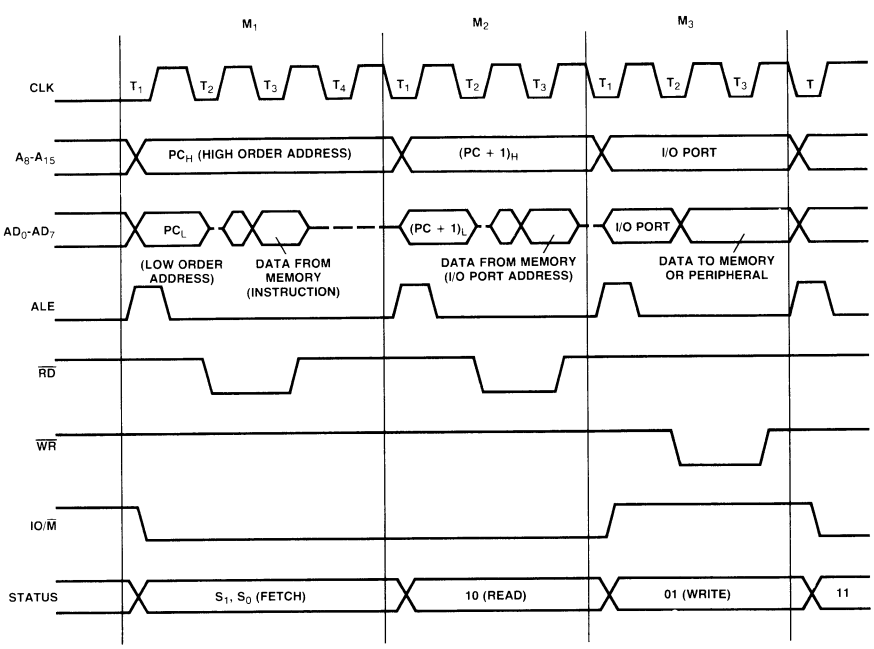

Figure 2. Am8085A Basic System Timing.

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INTERRUPT AND SERIAL I/O (Cont.)

Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

The TRAP interrupt is special in that it preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.

BASIC SYSTEM TIMING

The Am8085A has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8 bits of address on the Data Bus. Figure 2 shows an instruction fetch, memory read and I/O write cycle (OUT). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

As in the Am8080A, the READY line is used to extend the read and write pulse lengths so that the Am8085A can be used with slow memory. Hold causes the CPU to relinquish the bus when it is through with it by floating the Address and Data Buses.

SYSTEM INTERFACE

Am8085A family includes memory components, which are directly compatible to the Am8085A CPU. For example, a system consisting of the three chips, Am8085A, Am8156, and Am8355 will have the following features:

- 2K Bytes ROM
- 256 Bytes RAM
- 1 Timer/Counter
- 4 8-Bit I/O Ports
- 1 6-Bit I/O Port
- 4 Interrupt Levels
- Serial In/Serial Out Ports

This minimum system, using the standard I/O technique is as shown in Figure 3.

In addition to standard I/O, the memory mapped I/O offers an efficient I/O addressing technique. With this technique, an area of memory address space is assigned for I/O address, thereby, using the memory address for I/O manipulation. Figure 4 shows the system configuration of Memory Mapped I/O using Am8085A.

The Am8085A CPU can also interface with the standard memory that does not have the multiplexed address/data bus. It will require a simple Am8212 (8-bit latch) as shown in Figure 5.

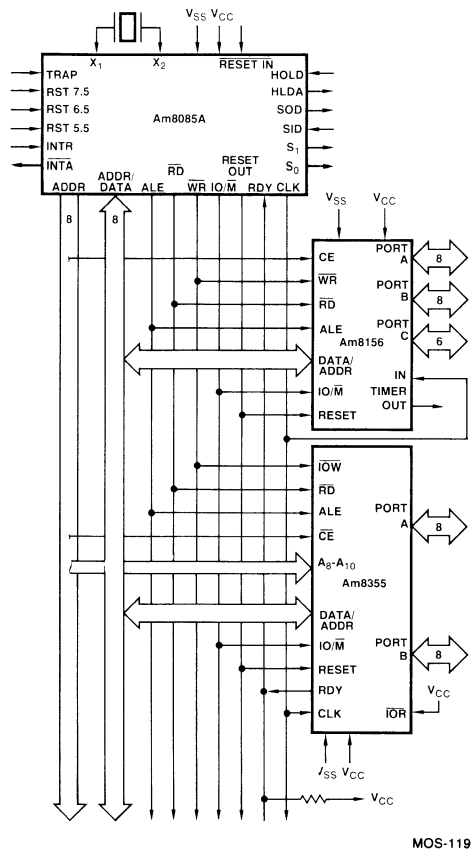

Figure 3. Am8085A Minimum System (Standard I/O Technique).

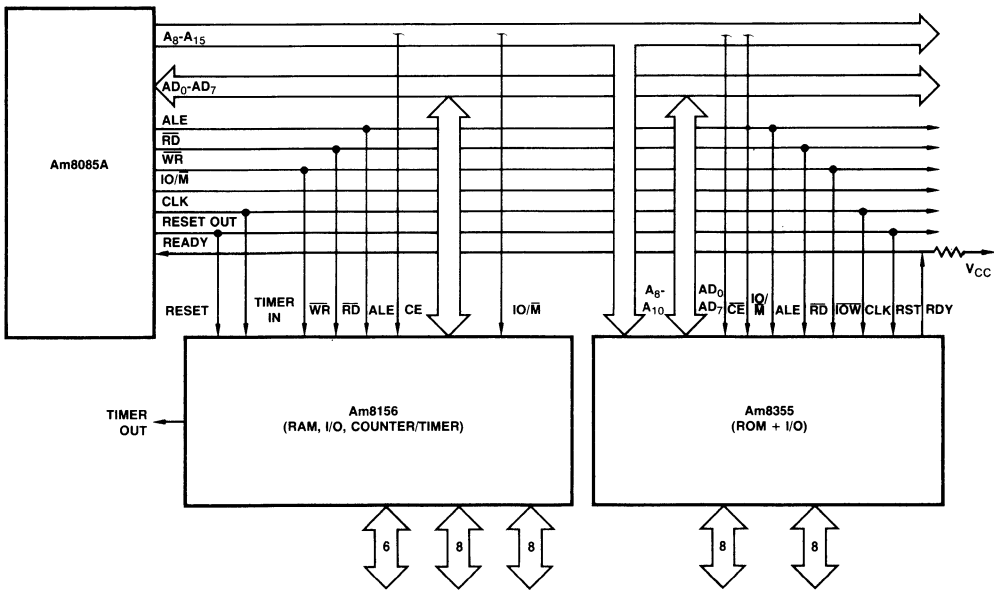

Figure 4. Minimum System (Memory Mapped I/O).

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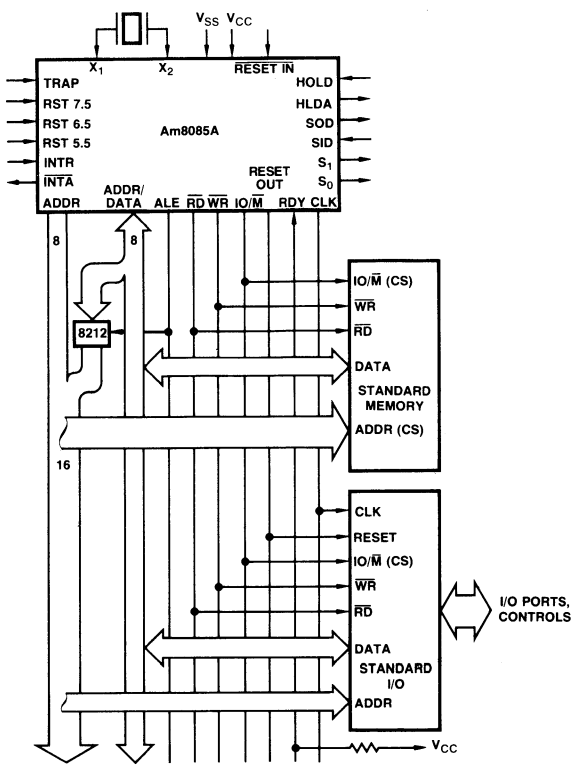

Figure 5. System Using Standard Memories.

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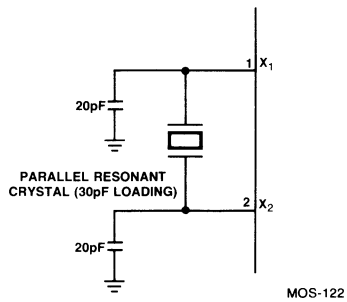
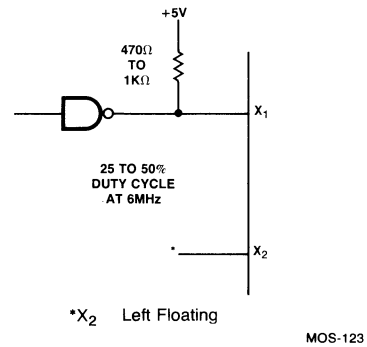
DRIVING THE X_1 AND X_2 INPUTS

The user may drive the X_1 and X_2 inputs of the Am8085A with a crystal, an external clock source or an RC network as shown below. The driving frequency must be twice the desired internal operating frequency (the Am8085A would require a 6MHz crystal for 3MHz internal operation).

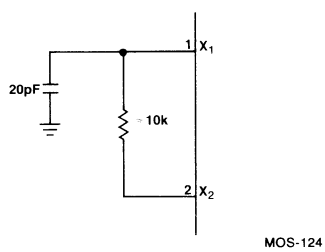


1-6 MHz Input Frequency

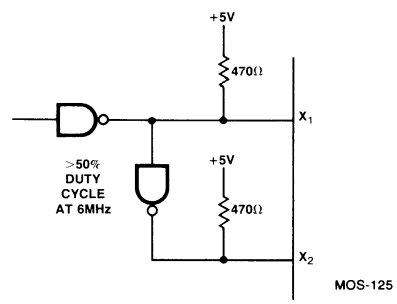


1-6 MHz Input Frequency

The 20pF capacitors are required to guarantee oscillation at the proper frequency during system startup.



≈3 MHz Input Frequency



≈6 MHz Input Frequency

RC Mode causes a large drift in clock frequency because of the variation in on-chip timing generation parameters. Use of RC Mode should be limited to an application which can tolerate a wide frequency variation.

Note: Duty cycle refers to the percentage of the clock input cycle when X_1 is high.

Figure 6. Driving the Clock Inputs (X_1 and X_2) of Am8085A.

GENERATING Am8085A WAIT STATE

The following circuit may be used to insert one WAIT state in each Am8085A machine cycle.

The D flip-flops should be chosen such that

- CLK is rising edge triggered
- CLEAR is low-level active.

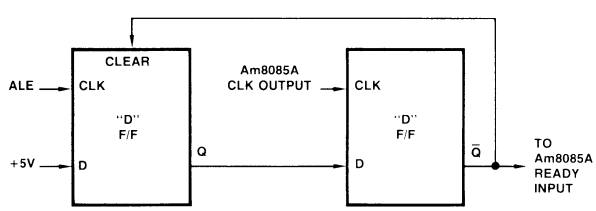


Figure 7. Generation of a Wait State for Am8085A CPU.

MOS-126

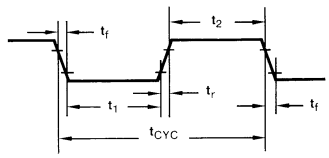
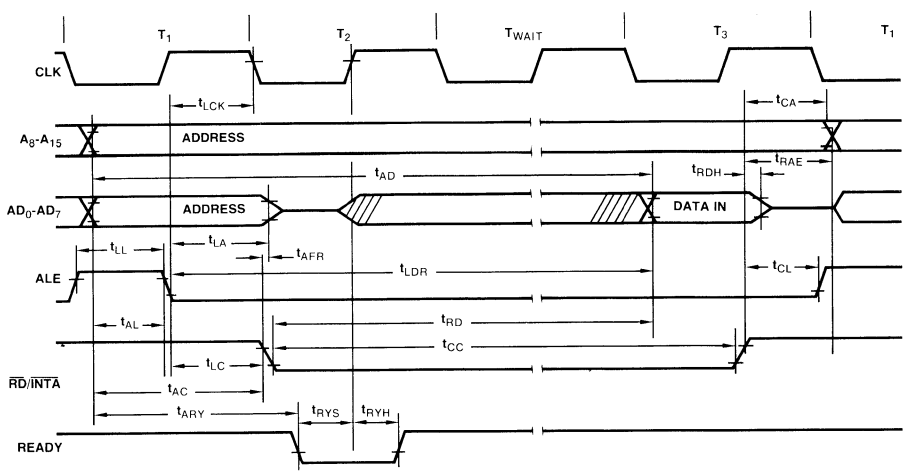


Figure 8. Clock Timing Waveform.

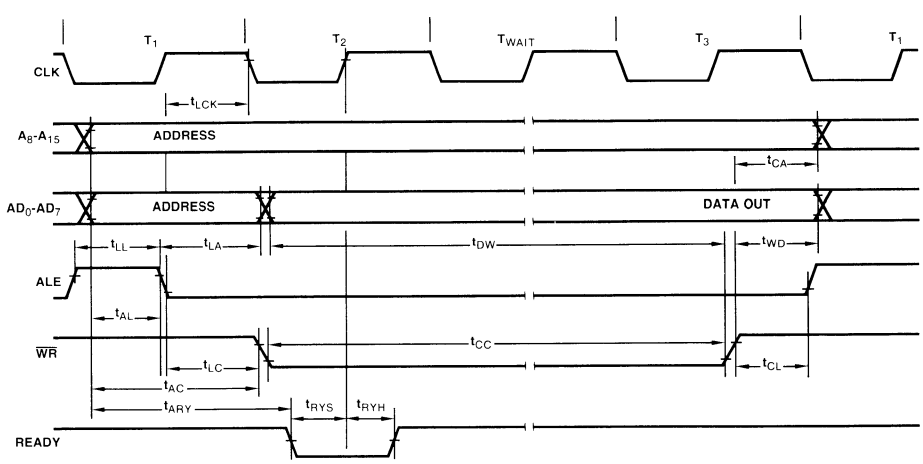
MOS-127

READ OPERATION



MOS-128

WRITE OPERATION



MOS-129

Figure 9. Am8085A Bus Timing.

HOLD OPERATION

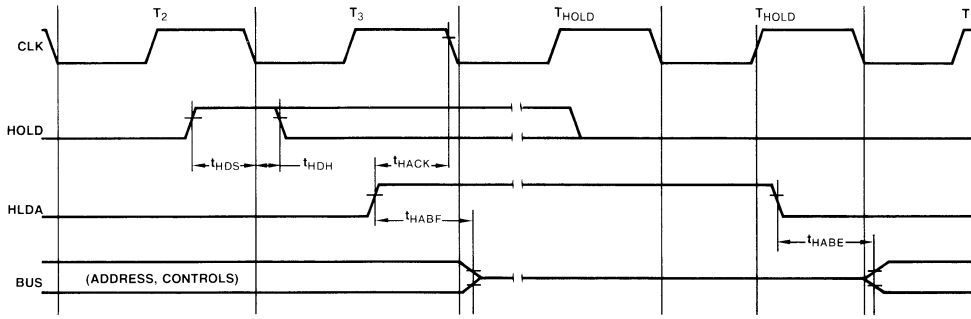


Figure 10. Am8085A Hold Timing.

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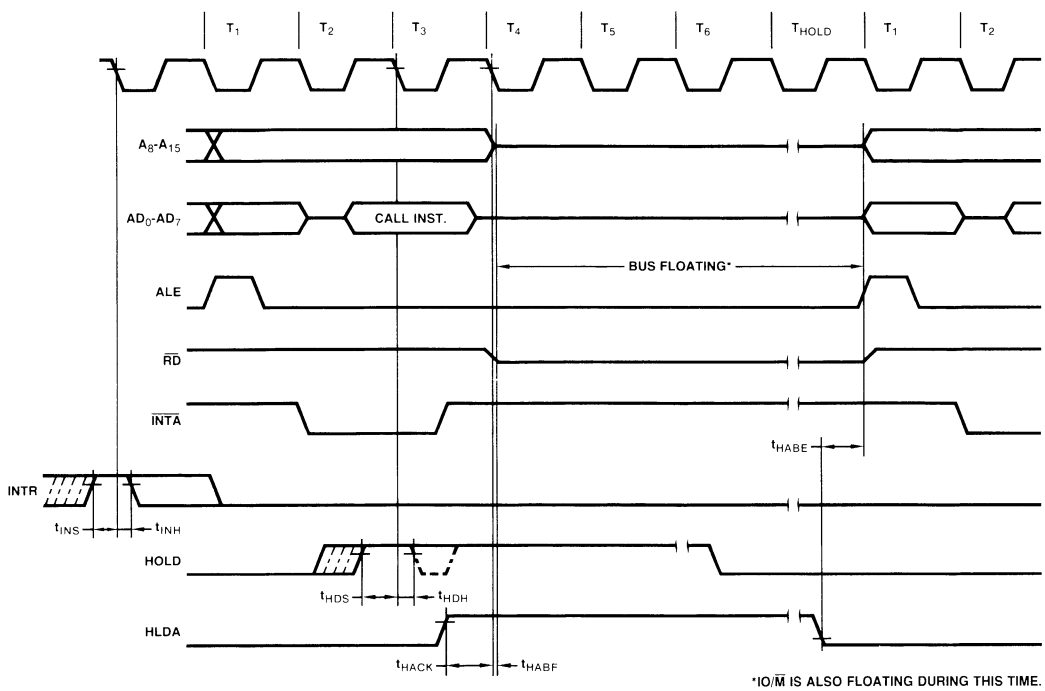

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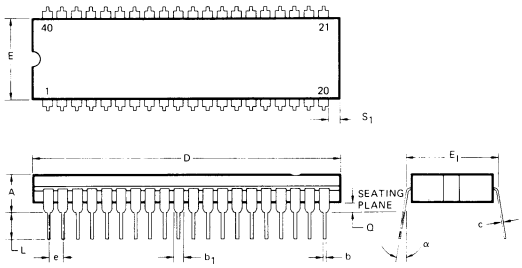
Figure 11. Am8085A Interrupt and Hold Timing.

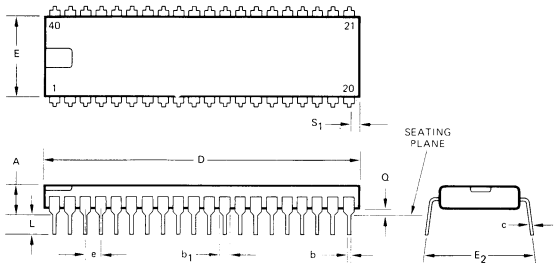
PHYSICAL DIMENSIONS

40-Pin Cerdip



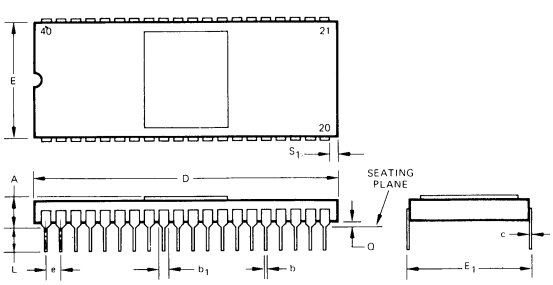
Reference Symbol	Inches	
	Min.	Max.
A	.150	.225
b	.016	.020
b_1	.045	.065
c	.009	.011
D	2.020	2.100
E	.510	.550
E_1	.600	.630
e	.090	.110
L	.120	.150
Q	.015	.060
S_1	.005	

40-Pin Molded DIP



Reference Symbol	Inches	
	Min.	Max.
A	.150	.200
b	.015	.020
b_1	.055	.065
c	.009	.011
D	2.050	2.080
E	.530	.550
E_2	.585	.700
e	.090	.110
L	.015	.060
Q	.015	.060
S_1	.040	.070

40-Pin Hermetic DIP



Reference Symbol	Inches	
	Min.	Max.
A	.100	.200
b	.015	.022
b_1	.030	.060
c	.008	.013
D	1.960	2.040
E	.550	.610
E_1	.590	.620
e	.090	.110
L	.120	.160
Q	.020	.060
S_1	.005	

Memories

Am9708/Am2708

1024 x 8 Erasable Read Only Memory

DISTINCTIVE CHARACTERISTICS

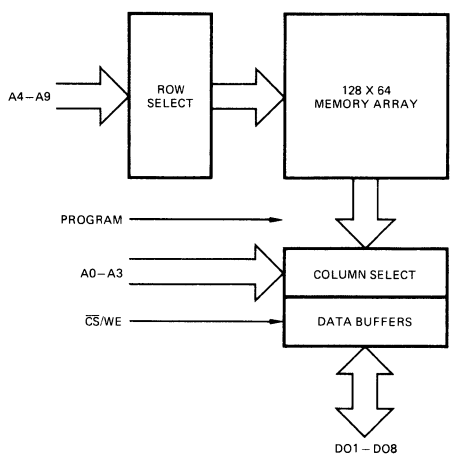
- Direct replacement for Intel 2708/8708
- Interchangeable with Am9208, Am9216 masked ROMs
- Full military temperature operation
- Fast programming time – typically 50 sec.
- TTL compatible interface signals
- Fully static operation – no clocks
- Fast access time – 450 ns
- Three-state outputs
- Tested for 100% programmability
- 100% MIL-STD-883 reliability assurance testing

GENERAL DESCRIPTION

The Am2708 is an 8,192-bit erasable and programmable MOS read-only memory. It is organized as 1024 words by 8 bits per word. Erasing the data in the EROM is accomplished by projecting ultra-violet light through a transparent sapphire lid for a predetermined time period.

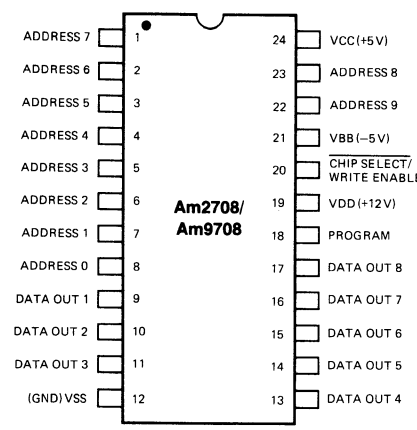
When the Chip Select/Write Enable input is at the high logic level, the device is unselected and the data lines are in their high impedance state. The device is selected when $\overline{CS}$/WE is at the low logic level. The contents of a particular memory location, specified by the 10 address lines, will be available on the data lines after the access time has elapsed. For programming, $\overline{CS}$/WE is connected to +12V and is used in conjunction with the Program input. The Address and Data lines are TTL compatible for all operating and programming modes.

BLOCK DIAGRAM



MOS-052

CONNECTION DIAGRAM



Top View

Pin 1 is marked for orientation.

MOS-053

ORDERING INFORMATION

Package Type	Ambient Temperature Specification	Order Number
Hermetic DIP/ Sapphire Lid	$0°C \leq T_A \leq +70°C$	AM2708DC B2708
Hermetic DIP/ Sapphire Lid	$-55°C \leq T_A \leq +125°C$	AM9708DM

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
All Signal Voltages, except Program and $\overline{CS}$/WE, with Respect to VBB	−0.3V to +15V
Program Input Voltage with Respect to VBB	−0.3V to +35V
$\overline{CS}$/WE Input with Respect to VBB	−0.3V to +20V
VCC and VSS with Respect to VBB	−0.3V to +15V
VDD with Respect to VBB	−0.3V to +20V
Power Dissipation	1.5W

The product described by this specification includes internal circuitry designed to protect input devices from excessive accumulation of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to any voltages that exceed the maximum ratings.

OPERATING RANGE

Ambient Temperature	VDD	VCC	VBB	VSS
0°C to +70°C	+12V ±5%	+5V ±5%	−5V ±5%	0V
−55°C to +125°C	+12V ±10%	+5V ±10%	−5V ±10%	0V

PROGRAMMING CONDITIONS

Ambient Temperature	VDD	VCC	VBB	VSS	$\overline{CS}$/WE	VIHP
+25°C	+12V ± 5%	+5V ± 5%	−5V ± 5%	0V	+12V ± 5%	26V ± 1V

ELECTRICAL CHARACTERISTICS over operating range (Note 1)

Parameters	Description	Test Conditions		Min.	Typ.	Max.	Units
VIL	Input LOW Voltage			VSS		0.65	Volts
VIH	Input HIGH Voltage	T_A = 0°C to +70°C		3.0		VCC+1	Volts
		T_A = −55°C to +125°C		2.4		VCC+1	Volts
VOL	Output LOW Voltage	IOL = 1.6mA				0.45	Volts
VOH	Output HIGH Voltage	IOH = − 100μA		3.7			Volts
		IOH = −1.0mA		2.4			Volts
ILI	Address and Chip Select Input Load Current	VSS ≤ VIN ≤ VCC			1.0	10	μA
ILO	Output Leakage Current	VOUT = Worst Case $\overline{CS}$/WE = + 5.0V			1.0	10	μA
IDD	VDD Supply Current	All inputs HIGH. $\overline{CS}$/WE = +5.0V	T_A = 0°C		50	65	mA
			T_A = −55°C			80	
ICC	VCC Supply Current		T_A = 0°C		6.0	10	mA
			T_A = −55°C			15	
IBB	VBB Supply Current		T_A = 0°C		30	45	mA
			T_A = −55°C			60	
PD	Power Dissipation	T_A = 70°C				800	mW
CIN	Input Capacitance	T_A = 25°C f = 1MHz All pins at 0V			4.0	6.0	pF
COUT	Output Capacitance				8.0	12.0	pF

SWITCHING CHARACTERISTICS over operating range (Note 2)

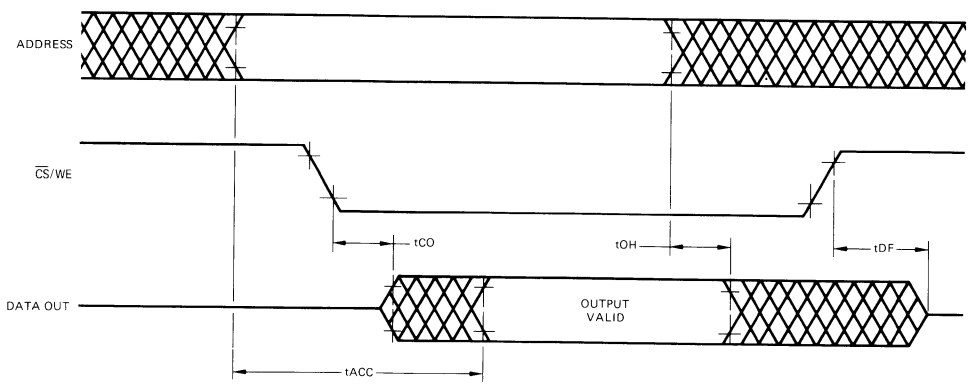
Parameters	Description	Test Conditions	0°C ≤ T_A ≤ 70°C		−55°C ≤ T_A ≤ +125°C		Units
			Min.	Max.	Min.	Max.	
tACC	Address to Output Access Time (Note 3)	tr = tf ≤ 20ns Output Load: One Standard TTL Gate Plus 100pF		450		480	ns
tCO	Chip Select to Output on Delay (Note 4)			120		150	ns
tDF	Chip Select to Output OFF Delay		0	120	0	150	
tOH	Previous Read Data Valid with Respect to Address Change		0		0		

PROGRAMMING CHARACTERISTICS under programming conditions

Parameter	Description	Min.	Max.	Units
tAS	Address Set Up Time	10		µs
tCSS	$\overline{CS}$/WE Set Up Time	10		µs
tDS	Data Set Up Time	10		µs
tAH	Address Hold Time (Note 5)	1.0		µs
tCH	$\overline{CS}$/WE Hold Time (Note 5)	0.5		µs
tDH	Data Hold Time	1.0		µs
tDF	Chip Select to Output Off Delay	0	120	ns
tDPR	Program to Read Delay		10	µs
tPW	Program Pulse Width	0.1	1.0	ms
tPR, tPF	Program Pulse Transition Times	0.5	2.0	µs
VIHW	$\overline{CS}$/WE Input High Level	11.4	12.6	Volts
VIHP	Program Pulse High Level (Note 6)	25	27	Volts
VILP	Program Pulse Low Level (Note 6)	VSS	1.0	Volts

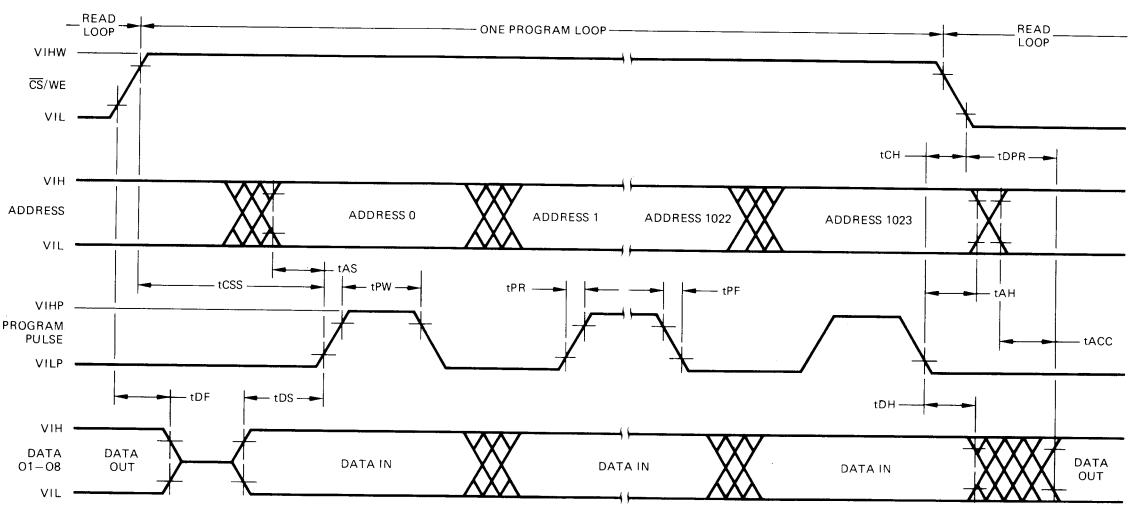
SWITCHING WAVEFORMS

READ CYCLE



MOS-054

PROGRAM MODE (Note 5)



MOS-055

PROGRAMMING THE Am2708

All 8192 bits of the Am2708 are in the logic HIGH state after erasure. When any of the output bits are programmed, the output state will change from HIGH to LOW. Programming of the device is initiated by raising the $\overline{CS}$/WE input to +12V. A memory location is programmed by addressing the device and supplying 8 data bits in parallel to the data out lines. When address and data bits are set up, a programming pulse is applied to the program input. All addresses are programmed sequentially in a similar manner. One pass through all 1024 addresses is considered one program loop. The number of program loops (N) required to complete the programming cycle is a function of the program pulse width (tPW) such that $N \geqslant 100ms/tPW$ requirement is met. Do not apply more than one program pulse per address without sequentially programming all other addresses. There should be N successive loops through all locations. The Program pin will source the IIPL current when it is low (VILP) and $\overline{CS}$/WE is high (VIHW). The Program pin should be actively pulled down to maintain its low level.

ERASING THE Am2708

The Am2708 can be erased by exposing the die to high-intensity, short-wave, ultra-violet light at a wavelength of 2537 angstroms through the transparent lid. The recommended dosage is ten watt-seconds per square centimeter. This erasing condition can be obtained by exposing the die to model S-52 ultraviolet lamp manufactured by Ultra-Violet Products, Inc. or Product Specialties, Inc. for approximately 20 to 30 minutes from a distance of about 2.5 centimeters above the transparent lid. The light source should not be operated with a short-wave filter installed. All bits will be in a logic HIGH state when erasure is complete.

CAUTION

Ultraviolet radiation is invisible and can damage human eyes. Precautions should be taken to avoid exposure to direct or reflected ultraviolet radiation. It will often be convenient to fully enclose the ultraviolet source and the EROMs being erased to prevent accidental exposure.

Ultraviolet lamps can also ionize oxygen and create ozone which can be harmful to humans. Erasing should be carried out in a well ventilated area in order to minimize the concentration of ozone.

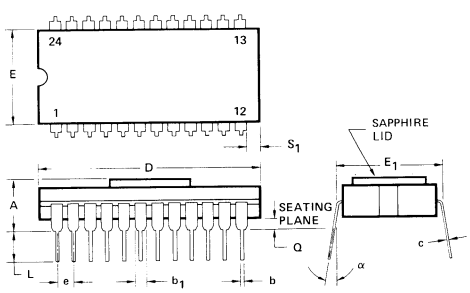
NOTES:

1. Typical values are for $T_A = 25^\circ C$, nominal supply voltages and nominal processing parameters.
2. Timing reference levels (Read) –
   Inputs: High = 2.8V (DC), 2.2V (DM); Low = 0.8V
   Outputs: High = 2.4V, Low = 0.8V
3. Typical access time is 280ns.
4. Typical chip select to output on delay is 60ns.
5. tAH must be greater than tCH.
6. VIHP – VILP ⩾ 25 Volts.

PHYSICAL DIMENSIONS

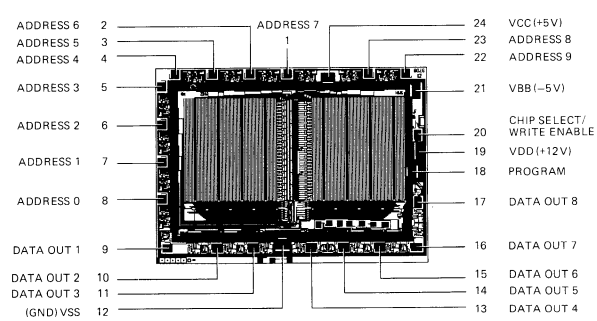
Dual-In-Line

24-Pin Cerdip



Reference Symbol	Inches	
	Min.	Max.
A	.150	.225
b	.016	.020
b_1	.045	.065
c	.009	.011
D	1.230	1.240
E	.510	.550
E_1	.600	.630
e	.090	.110
L	.120	.150
Q	.015	.050
S_1	.010	
α	3°	13°

Metallization and Pad Layout



DIE SIZE 0.195" X 0.139"

Am27S18 • Am27S19

256-Bit Generic Series Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- High Speed – 40ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures.

FUNCTIONAL DESCRIPTION

The Am27S18 and Am27S19 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 32 x 8 configuration, they are available in both open collector Am27S18 and three-state Am27S19 output versions. After programming, stored information is read on outputs O_0-O_7 by applying unique binary addresses to A_0-A_4 and holding the chip select input, $\overline{CS}$, at a logic LOW. If the chip select input goes to a logic HIGH, O_0-O_7 go to the off or high impedance state.

GENERIC SERIES CHARACTERISTICS

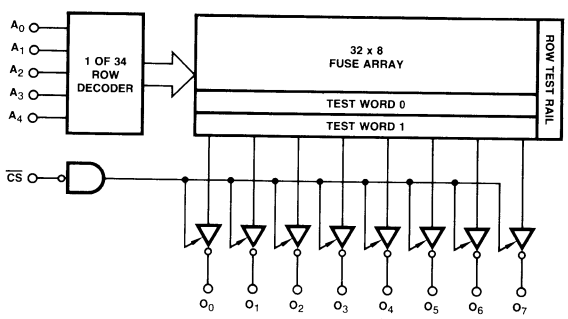
The Am27S18 and Am27S19 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliabilty. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

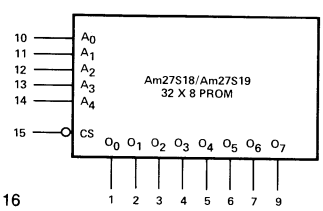
Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

BLOCK DIAGRAM



BPM-018

LOGIC SYMBOL



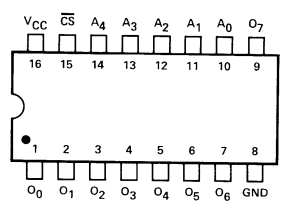
V_{CC} = Pin 16
GND = Pin 8

BPM-019

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Open Collectors		
Hermetic DIP	0°C to +75°C	AM27S18DC
Hermetic DIP	−55°C to +125°C	AM27S18DM
Hermetic Flat Pak	−55°C to +125°C	AM27S18FM
Three-State Outputs		
Hermetic DIP	0°C to +75°C	AM27S19DC
Hermetic DIP	−55°C to +125°C	AM27S19DM
Hermetic Flat Pak	−55°C to +125°C	AM27S19FM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BPM-020

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	Am27S18XC, Am27S19XC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	Am27S18XM, Am27S19XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am27S19 only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V		−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			25	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC} (Am27S19 only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)	−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		90	115	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; V_O = 4.5V			40	μA
		V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; Am27S19 only; V_O = 2.4V			40	μA
		V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; Am27S19 only; V_O = 0.4V			−40	μA
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz (Note 3)		4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz (Note 3)		8		pF

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but periodically sampled.

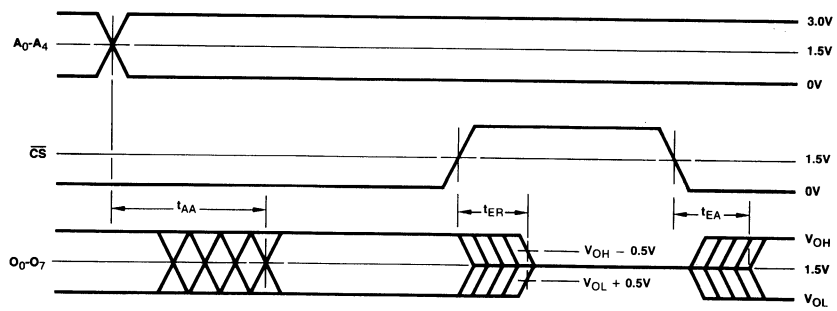
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PRELIMINARY DATA

Parameter	Description	Test Conditions	Typ. 5V 25°C	Max. 5V 25°C	Max. COM'L	Max. MIL	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1–3)	25	35	40	50	ns
t_{EA}	Enable Access Time		15	20	25	30	ns
t_{ER}	Enable Recovery Time		15	20	25	30	ns

Notes:
1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} – 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

SWITCHING WAVEFORMS



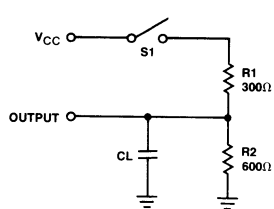
Note: Level on output while $\overline{CS}$ is HIGH is determined externally.

BPM-021

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS	WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY		DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L		DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H			

AC TEST LOAD



BPM-022

PROGRAMMING

The Am27S18 and Am27S19 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip enabled, and the output level sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

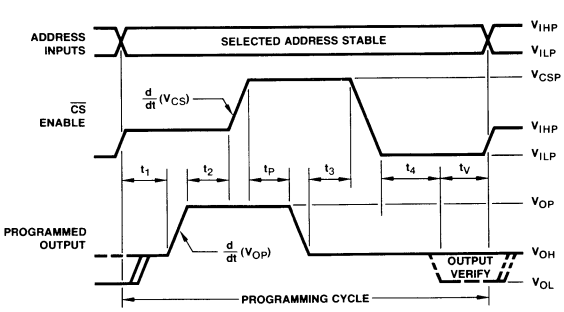
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	$\overline{CS}$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP}+0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{CS})/dt$	Rate of $\overline{CS}$ Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

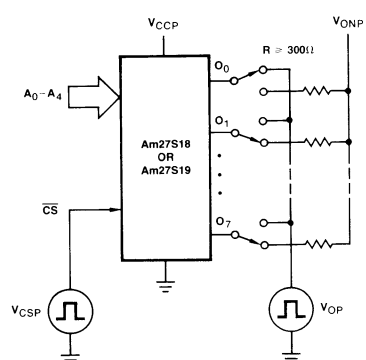
Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-023

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-024

PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27S18 • Am27S19 ADAPTERS AND CONFIGURATOR	715-1407-1	PA16-2 and 32 x 8 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 32 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of eight Ps or Ns, starting with output O_7.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the eight Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

TYPICAL PAPER TAPE FORMAT

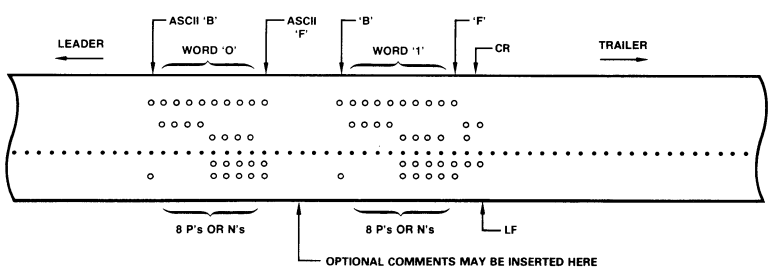
```
ØØØ   BPNPPNNNPF   WORD ZERO (R) (L)
      BPPPPPPNNF   COMMENT FIELD (R) (L)
ØØ2   BNNNPPPPNF   ANY (R) (L)
      BNNNNNNNNF   TEXT (R) (L)
ØØ4   BPNNNNNNPF   CAN (R) (L)
      BNPPNPPNNF   GO (R) (L)
ØØ6   BPNNPPPNNF   HERE (R) (L)
 :         :           :
Ø31   BNNNNPPPNF   END (R) (L)
```

(R) = CARRIAGE RETURN
(L) = LINE FEED

RESULTING DEVICE TRUTH TABLE ($\overline{CS}$ = LOW)

A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
L	L	L	L	L	H	L	H	H	L	L	L	H
L	L	L	L	H	H	H	H	H	H	H	L	L
L	L	L	H	L	L	L	L	H	H	H	H	L
L	L	L	H	H	L	L	L	L	L	L	L	L
L	L	H	L	L	H	L	L	L	L	L	L	H
L	L	H	L	H	L	H	H	L	H	H	L	L
L	L	H	H	L	H	L	L	H	H	H	L	L
		⋮						⋮				
H	H	H	H	H	L	L	L	L	H	H	H	L

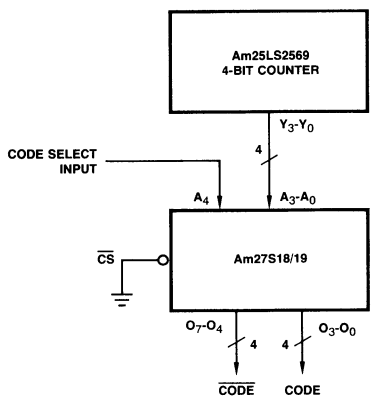
ASCII PAPER TAPE



BPM-025

APPLYING THE Am27S18 AND Am27S19

The Am27S18 and Am27S19 PROMs may be used as code converters. Examples include conversion of hexadecimal, octal or BCD to seven segment display drive format. In many code conversion applications an extra PROM address input is available and may be used as a polarity control, blanking control or code selector input. The use of a single Am27S18 or Am27S19 to convert the outputs of a binary counter to either excess three or gray code format is illustrated below. In this case both codes are generated in true and complemented form simultaneously.



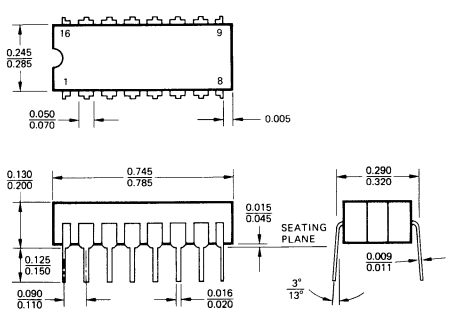
BPM-026

TRUTH TABLE

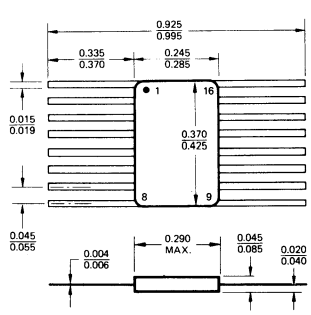
ADDRESS					COMPLEMENT				TRUE				
A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	
0	0	0	0	0	1	1	0	0	0	0	1	1	EXCESS THREE CODE
0	0	0	0	1	1	0	1	1	0	1	0	0	
0	0	0	1	0	1	0	1	0	0	1	0	1	
0	0	0	1	1	1	0	0	1	0	1	1	0	
0	0	1	0	0	1	0	0	0	0	1	1	1	
0	0	1	0	1	0	1	1	1	1	0	0	0	
0	0	1	1	0	0	1	1	0	1	0	0	1	
0	0	1	1	1	0	1	0	1	1	0	1	0	
0	1	0	0	0	0	1	0	0	1	0	1	1	
0	1	0	0	1	0	0	1	1	1	1	0	0	
0	1	0	1	0	X	X	X	X	X	X	X	X	
0	1	0	1	1	X	X	X	X	X	X	X	X	
0	1	1	0	0	X	X	X	X	X	X	X	X	
0	1	1	0	1	X	X	X	X	X	X	X	X	
0	1	1	1	0	X	X	X	X	X	X	X	X	
0	1	1	1	1	X	X	X	X	X	X	X	X	
1	0	0	0	0	1	1	1	1	0	0	0	0	GRAY CODE
1	0	0	0	1	1	1	1	0	0	0	0	1	
1	0	0	1	0	1	1	0	0	0	0	1	1	
1	0	0	1	1	1	1	0	1	0	0	1	0	
1	0	1	0	0	1	0	0	1	0	1	1	0	
1	0	1	0	1	1	0	0	0	0	1	1	1	
1	0	1	1	0	1	0	1	0	0	1	0	1	
1	0	1	1	1	1	0	1	1	0	1	0	0	
1	1	0	0	0	0	0	1	1	1	1	0	0	
1	1	0	0	1	0	0	1	0	1	1	0	1	
1	1	0	1	0	0	0	0	0	1	1	1	1	
1	1	0	1	1	0	0	0	1	1	1	1	0	
1	1	1	0	0	0	1	0	1	1	0	1	0	
1	1	1	0	1	0	1	0	0	1	0	1	1	
1	1	1	1	0	0	1	1	0	1	0	0	1	
1	1	1	1	1	0	1	1	1	1	0	0	0	

PHYSICAL DIMENSIONS
Dual-In-Line

16-Pin Ceramic



16-Pin Flat Package



Am27S20 • Am27S21

1024-Bit Generic Series Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- High Speed – 45ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures.

GENERIC SERIES CHARACTERISTICS

The Am27S20 and Am27S21 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliabilty. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

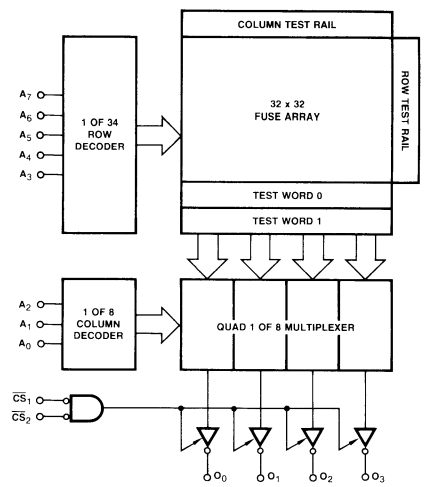
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Open Collectors		
Hermetic DIP	0°C to +75°C	AM27S20DC
Hermetic DIP	−55°C to +125°C	AM27S20DM
Hermetic Flat Pak	−55°C to +125°C	AM27S20FM
Three-State Outputs		
Hermetic DIP	0°C to +75°C	AM27S21DC
Hermetic DIP	−55°C to +125°C	AM27S21DM
Hermetic Flat Pak	−55°C to +125°C	AM27S21FM

FUNCTIONAL DESCRIPTION

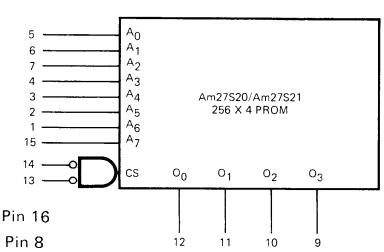
The Am27S20 and Am27S21 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 256 x 4 configuration, they are available in both open collector Am27S20 and three-state Am27S21 output versions. After programming, stored information is read on outputs O_0-O_3 by applying unique binary addresses to A_0-A_7 and holding the chip select inputs, $\overline{CS}_1$ and $\overline{CS}_2$, at a logic LOW. If either chip select input goes to a logic HIGH, O_0-O_3 go to the off or high impedance state.

BLOCK DIAGRAM



BPM-027

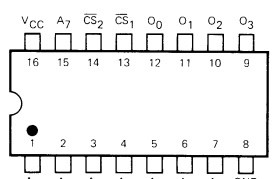
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

BPM-028

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BPM-029

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	Am27S20XC, Am27S21XC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	Am27S20XM, Am27S21XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am27S21 only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V		−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			25	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC} (Am27S21 only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)	−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		95	130	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX., $V_{\overline{CS1}}$ = 2.4V; Am27S21 only; V_O = 4.5V			40	µA
		V_{CC} = MAX., $V_{\overline{CS1}}$ = 2.4V; Am27S21 only; V_O = 2.4V			40	µA
		V_{CC} = MAX., $V_{\overline{CS1}}$ = 2.4V; Am27S21 only; V_O = 0.4V			−40	µA
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz (Note 3)		4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz (Note 3)		8		pF

Note 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C

2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

3. These parameters are not 100% tested, but are periodically sampled.

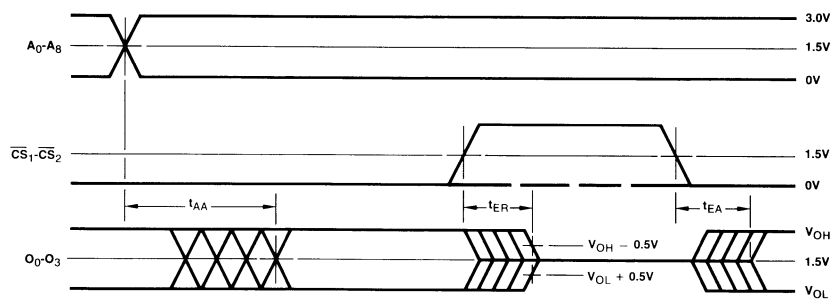
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PRELIMINARY DATA

Parameter	Description	Test Conditions	Typ. 5V 25°C	Max. 5V 25°C	Max. COM'L	Max. MIL	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1–3)	25	35	45	60	ns
t_{EA}	Enable Access Time		15	18	20	30	ns
t_{ER}	Enable Recovery Time		15	18	20	30	ns

Notes:
1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} – 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

SWITCHING WAVEFORMS



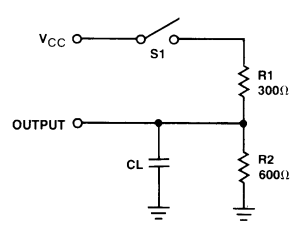
Note: Level on output while either $\overline{CS}$ is HIGH is determined externally.

BPM-030

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS	WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY	▒▒▒	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
▒▒▒	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L	><><	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE
▒▒▒	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H			

AC TEST LOAD



BPM-031

PROGRAMMING

The Am27S20 and Am27S21 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}_1$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}_1$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip enabled, and the output level sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}_1$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

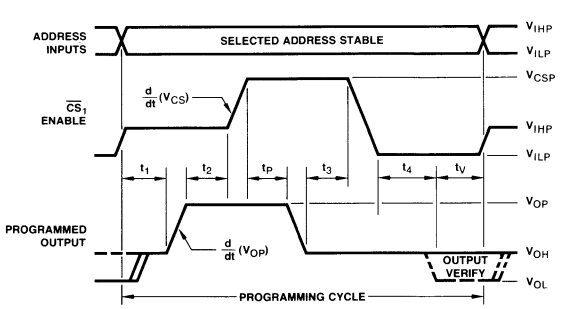
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	$\overline{CS}_1$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	$V_{CCP}+0.3$	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{CS})/dt$	Rate of $\overline{CS}_1$, Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

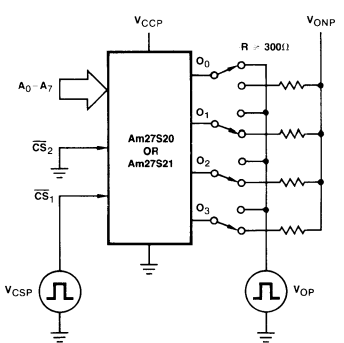
Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During t_v, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-032

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-033

PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27S20 • Am27S21 ADAPTERS AND CONFIGURATOR	715-1408-1	PA16-1 and 256 x 4 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 256 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of four Ps or Ns, starting with output O_3.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the four Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

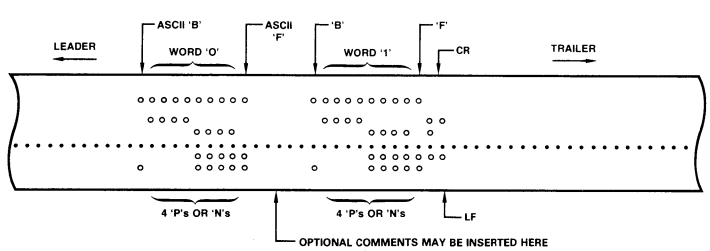
TYPICAL PAPER TAPE FORMAT

```
ØØØ   BNNNPF   WORD ZERO (R) (L)
      BPPNNF   COMMENT FIELD (R) (L)
ØØ2   BPPPNF   ANY (R) (L)
      BNNNNF   TEXT (R) (L)
ØØ4   BNNNPF   CAN (R) (L)
      BPPNNF   GO (R) (L)
ØØ6   BPPNNF   HERE (R) (L)
 :     ::::::    :
255   BPPPNF   END (R) (L)
```

RESULTING DEVICE TRUTH TABLE ($\overline{CS}_1$ & $\overline{CS}_2$ = LOW)

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_3	O_2	O_1	O_0
L	L	L	L	L	L	L	L	L	L	L	H
L	L	L	L	L	L	L	H	H	H	L	L
L	L	L	L	L	L	H	L	H	H	H	L
L	L	L	L	L	L	H	H	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	H
L	L	L	L	L	H	L	H	H	H	L	L
L	L	L	L	L	H	H	L	H	H	L	L
				⋮					⋮		
H	H	H	H	H	H	H	H	H	H	H	L

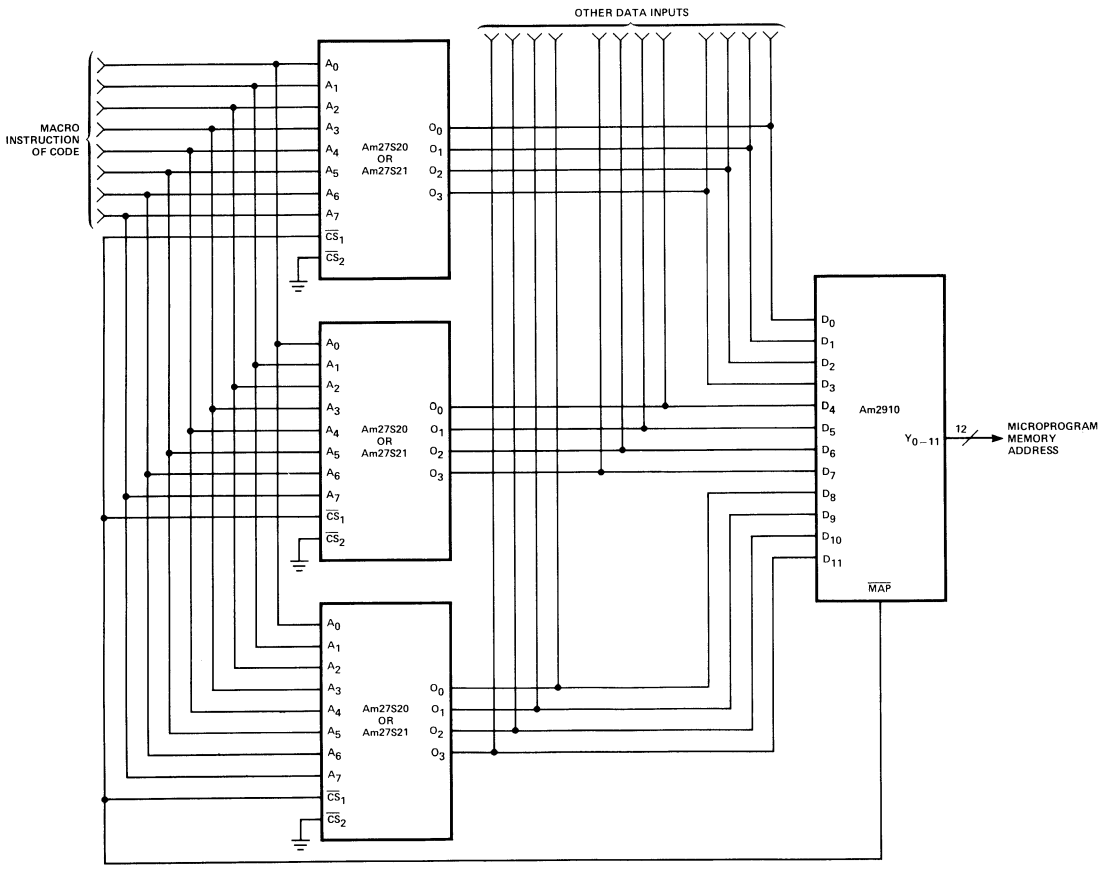
ASCII PAPER TAPE



BPM-034

APPLYING THE Am27S20/21

Typical application of the Am27S20/21 is shown below. The Am27S20/21's are employed as mapping ROMs in a microprogram computer control unit. The eight-bit macroinstruction from main memory is brought into the A_{0-7} inputs of the mapping ROM array. The instruction is mapped into a 12-bit address space with each PROM output supplying 4 bits. The 12 bits of address are then supplied to the "D" inputs of the Am2910 as a possible next address source for microprogram memory. The $\overline{MAP}$ output of the Am2910 is connected to the $\overline{CS}_1$ input of the Am27S20/21 such that when the $\overline{CS}_1$ input is HIGH, the outputs of the PROMs are either HIGH in the case of the Am27S20 or in the three-state mode in the case of the Am27S21. In both cases the $\overline{CS}_2$ input is grounded, thus data from other sources are free to drive the D inputs of the Am2910 when $\overline{MAP}$ is HIGH.

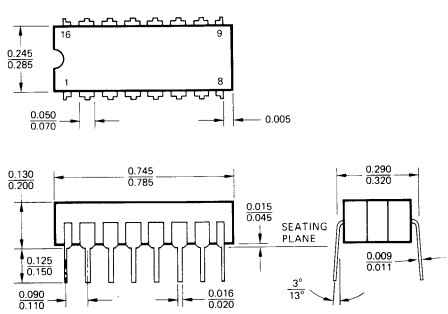


MICROPROGRAMMING INSTRUCTION MAPPING

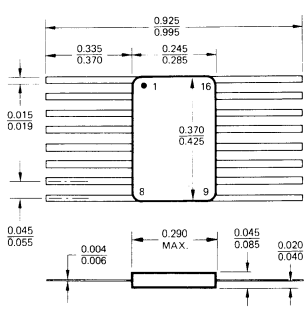
BPM-035

PHYSICAL DIMENSIONS
Dual-In-Line

16-Pin Ceramic



16-Pin Flat Package



Am27S12 • Am27S13

2048-Bit Generic Series Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- High Speed – 50ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures.

GENERIC SERIES CHARACTERISTICS

The Am27S12 and Am27S13 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliabilty. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

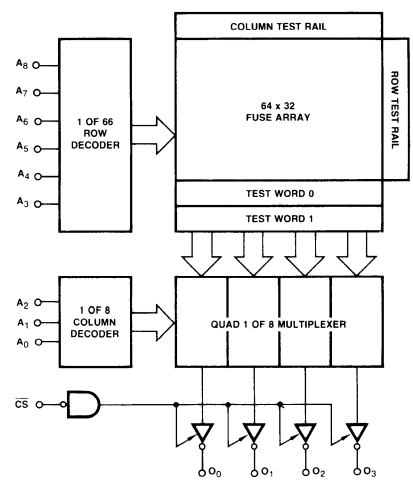
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Open Collectors		
Hermetic DIP	0°C to +75°C	AM27S12DC
Hermetic DIP	−55°C to +125°C	AM27S12DM
Hermetic Flat Pak	−55°C to +125°C	AM27S12FM
Three-State Outputs		
Hermetic DIP	0°C to +75°C	AM27S13DC
Hermetic DIP	−55°C to +125°C	AM27S13DM
Hermetic Flat Pak	−55°C to +125°C	AM27S13FM

FUNCTIONAL DESCRIPTION

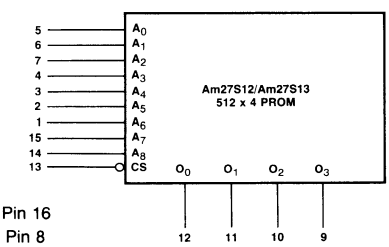
The Am27S12 and Am27S13 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 512 x 4 configuration, they are available in both open collector Am27S12 and three-state Am27S13 output versions. After programming, stored information is read on outputs O_0-O_3 by applying unique binary addresses to A_0-A_8 and holding the chip select input, $\overline{CS}$, at a logic LOW. If the chip select input goes to a logic HIGH, O_0-O_3 go to the off or high impedance state.

BLOCK DIAGRAM



BPM-001

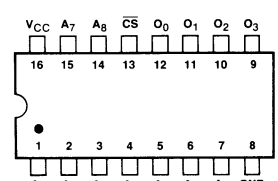
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

BPM-002

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BPM-003

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	Am27S12XC, Am27S13XC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	Am27S12XM, Am27S13XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am27S13 only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V		−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			25	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC} (Am27S13 only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)	−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		100	130	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; V_O = 4.5V			40	µA
		V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; Am27S13 only; V_O = 2.4V			40	µA
		V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; Am27S13 only; V_O = 0.4V			−40	µA
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz (Note 3)		4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz (Note 3)		8		pF

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.

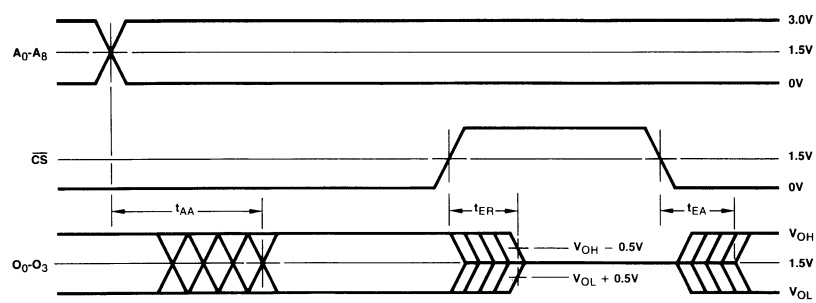
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PRELIMINARY DATA

Parameter	Description	Test Conditions	Typ. 5V 25°C	Max. 25°C	Max. COM'L	Max. MIL	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1-3)	30	45	50	60	ns
t_{EA}	Enable Access Time		15	20	25	30	ns
t_{ER}	Enable Recovery Time		15	20	25	30	ns

Notes:
1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} − 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

SWITCHING WAVEFORMS



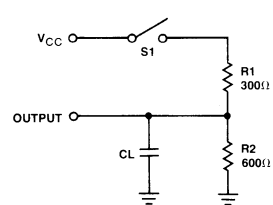
Note: Level on output while $\overline{CS}$ is HIGH is determined externally.

BPM-004

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS	WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY		DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L		DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H			

AC TEST LOAD



BPM-005

PROGRAMMING

The Am27S12 and Am27S13 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip enabled, and the output level sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycle. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

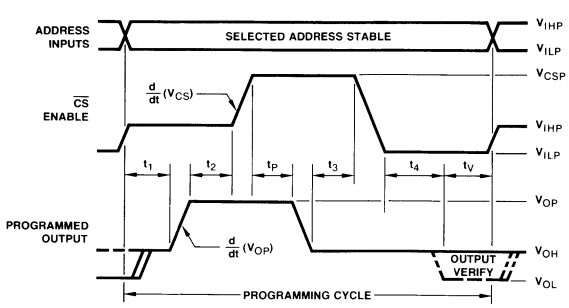
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	CS Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP}+0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{CS})/dt$	Rate of CS Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

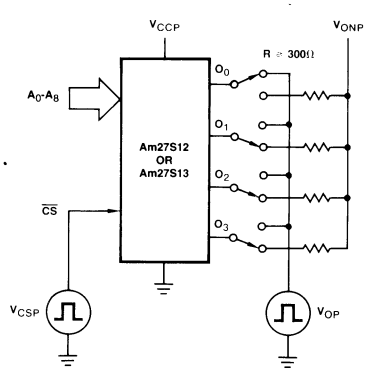
Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During t_v, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-006

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-007

PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27S12 • Am27S13 ADAPTERS AND CONFIGURATOR	715-1407-2	PA16-2 and 512 x 4 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 512 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of four Ps or Ns, starting with output O_3.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the four Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

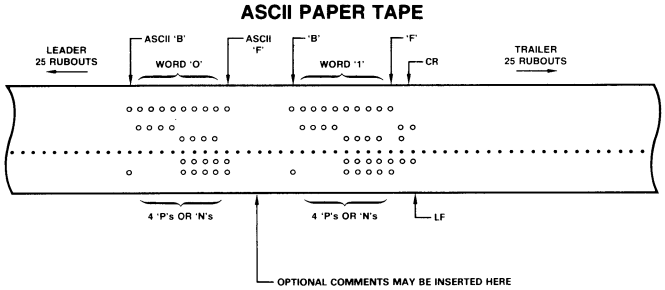
TYPICAL PAPER TAPE FORMAT

```
ØØØ   BNNNPF   WORD ZERO (R) (L)
      BPPNNF   COMMENT FIELD (R) (L)
ØØ2   BPPPNF   ANY (R) (L)
      BNNNNF   TEXT (R) (L)
ØØ4   BNNNPF   CAN (R) (L)
      BPPNNF   GO (R) (L)
ØØ6   BPPNNF   HERE (R) (L)
 .     .....     .
 .     .....     .
 .     .....     .
511   BPPPNF   END (R) (L)
```

RESULTING DEVICE TRUTH TABLE ($\overline{CS}$ = LOW)

A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_3	O_2	O_1	O_0
L	L	L	L	L	L	L	L	L	L	L	L	H
L	L	L	L	L	L	L	L	H	H	H	L	L
L	L	L	L	L	L	L	H	L	H	H	H	L
L	L	L	L	L	L	L	H	H	L	L	L	L
L	L	L	L	L	L	H	L	L	L	L	L	H
L	L	L	L	L	L	H	L	H	H	H	L	L
L	L	L	L	L	L	H	H	L	H	H	L	L
					⋮							
H	H	H	H	H	H	H	H	H	H	H	H	L

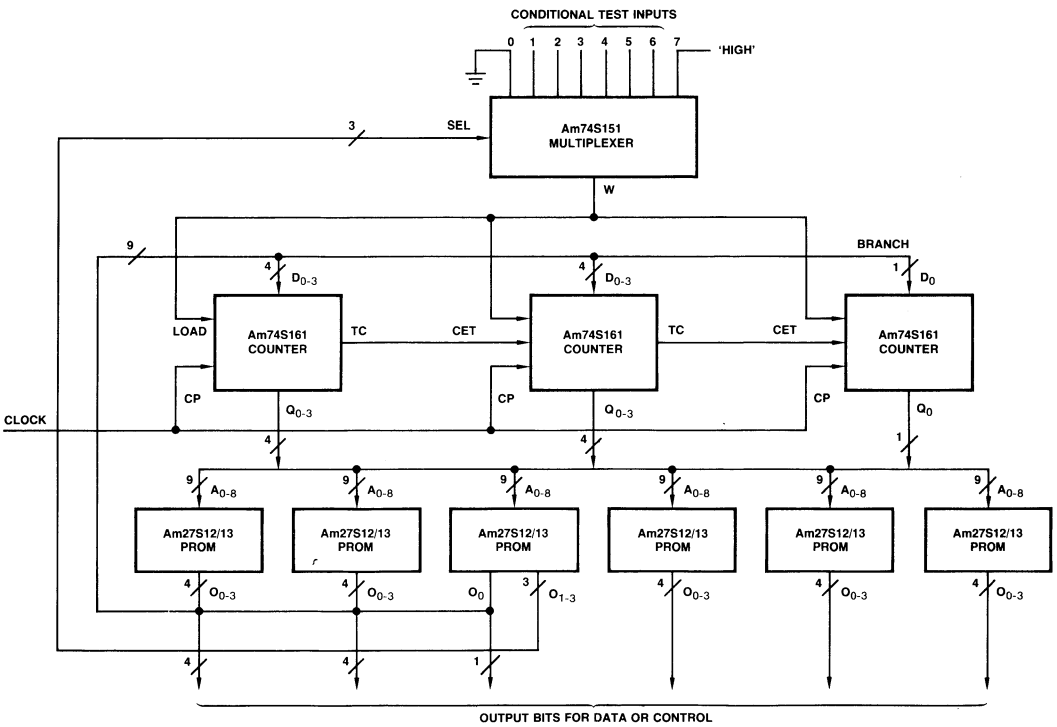
ASCII PAPER TAPE



BPM-008

APPLYING THE Am27S12 AND Am27S13

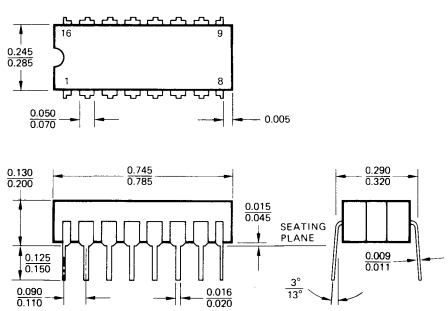
The Am27S12 and Am27S13 can be used with a high speed counter to form a pico-controller for microprogrammed systems. A typical application is illustrated below wherein a multiplexer, under control of one of the PROMs, is continuously sensing the CONDITIONAL TEST INPUTS. When the selected condition occurs, a HIGH signal will result at the multiplexer output causing a predetermined branch address to be loaded into the parallel inputs of the counters on the next clock pulse. The counter then accesses the preprogrammed data or control information sequence from the Am27S12 or Am27S13 PROMs.



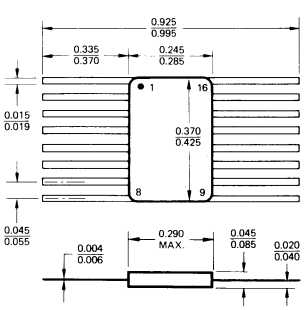
BPM-009

PHYSICAL DIMENSIONS
Dual-In-Line

16-Pin Ceramic



16-Pin Flat Package



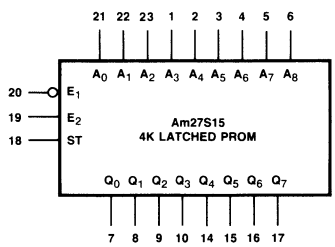
Am27S15

4096-Bit Generic Series Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- On-chip data latches
- Latched true and complemented output enables for easy word expansion
- Predetermined OFF outputs on power-up
- Plug-in replacement for the 82S115
- Fast access time – 60ns commercial and 90ns military maximum
- Performance pretested with N^2 patterns
- Highly reliable, ultra-fast programming Platinum-Silicide fuses – High programming yield
- Low current PNP inputs
- High current three-state outputs
- Common Generic PROM Series characteristics and programming procedures

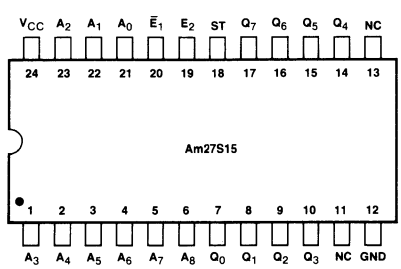
LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12
(Pins 11 and 13 open)

BPM-010

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.
NC = No connection.

BPM-011

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	0°C to +75°C	Am27S15DC
Hermetic DIP	−55°C to +125°C	Am27S15DM

FUNCTIONAL DESCRIPTION

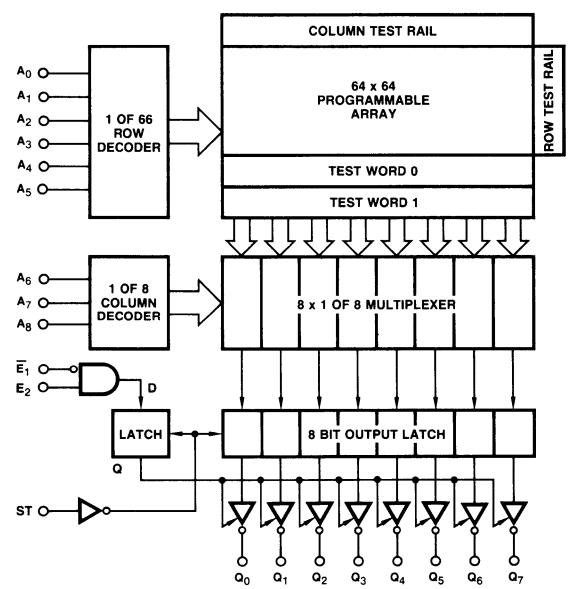
The Am27S15 is an electrically programmable Schottky read only memory incorporating on-chip data and enable latches. The device is organized as 512 words of 8 bits and features three-state outputs with full 16mA drive capability.

When in the transparent mode, with the strobe (ST) input HIGH, reading stored data is accomplished by enabling the chip ($\overline{E}_1$ LOW and E_2 HIGH) and applying the binary word address to the address inputs, A_0-A_8. In this mode, changes of the address inputs cause the outputs, Q_0-Q_7, to read a different stored word; changes of either enable input level disable the outputs, causing them to go to the high impedance state.

Dropping the strobe input to the LOW level places the device in the latched mode of operation. The output condition present (reading a word of stored data or disabled) when the strobe goes LOW remains at the outputs, regardless of further address or enable transitions, until a positive (LOW to HIGH) strobe transition occurs. With the strobe HIGH, Q_0-Q_7 again respond to the address and enable input conditions.

If the strobe is LOW (latched mode) when V_{CC} power is first applied, the outputs will be in the disabled state, eliminating the need for special "power-up" design precautions.

BLOCK DIAGRAM



BPM-012

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC}(max)
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration = 1sec)	200mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	Am27S15XC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	Am27S15XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA, V_{IN} = V_{IH} or V_{IL}	COM'L	2.7			Volts
			MIL	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA, V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	COM'L			0.85	Volts
			MIL			0.80	
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V	COM'L			−0.100	mA
			MIL			−0.150	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				25	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)	COM'L	−20		−70	mA
			MIL	−15		−85	
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX.	COM'L		125	175	mA
			MIL		125	185	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX., $\overline{VE_1}$ = 2.4V, VE_2 = 0.4V	V_O = 4.5V			100	μA
			V_O = 2.4V			40	
			V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 3)			5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 3)			12		

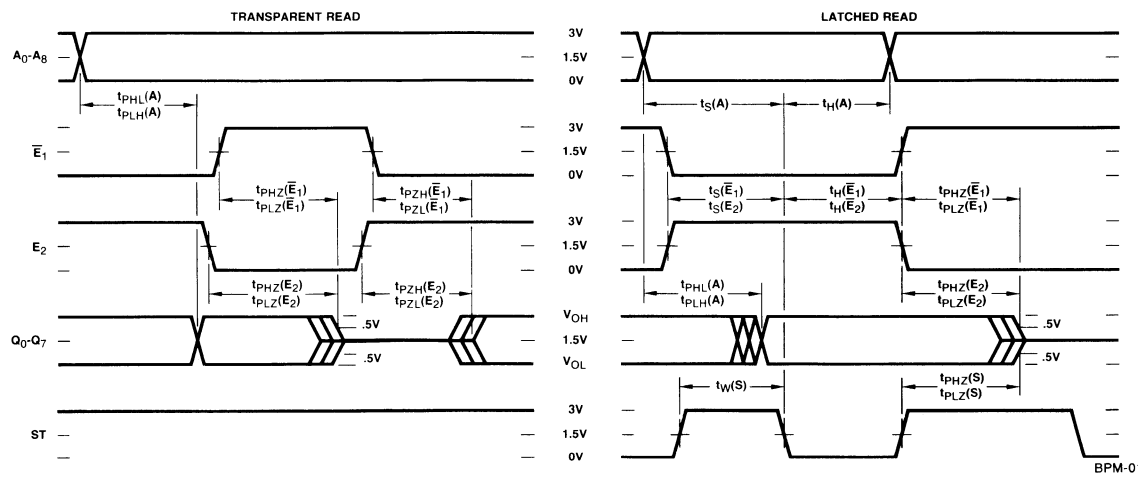
Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

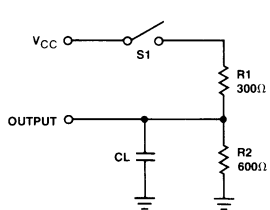
Parameter	Description	Test Conditions	Typ. (Note 1)	COM'L Min.	COM'L Max.	MIL Min.	MIL Max.	Units
$t_{PHL}(A)$ $t_{PLH}(A)$	Transparent Mode Address to Output Access Time	C_L = 30pF S_1 Closed (See AC Test Load Below)	35		60		90	ns
$t_W(S)$	Strobe Pulse Width (HIGH)		10	30		40		ns
$t_S(A)$	Address to Strobe (LOW) Set-up Time		35	60		90		ns
$t_H(A)$	Address to Strobe (LOW) Hold Time		−10	0		5		ns
$t_S(E_1)$ $t_S(E_2)$	Enable to Strobe (LOW) Set-up Time			40		50		ns
$t_H(E_1)$ $t_H(E_2)$	Enable to Strobe (LOW) Hold Time		0	10		10		ns
$t_{PZH}(\overline{E}_1,E_2)$ $t_{PZL}(\overline{E}_1,E_2)$	Transparent Mode Enable to Output Enabled (HIGH or LOW) Time	C_L = 30pF S_1 Closed for t_{PZL}, & Open for t_{PZH}	20		40		50	ns
$t_{PHZ}(S)$ $t_{PLZ}(S)$	Strobe Delatch (HIGH) to Output Disabled (OFF or HIGH impedance) Time	C_L = 5pF (Note 2) S_1 closed for t_{PLZ} & Open for t_{PHZ}			35		45	ns
$t_{PHZ}(\overline{E}_1,E_2)$ $t_{PLZ}(\overline{E}_1,E_2)$	Transparent Mode Enable to Output Disabled (OFF or high impedance) Time		20		40		50	ns

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. t_{PHZ} and t_{PLZ} are measured to the V_{OH} − 0.5V and V_{OL} + 0.5V output levels respectively. All other switching parameters are tested from and to the 1.5V threshold levels.
3. Tests are performed with input rise and fall times (10% to 90%) of 5ns or less.

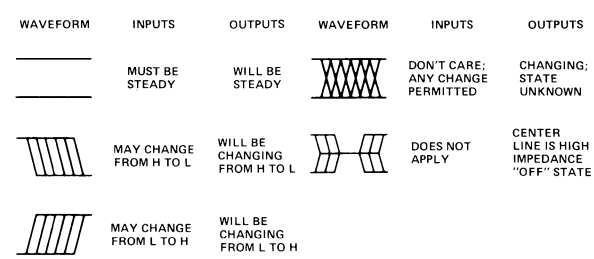
SWITCHING WAVEFORMS



AC TEST LOAD



KEY TO TIMING DIAGRAM



PROGRAMMING

The Am27S15 is manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to the memory output after the $\overline{E}_1$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{E}_1$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip is enabled and the output level is sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{E}_1$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be continuously applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

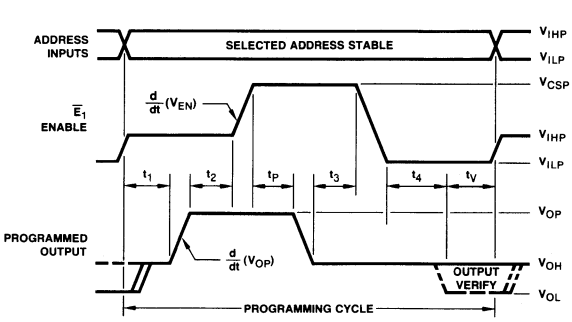
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{ENP}	$\overline{E}_1$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0.0	V_{CCP}+0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{EN})/dt$	Rate of $\overline{E}_1$ Voltage Change	100	1000	v/μsec
t_p	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

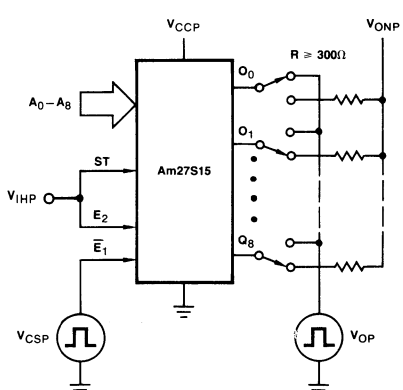
Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1 through t_4 must be greater than 100ns; maximum delays of 1μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-015

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-016

PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27S15 ADAPTERS AND CONFIGURATOR	715-1411-1	PA24-9 and 512 x 8 w/Latch(L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, however, much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 512 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of eight Ps or Ns, starting with output Q_7.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B"
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words) with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the eight Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the the tape is mailed.

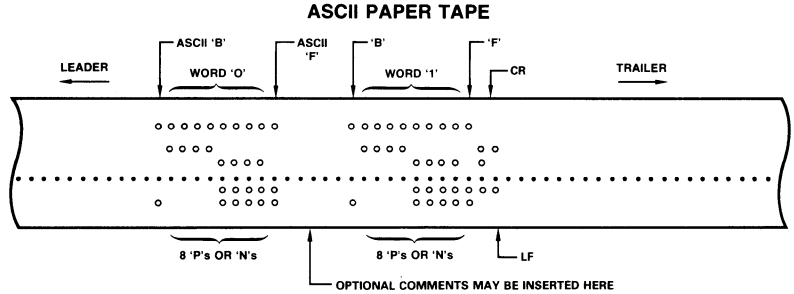
TYPICAL PAPER TAPE FORMAT

```
ØØØ   BPNPPNNNPF   WORD ZERO (R) (L)
      BPPPPPPNNF   COMMENT FIELD (R) (L)
ØØ2   BNNNPPPPNF   ANY (R) (L)
      BNNNNNNNNF   TEXT (R) (L)
ØØ4   BPNNNNNNPF   CAN (R) (L)
      BNPPNPPNNF   GO (R) (L)
ØØ6   BPNNPPPNNF   HERE (R) (L)
 :    ::::::::::    :
511   BNNNNPPPNF   END (R) (L)
(R) = CARRIAGE RETURN
(L) = LINE FEED
```

RESULTING DEVICE TRUTH TABLE ($\overline{E}_1$ AND $\overline{E}_2$ LOW)

A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
L	L	L	L	L	L	L	L	L	H	L	H	H	L	L	L	H
L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L	L
L	L	L	L	L	L	L	H	L	L	L	L	H	H	H	H	L
L	L	L	L	L	L	L	H	H	L	L	L	L	L	L	L	L
L	L	L	L	L	L	H	L	L	H	L	L	L	L	L	L	H
L	L	L	L	L	L	H	L	H	L	H	H	L	H	H	L	L
L	L	L	L	L	L	H	H	L	H	L	L	H	H	H	L	L
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
H	H	H	H	H	H	H	H	H	L	L	L	L	H	H	H	L

ASCII PAPER TAPE



BPM-017

GENERIC SERIES CHARACTERISTICS

The Am27S15 is a member of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

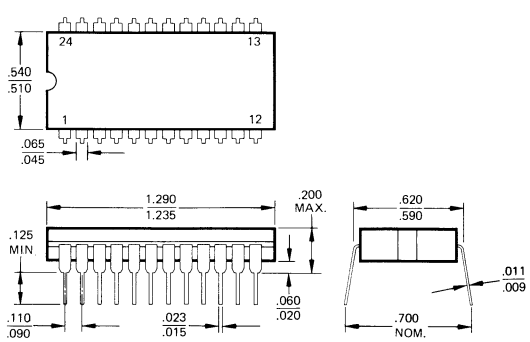
All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

PHYSICAL DIMENSIONS
Dual-In-Line

24-Pin Hermetic



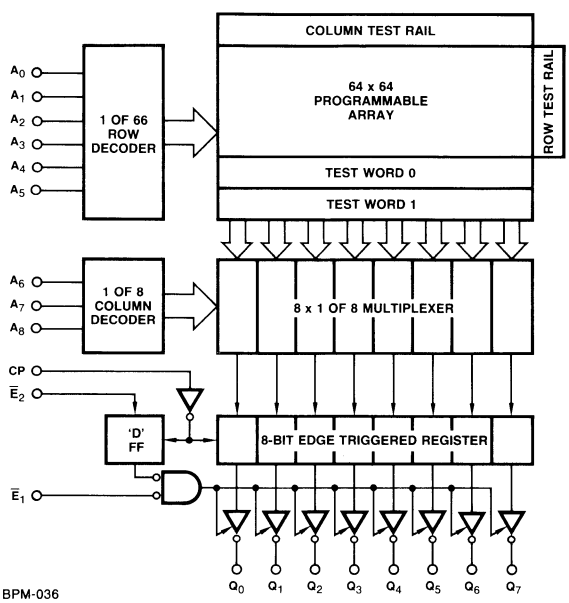
Am27S26 • Am27S27

4096-Bit Generic Series Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- On chip edge triggered registers – Ideal for pipelined microprogrammed systems
- Versatile synchronous and asynchronous enables for simplified word expansion
- Predetermined OFF outputs on power-up
- Fast 50ns address setup and 20ns clock to output times
- Excellent performance over the military range
- Performance pretested with N^2 patterns
- Space saving 22 pin package
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Common Generic PROM Series characteristics and programming procedures

BLOCK DIAGRAM



BPM-036

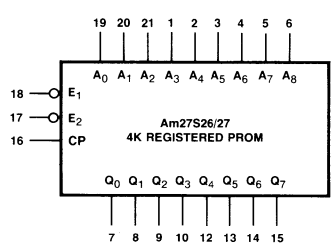
FUNCTIONAL DESCRIPTION

The Am27S26 and Am27S27 are electrically programmable Schottky TTL read only memories incorporating true D-type, master-slave data registers on chip. These devices feature the versatile 512 word by 8 bit organization and are available in both the open collector Am27S26 and three-state Am27S27 output versions. Designed to optimize system performance, these devices also substantially reduce the cost of pipelined microprogrammed system and other designs wherein accessed PROM data is temporarily stored in a register. The Am27S26 and Am27S27 also offer maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables.

When V_{CC} power is first applied, the synchronous enable ($\overline{E}_2$) flip-flop will be in the set condition causing the outputs, Q_0-Q_7, to be in the OFF or high impedance state, eliminating the need for a register clear input. Reading data is accomplished by first applying the binary word address to the address inputs, A_0-A_8, and a logic LOW to the synchronous output enable, $\overline{E}_2$. During the address setup time, stored data is accessed and loaded into the master flip-flops of the data register. Since the synchronous enable setup time is less than the address setup requirement, additional decoding delays may occur in the enable path without reducing memory performance. Upon the next LOW-to-HIGH transition of the clock, CP, data is transferred to the slave flip-flops which drive the output buffers. Providing the asynchronous enable, $\overline{E}_1$, is also LOW, stored data will appear on the outputs, Q_0-Q_7. If $\overline{E}_2$ is HIGH when the positive clock edge occurs, outputs go to the OFF or high impedance state. The outputs may be disabled at any time by switching $\overline{E}_1$ to a HIGH level. Following the positive clock edge, the address and synchronous enable inputs are free to change; changes do not affect the outputs until another positive clock edge occurs. This unique feature allows the PROM decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs. For less complex applications either enable may be effectively eliminated by tying it to ground.

The on-chip, edge triggered register simplifies system timing since the PROM clock may be derived directly from system clock without introducing dangerous race conditions. Other register timing requirements are similar to those of standard Schottky registers and are easily implemented.

LOGIC SYMBOL



V_{CC} = Pin 22
GND = Pin 11

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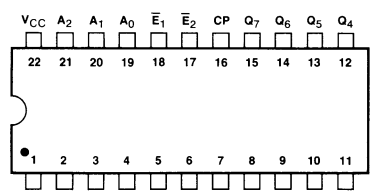
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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GENERIC SERIES CHARACTERISTICS

The Am27S26 and Am27S27 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	AM27S26XC, AM27S27XC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	AM27S26XM, AM27S27XM	T_C = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions			Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am27S27 only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}			2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}				0.38	0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V				−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V					25	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC} (Am27S27 only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)			−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.				130	185	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX. $V\overline{E}_1$ = 2.4V		V_O = 4.5V			100	μA
			Am27S27 Only	V_O = 2.4V			40	
				V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 3)				5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 3)				12		pF

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.

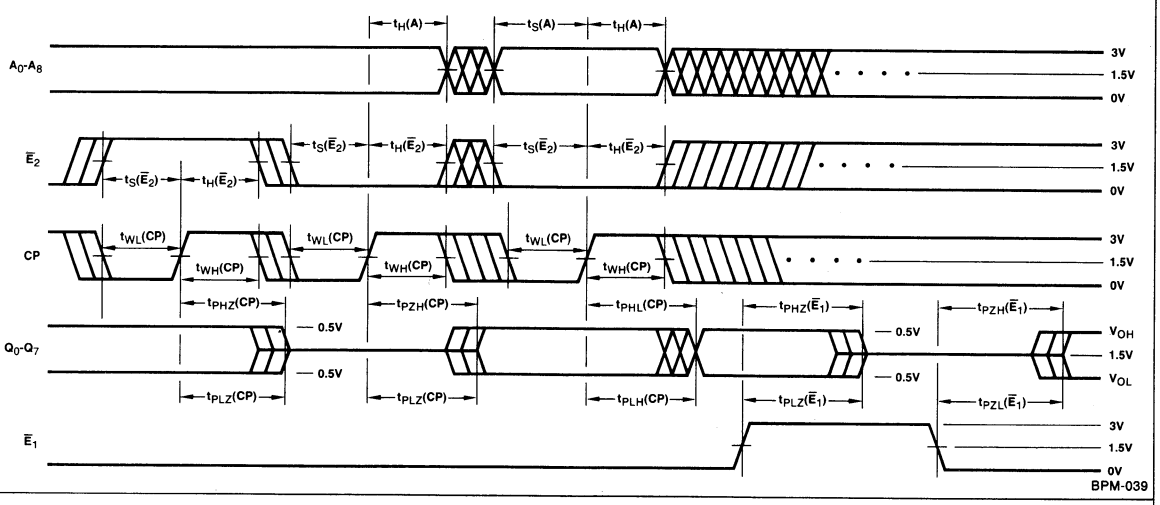
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PRELIMINARY DATA

Parameter	Description	Test Conditions	T_A = 25°C, V_{CC} = 5.0V Typ.	Min.	Max.	COM'L Min.	COM'L Max.	MIL Min.	MIL Max.	Units
$t_S(A)$	Address to CP (HIGH) Setup Time	C_L = 30pF, S_1 closed. (See AC Test Load below)	40	50						ns
$t_H(A)$	Address to CP (HIGH) Hold Time		−15	0						ns
$t_{PHL}(CP)$ $t_{PLH}(CP)$	Delay from CP (HIGH) to Output (HIGH or LOW)		15		20					ns
$t_{WH}(CP)$ $t_{WL}(CP)$	CP Width (HIGH or LOW)		10	20						ns
$t_S(\overline{E}_2)$	$\overline{E}_2$ to CP (HIGH) Setup Time		10	20						ns
$t_H(\overline{E}_2)$	$\overline{E}_2$ to CP (HIGH) Hold Time		−10	0						ns
$t_{PZL}(CP)$ $t_{PZH}(CP)$	Delay from CP (HIGH) to Active Output (HIGH or LOW) (Note 1)	C_L = 30pF, S_1 closed for t_{PZL} and open for t_{PZH}	15		25					ns
$t_{PZL}(\overline{E}_1)$ $t_{PZH}(\overline{E}_1)$	Delay from $\overline{E}_1$ (LOW) to Active Output (HIGH or LOW) (Note 1)		15		30					ns
$t_{PLZ}(CP)$ $t_{PHZ}(CP)$	Delay from CP (HIGH) to Inactive Output (OFF or high Impedance)(Note 1)	C_L = 5pF (Note 2), S_1 closed for t_{PLZ} and open for t_{PHZ}	15		25					ns
$t_{PLZ}(\overline{E}_1)$ $t_{PHZ}(\overline{E}_1)$	Delay from $\overline{E}_1$ (HIGH) to Inactive Output (OFF or high Impedance)(Note 1)		10		20					ns

Notes: 1. t_{PHZ} and t_{PZH} apply to the three-state Am29775 only.
2. t_{PHZ} and t_{PLZ} are measured to the V_{OH} − 0.5V and V_{OL} + 0.5V output levels respectively. All other switching parameters are tested from and to the 1.5V threshold levels.
4. Tests are performed with input 10% to 90% rise and fall times of 5ns or less.

SWITCHING WAVEFORMS



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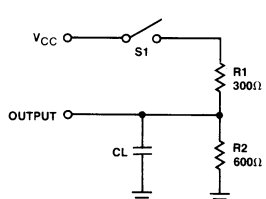
AC TEST LOAD



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KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

PROGRAMMING

The Am27S26 and Am27S27 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to the memory output after the $\overline{E}_1$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{E}_1$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip is enabled and the CP input is clocked. Each data verification attempt must be preceded by a positive going (LOW-to-HIGH) clock edge to load the array data into the on-chip register. The output level is then sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{E}_1$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be continuously applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

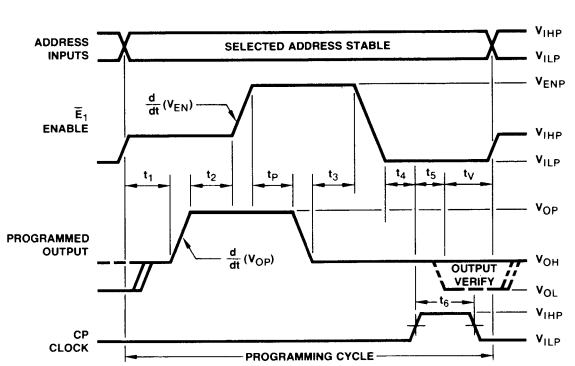
When all programming has been completed, the data content of the memory should be verified by clocking and reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	V
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	V
V_{ILP}	Input LOW Level During Programming	0.0	0.45	V
V_{ENP}	$\overline{E}_1$ Voltage During Programming	14.5	15.5	V
V_{OP}	Output Voltage During Programming	19.5	20.5	V
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP}+0.3	V
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{EN})/dt$	Rate of $\overline{E}_1$ Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1 through t_6 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



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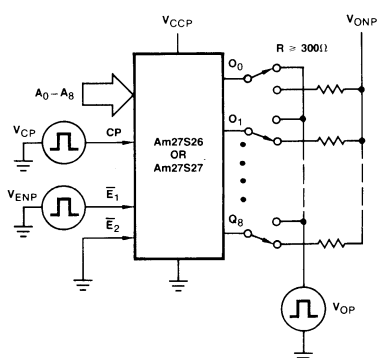
SIMPLIFIED PROGRAMMING DIAGRAM



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PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27S26 Am27S27 ADAPTERS AND CONFIGURATOR	715-1412-2	PA22-4 and 512 x 8 w/Register (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, however, much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 512 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of eight Ps or Ns, starting with output Q_7.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words) with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the eight Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

TYPICAL PAPER TAPE FORMAT

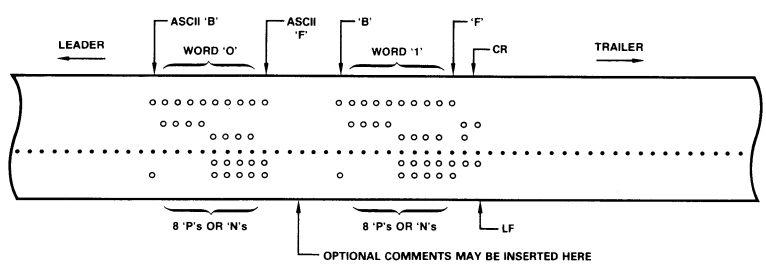
```
ØØØ   BPNPPNNNPF   WORD ZERO (R) (L)
      BPPPPPPNNF   COMMENT FIELD (R) (L)
ØØ2   BNNNPPPPNF   ANY (R) (L)
      BNNNNNNNNF   TEXT (R) (L)
ØØ4   BPNNNNNNPF   CAN (R) (L)
      BNPPNPPNNF   GO (R) (L)
ØØ6   BPNNPPPNNF   HERE (R) (L)
 :    :::::::::::   :
511   BNNNNPPPNF   END (R) (L)
```

(R) = CARRIAGE RETURN
(L) = LINE FEED

RESULTING DEVICE TRUTH TABLE ($\overline{E}_1$ AND $\overline{E}_2$ LOW)

A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
L	L	L	L	L	L	L	L	L	H	L	H	H	L	L	L	H
L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L	L
L	L	L	L	L	L	L	H	L	L	L	L	H	H	H	H	L
L	L	L	L	L	L	L	H	H	L	L	L	L	L	L	L	L
L	L	L	L	L	L	H	L	L	H	L	L	L	L	L	L	H
L	L	L	L	L	L	H	L	H	L	H	H	L	H	H	L	L
L	L	L	L	L	L	H	H	L	H	L	L	H	H	H	L	L
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
H	H	H	H	H	H	H	H	H	L	L	L	L	H	H	H	L

ASCII PAPER TAPE



BPM-043

APPLYING THE Am27S26 AND Am27S27 IN BIPOLAR MICROCOMPUTERS

With the advent of the Am2901 and Am2903 4-bit microprocessor slices, the Am2910 bipolar microprogram sequencer and the Am27S26/27 registered PROM, the design engineer can upgrade the performance of existing systems or implement new system taking advantage of the latest state-of-the-art technology in Low-Power Schottky integrated circuits. These devices, however, utilize a new concept in machine design not familar to many design engineers. This technique is called microprogramming.

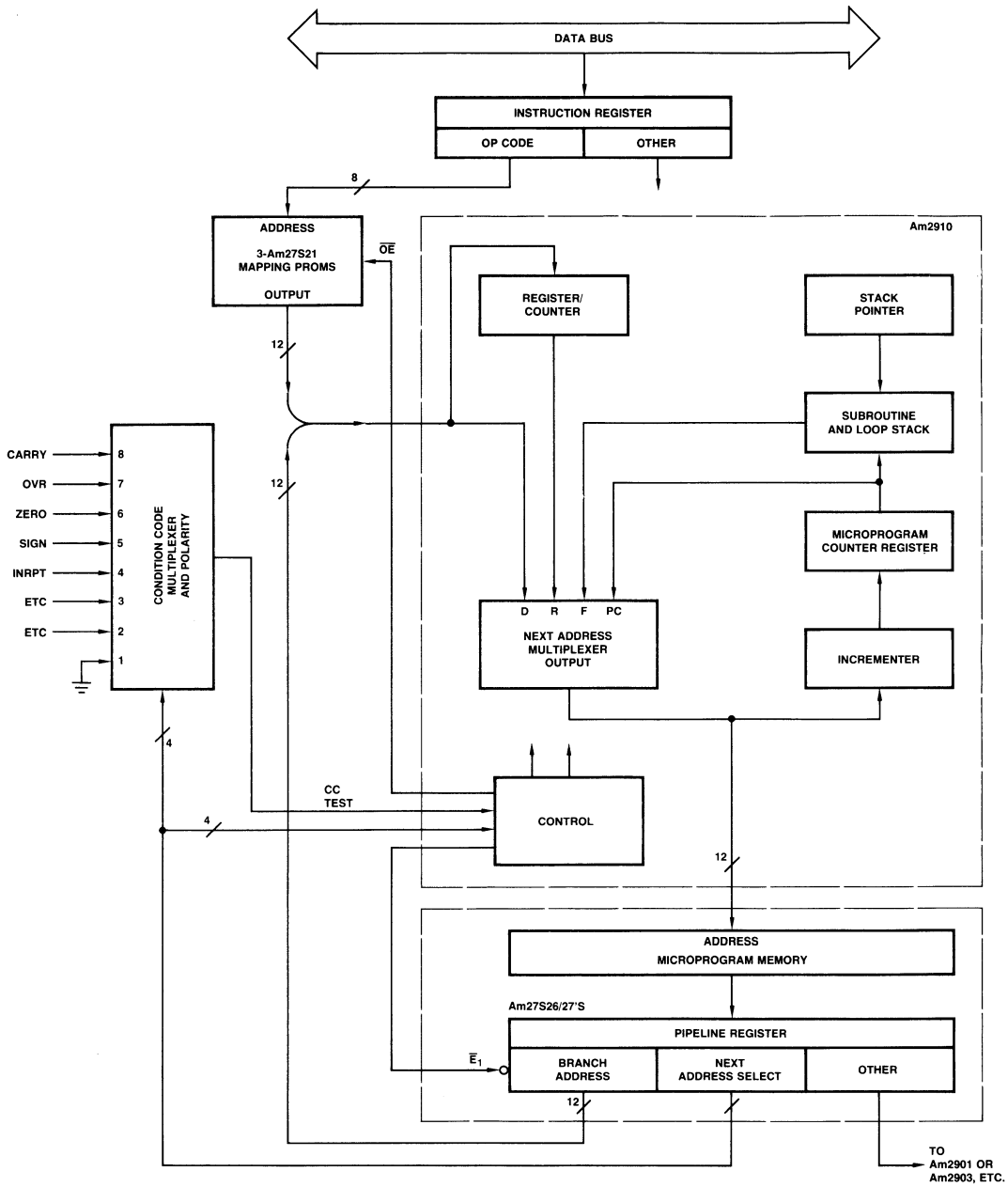


Fig. 1. A Typical Computer Control Unit using the Am27S26/27.

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APPLYING THE Am27S26 and Am27S27 IN BIPOLAR MICROCOMPUTERS (Cont.)

Basically, a microprogrammed machine is one in which a coherent sequence of microinstructions is used to execute various commands required by the machine. If the machine is a computer, each sequence of microinstructions can be made to execute a machine instruction. All of the little elemental tasks performed by the machine in executing the machine instruction are called microinstructions. The storage area for these microinstructions is usually called the microprogram memory.

A microinstruction usually has two primary parts. These are: (1) the definition and control of all elemental micro-operations to be carried out and (2) the definition and control of the address of the next microinstruction to be executed.

The definition of the various micro-operations to be carried out usually includes such things as ALU source operand selection, ALU function, ALU destination, carry control, shift control, interrupt control, data-in and data-out control, and so forth. The definition of the next microinstruction function usually includes identifying the source selection of the next microinstruction address and, in some cases, supplying the actual value of that microinstruction address.

Microprogrammed machines are usually distinquished from non-microprogrammed machines in the following manner. Older, non-microprogrammed machines implemented the control function by using combinations of gates and flip-flops connected in a somewhat random fashion in order to generate the required timing and control signals for the machine. Microprogrammed machines, on the other hand, are normally considered highly ordered, particularly with regard to the control function field, and use high speed PROM's for control definition. In its simplest definition, a microprogram control unit consists of the microprogram memory and the structure required to determine the address of the next microinstruction

The microprogram memory control unit block diagram of Figure 1 is easily implemented using the Am2910 and the Am27S26/27 registered PROM's. This architecture provides a structured state machine design capable of executing many highly sophisticated next address control instructions. The Am2910 contains a next address multiplexer that provides four different inputs from which the address of the next microinstruction can be selected. These are the direct input (D), the register input (R), the program counter (PC), and the file (F). The starting address decoder (mapping PROM) output and the Am27S26/27's pipeline register output are connected together at the D input to the Am2910 and are operated in the three-state mode.

The architecture of Figure 1 shows an instruction register capable of being loaded with a machine instruction word from the data bus. The op code portion of the instruction is decoded using a mapping PROM to arrive at a starting address for the microinstruction sequence required to execute the machine instruction. When the microprogram memory address is to be the first microinstruction of the machine instruction sequence, the Am2910 next address control selects the multiplexer D input and enables the three-state output from the mapping PROM. When the current microinstruction being executed is selecting the next microinstruction address as a JUMP function, the JUMP address will be available at the multiplexer D input. This is accomplished by having the Am2910 select the next address multiplexer D input and also enabling the three-state output of the pipeline register branch address field. The register enable input to the Am2910 can be grounded so that this register will load the value at the Am2910 D input. The value at D is clocked into the Am2910's register (R) at the end of the current microcycle, which makes the D value of this microcycle available as the R value of the next microcyle. Thus, by using the branch address field of two sequential microinstructions, a conditional JUMP-TO-ONE-OF-TWO-SUBROUTINES or a conditional JUMP-TO-ONE-OF-TWO-BRANCH-ADDRESSES can be executed by either selecting the D input or the R input of the next address multiplexer.

When sequencing through continuous microinstructions in the Am27S26/27 microprogram memory, the program counter in the Am2910 is used. Here, the control logic simply selects the PC input of the next address multiplexer. In addition, most of these instructions enable the three-state outputs of the Am27S26/27 pipeline register associated with the branch address field, which allows the register within the Am2910 to be loaded. The 5 x 12 stack in the Am2910 is used for looping and subroutining in microprogram operations. Up to five levels of subroutines or loops can be nested. Also, loops and subroutines can be intermixed as long as the five word depth of the stack is not exceeded.

The expansion scheme for increasing the depth of Am27S26/27's is shown in Figure 2. Note that no speed degradation results when devices are cascaded. This is because the decode of the Am74S139 is in parallel with the PROM access time.

In order to provide an overall view of a typical Am2900 Bipolar Microprocessor, the block diagram of Figure 3 is presented. Here, the computer control unit (CCU) using the Am2910 and Am27S26/27 registered PROM's is depicted. In addition, the typical connection scheme for the Am2903 Bipolar Microprocessor slices is shown. The four Am2903 devices in the block diagram form a typical 16-bit architecture. Also shown in Figure 3 is the general connection for the Am2914 Priority Interrupt Controller and the Am2920 as a Memory Address Register.

The block diagram also shows the Am2917 as the bus interface unit. Note that the Am2917 can interface directly with a data bus and the drive levels and receive levels are such that the instruction register can be built using standard Low-Power Schottky devices. This is possible because the receiver threshold on the Am2917 is designed identically to the thresholds on standard power Schottky and the Low-Power Schottky devices.

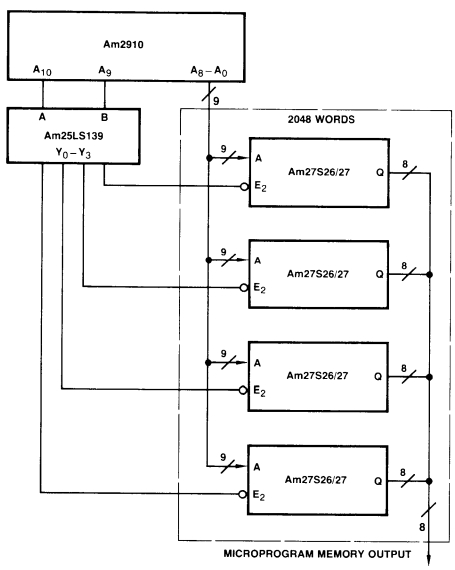


Fig. 2. Word Expansion Scheme for the Am27S26 and Am27S27.

BPM-045

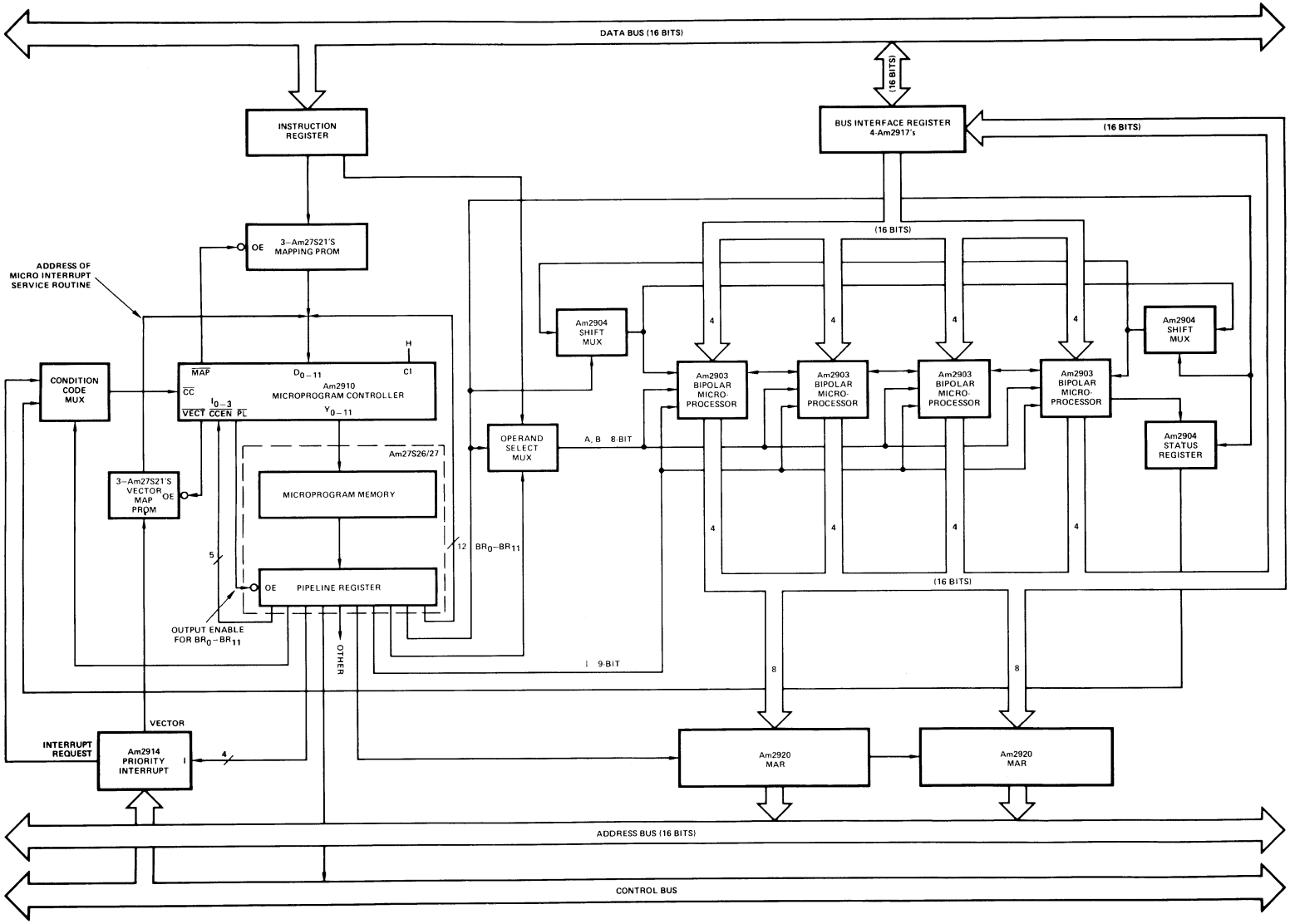
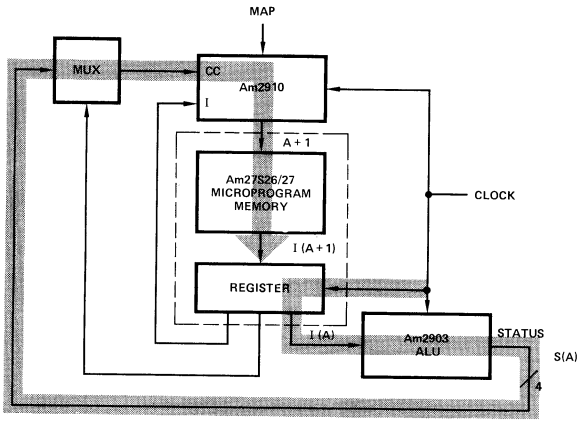


Fig. 3. Typical Bipolar Microcomputer using the Am27S26/27.

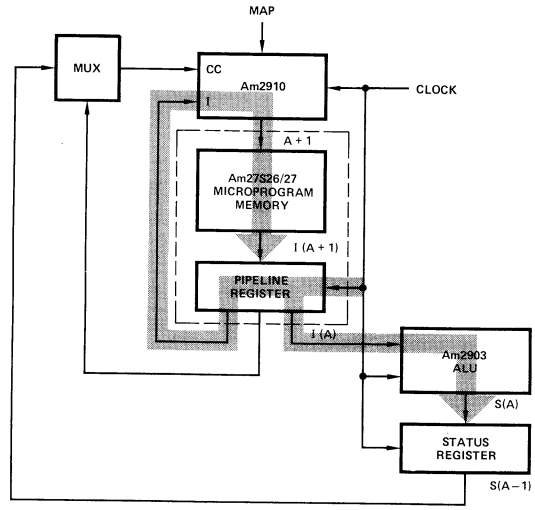
BPM-046

USING THE Am27S26/27 IN A PIPELINED ARCHITECTURE



A Register at the Microprogram Memory output contains the microinstruction being executed. The microprogram memory and Am2903 delay are in series. Conditional branches are executed on same cycle as the ALU operation generating the condition.

BPM-047



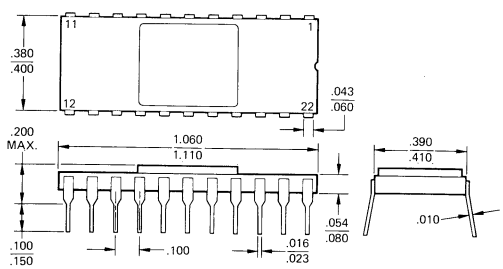
One level pipeline provides better speed than the architecture to the left. The Microprogram Memory and the Am2903 array are in parallel speed paths instead of in series. This is the recommended architecture for Am2900 designs. Note that the Am27S26/27 reduces the parts count of the microprogram memory/pipeline by a factor of two.

BPM-048

PHYSICAL DIMENSIONS

Dual In-Line

22-Pin Hermetic



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
	Open Collectors	
Hermetic DIP	0°C to +75°C	AM27S26DC
Hermetic DIP	−55°C to +125°C	AM27S26DM
	Three-State Outputs	
Hermetic DIP	0°C to +75°C	AM27S27DC
Hermetic DIP	−55°C to +125°C	AM27S27DM

Am8041

Universal Peripheral Interface 8-Bit Microcomputer

DISTINCTIVE CHARACTERISTICS

- Fully compatible with Am8080A, Am8085A, and Am8048 microprocessors
- Single level interrupts
- 8-bit CPU plus ROM, RAM, I/O, timer and clock in a single package
- Single +5V supply
- Alternative to custom LSI
- Pin compatible ROM versions
- 1K x 8 ROM, 64 x 8 RAM, 18 programmable I/O pins
- Asynchronous data register for interface to master processor
- Expandable I/O

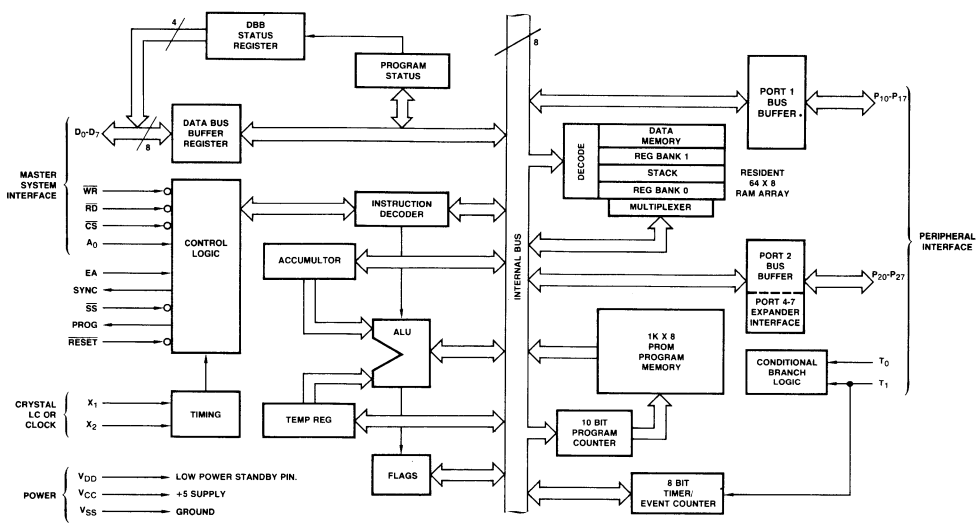
GENERAL DESCRIPTION

The AMD® Am8041 is a general purpose, programmable interface device designed for use with a variety of 8-bit microprocessor systems. It contains a low-cost microcomputer with program memory, data memory, 8-bit CPU, I/O ports, timer/counter, and clock in a simple 40-pin package. Interface registers are included to enable it to function as a peripheral controller in Am8080A, Am8085A, Am8048 and other 8-bit systems.

The Am8041 has 1K words of program memory and 64 words of data memory on-chip. The device has two 8-bit, TTL compatible I/O ports and two test inputs. Individual port lines can function as either inputs or outputs under software control. I/O can be expanded with Am8243 device which is directly compatible and has 16 I/O times. An 8-bit programmable timer/counter is included in the device for generating timing sequences or counting external inputs. Additional features include single 5V supply, low-power standby mode, single-level interrupt, and dual working register banks.

As a complete microcomputer, the Am8041 provides more flexibility for the designer than conventional LSI interface devices. It is designed to be an efficient controller. Applications include keyboard scanning, printer control, display multiplexing and similar functions which involve interfacing peripheral devices to microprocessor systems.

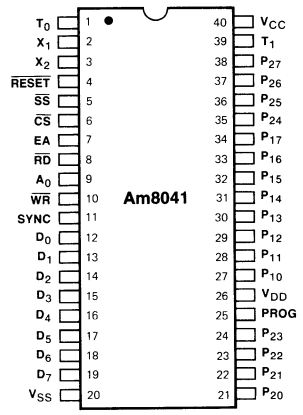
BLOCK DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	0°C to ≤ T_A ≤ +70°C	AM8041CC
Molded DIP		Am8041PC
Hermetic DIP	−55°C ≤ T_A ≤ +125°C	AM8041DM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS under which useful life may be impaired

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin with Respect to Ground	−0.5V to +7.0V
Power Dissipation	1.5 W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

DC AND OPERATING CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = V_{DD} = + 5.0V ±5%, V_{SS} = 0V

Parameter	Description	Test Conditions	Limits Min.	Typ.	Max.	Units
V_{IL}	Input Low Voltage (All Except X_1, X_2)		−0.5		0.8	Volts
V_{IH}	Input High Voltage (All Except X_1, X_2, $\overline{RESET}$)		2.0		V_{CC}	Volts
V_{IH2}	Input High Voltage (X_1, X_2, $\overline{RESET}$)		3.8		V_{CC}	Volts
V_{OL}	Output Low Voltage (D_0-D_7, Sync)	I_{OL} = 2.0mA			0.45	Volts
V_{OL2}	Output Low Voltage (All Other Outputs)	I_{OL} = 1.6mA			0.45	Volts
V_{OH}	Output High Voltage (D_0-D_7)	I_{OH} = −400μA	2.4			Volts
V_{OH1}	Output High Voltage (All Other Outputs)	I_{OH} = − 50μA	2.4			Volts
I_{IL}	Input Leakage Current (T_0, T_1, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, A_0, EA)	$V_{SS} \leq V_{IN} \leq V_{CC}$			±10	μA
I_{OL}	Output Leakage Current (D_0-D_7, High Z State)	V_{SS} + 0.45 ≤ $V_{IN} \leq V_{CC}$			±10	μA
I_{DD}	V_{DD} Supply Current			10	25	mA
I_{CC} + I_{DD}	Total Supply Current			65	135	mA
V_{OL3}	Output Low Voltage (Prog)	I_{OL} = 1.0mA			0.45	Volts
I_{LI1}	Low Input Source Current (P_{10}-P_{17}, P_{20}-P_{27})	V_{IL} = 0.8V			0.4	mA
I_{LI2}	Low Input Source Current ($\overline{RESET}$, SS)	V_{IL} = 0.8V			0.2	mA

AC CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = V_{DD} = + 5.0V ±5%, V_{SS} = 0V

DBB READ

Am8041

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{AR}	$\overline{CS}$, A_0 Set-up to $\overline{RD}\downarrow$		0			ns
t_{RA}	$\overline{CS}$, A_0 Hold After $\overline{RD}\uparrow$		0			ns
t_{RR}	$\overline{RD}$ Pulse Width	t_{CY} = 2.5μs	250			ns
t_{AD}	$\overline{CS}$, A_0 to Data Out Delay				150	ns
t_{RD}	$\overline{RD}\downarrow$ to Data Out Delay				150	ns
t_{DF}	$\overline{RD}\uparrow$ to Data Float Delay		10			ns
					100	
t_{RV}	Recovery Time Between Reads and/or Write		1			μs
t_{CY}	Cycle Time	6MHz Crystal	2.5			μs

DBB WRITE

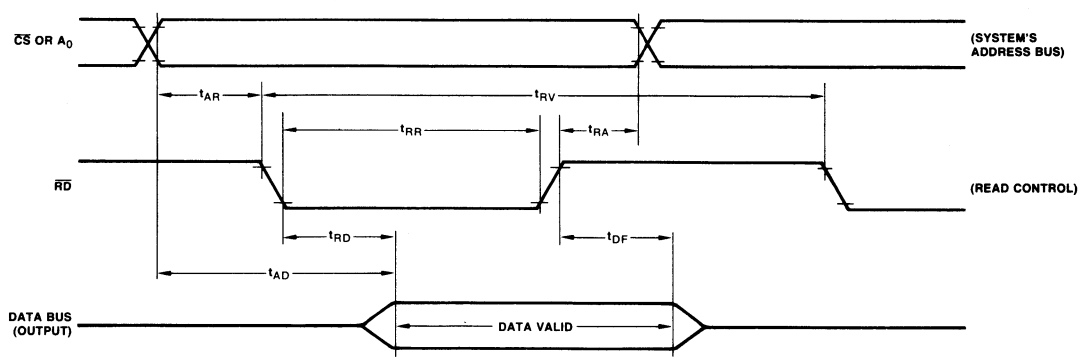
Am8041

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{AW}	$\overline{CS}$, A_0 Set-up to $\overline{WR}\downarrow$		0			ns
t_{WA}	CS, A_0 Hold After WR↑		0			ns
t_{WW}	WR Pulse Width	t_{CY} = 2.5μs	250			ns
t_{DW}	Data Set-up to WR↑		150			ns
t_{WD}	Data Hold After WR↑		0			ns

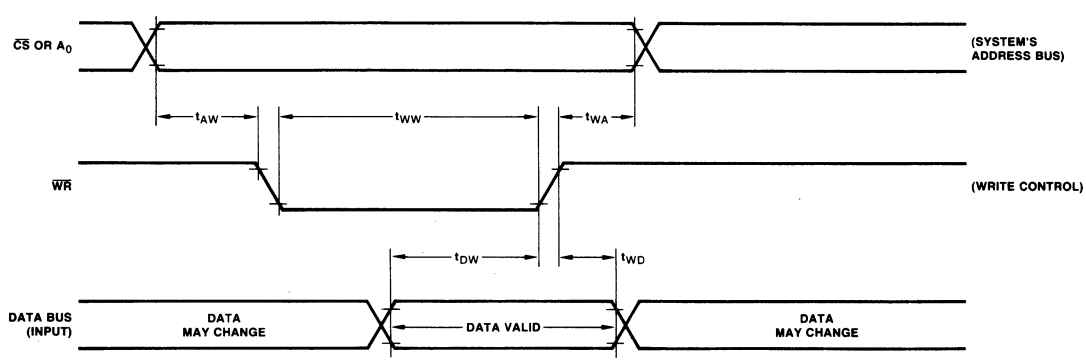
Note: D_0-D_7 outputs R_L = 2.2k to V_{SS}, 4.3k to V_{CC}, C_L = 100pF.

WAVEFORMS

READ OPERATION – DATA BUS BUFFER REGISTER



WRITE OPERATION – DATA BUS BUFFER REGISTER



Am8048/Am8035

Single Chip 8-Bit Microcomputers

DISTINCTIVE CHARACTERISTICS

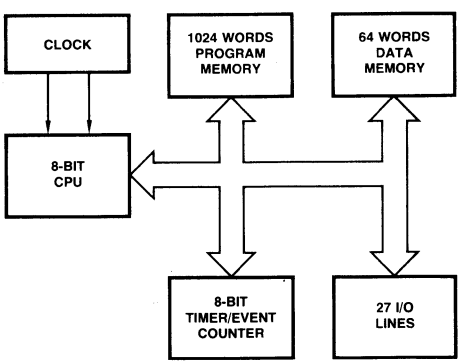
- 8-bit CPU, ROM, RAM, I/O in single package
- Single +5V supply
- 2.5μsec and 5.0μsec cycle versions
- All instructions 1 or 2 cycles
- Over 90 instructions: 70% single byte
- 1K x 8 ROM
- 64 x 8 RAM
- 27 I/O lines
- Interval timer/event counter
- Easily expandable memory and I/O
- Single level interrupt

GENERAL DESCRIPTION

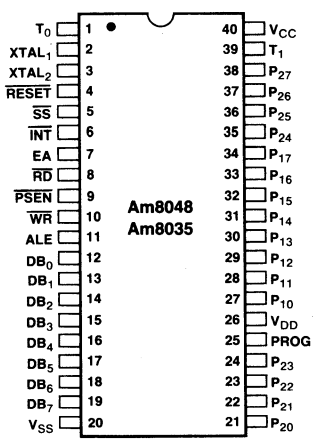
The Am8048 contains a 1k x 8 program memory, a 64 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on board oscillator and clock circuits. For systems that require extra capability, the Am8048 can be expanded using standard memories and Am9080A peripherals. The Am8035 is the equivalent of an Am8048 without program memory.

The microprocessor is designed to be an efficient controller. The Am8048 has extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over two bytes in length.

BLOCK DIAGRAM



CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Ambient Temperature Specification	Order Numbers	
Hermetic DIP	0°C ≤ T_A ≤ +70°C	AM8048CC	AM8035CC
Molded DIP		AM8048PC	AM8035PC
Hermetic DIP	−55°C ≤ T_A ≤ +125°C	AM8048DM	AM8035DM

MAXIMUM RATINGS (Above which useful life may be impaired)

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	0°C to +70°C
Voltage on Any Pin with Respect to Ground	−0.5V to +7.0V
Power Dissipation	1.5W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

DC AND OPERATING CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = V_{DD} = +5.0V ±10% (Note 1), V_{SS} = 0V

Parameters	Description	Test Conditions	Limits Min.	Typ.	Max.	Units
V_{IL}	Input Low Voltage		−.5		.8	Volts
V_{IH}	Input High Voltage (All Except $XTAL_1$, $XTAL_2$, $\overline{RESET}$)		2.0		V_{CC}	Volts
V_{IH1}	Input High Voltage ($\overline{RESET}$, $XTAL_1$, $XTAL_2$)		3.8		V_{CC}	Volts
V_{OL}	Output Low Voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	I_{OL} = 2.0mA			.45	Volts
V_{OL1}	Output Low Voltage (All Other Outputs Except PROG)	I_{OL} = 1.6mA			.45	Volts
V_{OLZ}	Output Low Voltage (PROG)	I_{OL} = 1.0mA			0.45	Volts
V_{OH}	Output High Voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	I_{OH} = −100μA	2.4			Volts
V_{OH1}	Output High Voltage (All Other Outputs)	I_{OH} = −50μA	2.4			Volts
I_{IL}	Input Leakage Current (T1, $\overline{INT}$)	$V_{SS} \leq V_{IN} \leq V_{CC}$			±10	μA
I_{OL}	Output Leakage Current (Bus, T_0) (High Impedance State)	$V_{CC} \geq V_{IN} \geq V_{SS}$ + .45			±10	μA
I_{DD}	Power Down Supply Current			10	20	mA
$I_{DD} + I_{CC}$	Total Supply Current			65	135	mA

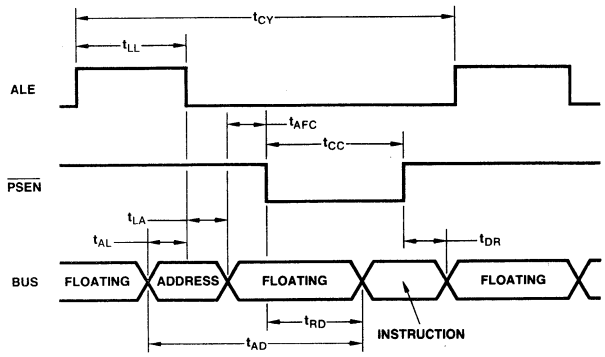
AC CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = V_{DD} = +5.0V ±10% (Note 1), V_{SS} = 0V

Parameters	Description	Test Conditions	Am8048 Am8035 Min.	Am8048 Am8035 Max.	Am8035-8 Min.	Am8035-8 Max.	Units
t_{LL}	ALE Pulse Width		400		600		ns
t_{AL}	Address Set-up to ALE		150		150		ns
t_{LA}	Address Hold from ALE		80		80		ns
t_{CC}	Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)		900		1500		ns
t_{DW}	Data Set-up Before $\overline{WR}$		500		640		ns
t_{WD}	Data Hold After $\overline{WR}$	C_L = 20pF	120		120		ns
t_{CY}	Cycle Time	6MHz XTAL (3.6MHz XTAL for −8)	2.5	15.0	4.17	15.0	μs
t_{DR}	Data Hold		0	200	0	200	ns
t_{RD}	$\overline{PSEN}$, $\overline{RD}$ to Data In			500		750	ns
t_{AW}	Address Set-up to $\overline{WR}$		230		260		ns
t_{AD}	Address Set-up to Data In			950		1450	ns
t_{AFC}	Address Float to $\overline{RD}$, $\overline{PSEN}$		0		0		ns

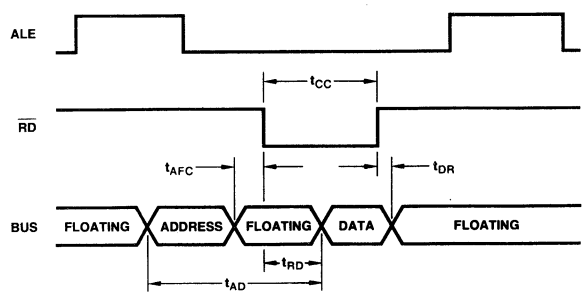
Notes: 1. Standard Am8035 ±5%, ±10% available.
2. Control Outputs: C_L = 80pF.
Bus Outputs: C_L = 150pF, t_{CY} = 2.5μs.

WAVEFORMS

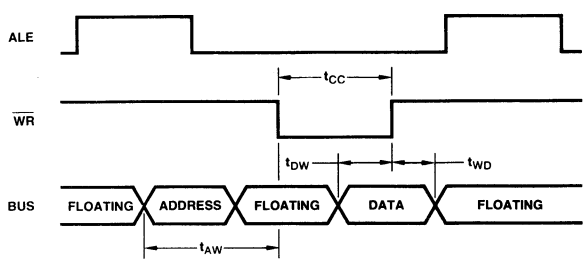
INSTRUCTION FETCH FROM EXTERNAL PROGRAM MEMORY



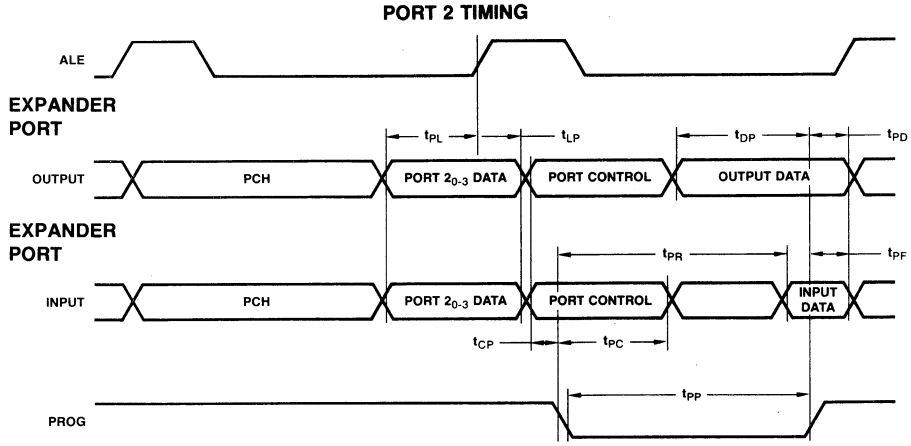
READ FROM EXTERNAL DATA MEMORY



WRITE TO EXTERNAL DATA MEMORY



PORT 2 TIMING



AC CHARACTERISTICS (Port 2 Timing)

T_A = 0°C to +70°C, V_{CC} = 5V ±10%

Parameters	Description	Test Conditions	Min.	Max.	Units
t_{CP}	Port Control Set-up before Falling Edge of $\overline{PROG}$		110		ns
t_{PC}	Port Control Hold after Falling Edge of $\overline{PROG}$		140		ns
t_{PR}	PROG to Time P2 Input Must be Valid			810	ns
t_{DP}	Output Data Set-up Time		220		ns
t_{PD}	Output Data Hold Time		65		ns
t_{PF}	Input Data Hold Time		0	150	ns
t_{PP}	$\overline{PROG}$ Pulse Width		1510		ns
t_{PL}	Port 2 I/O Data Set-up		400		ns
t_{LP}	Port 2 I/O Data Hold		150		ns

PIN DESCRIPTION

V_{SS}

Circuit GND potential.

V_{DD}

Power supply; +5V during operation. Low power standby pin for Am8048 ROM.

V_{CC}

Main power supply; +5V.

PROG

Output strobe for Am8243 I/O expander.

P_{10}-P_{17} Port 1

8-bit quasi-bidirectional port.

P_{20}-P_{27} Port 2

8-bit quasi-bidirectional port.

P_{20}-P_{23} contain the four high order program counter bits during an exteral program memory fetch and serve as a 4-bit I/O expander bus for Am8243.

D_0-D_7 BUS

True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched.

Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of PSEN. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$ and $\overline{WR}$.

T_0

Input pin testable using the conditional transfer instructions JT_0. and JNT_0. T_0 can be designated as a clock output using ENT0 CLK instruction. T_0 is also used during programming.

T_1

Input pin testable using the JT_1, and JNT_1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.

$\overline{INT}$

Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction (Active low).

$\overline{RD}$

Output strobe activated during a BUS read. Can be used to enable data onto the BUS from an external device.

Used as a Read Strobe to External Data Memory (Active low).

$\overline{RESET}$

Input which is used to initialize the processor. Also used during power down (Active low).

$\overline{WR}$

Output strobe during a BUS write (Active low) (Non-TTL V_{IH}).

Used as write strobe to External Data Memory.

ALE

Address Latch Enable. This signal occurs once during each cycle and is useful as a clock output.

The negative edge of ALE strobes address into external data and program memory.

$\overline{PSEN}$

Program Store Enable. This output occurs only during a fetch to external program memory (Active low).

$\overline{SS}$

Single step input can be used in conjunction with ALE to "single step" the processor through each instruction (Active low).

EA

External Access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification (Active high).

$XTAL_1$

One side of crystal input for internal oscillator. Also input for external source (Not TTL compatible).

$XTAL_2$

Other side of crystal input.

Am8253

Programmable Interval Timer

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

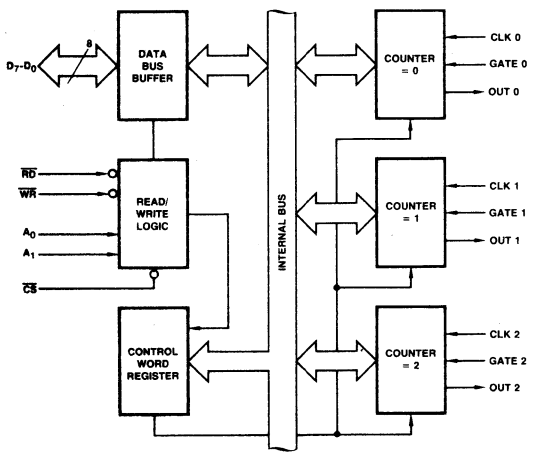
- Count binary or BCD
- Single +5V supply
- 24-pin dual-in-line package
- 3 independent 16-bit counters
- DC to 2MHz
- Programmable counter modes
- Bus oriented I/O

GENERAL DESCRIPTION

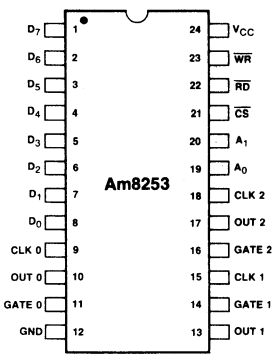
The Am8253 is a programmable counter/timer chip designed for use as an 8080A Family peripheral. It uses NMOS technology with a single +5V supply and is a direct replacement for Intel 8253.

It is organized as three independent 16-bit counters, each with a count rate of up to 2MHz. All modes of operation are software programmable. For improved performance, see Am9513 System Timing Controller.

BLOCK DIAGRAM



CONNECTION DIAGRAM
Top View



PIN NAMES

D7-D0	Data bus (8-bit)
CLK N	Counter clock inputs
GATE N	Counter gate inputs
OUT N	Counter outputs
$\overline{RD}$	Read counter
$\overline{WR}$	Write command or data
$\overline{CS}$	Chip select
A0-A1	Counter select
VCC	+5 Volts
GND	Ground

Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Ambient Temperature Specification	Order Numbers
Hermetic DIP*	0°C ≤ T_A ≤ +70°C	AM8253CC
Molded DIP		AM8253PC

*DC = Side-Brazed Ceramic CC = Cerdip

Am8279/Am8279-5

Programmable Keyboard/Display Interface

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

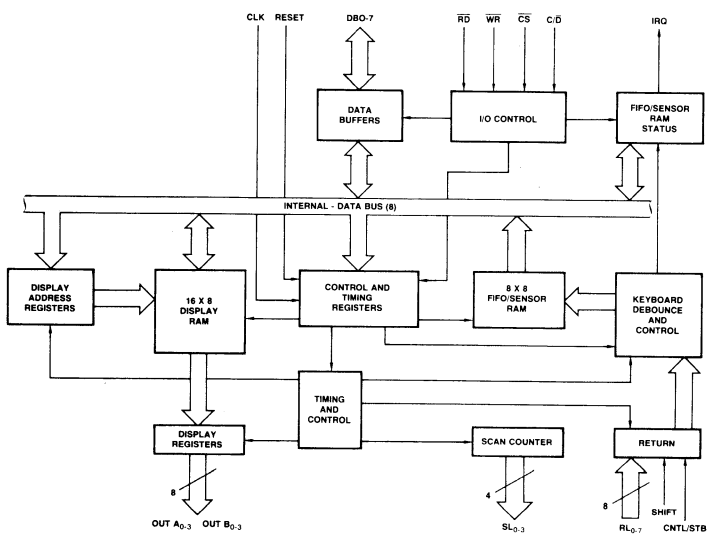
- Am8085A Compatible
- Simultaneous keyboard display operations
- Scanned keyboard mode
- Scanned sensor mode
- Strobed input entry mode
- 8 character keyboard FIFO
- 2 key lockout or N key rollover with contact debounce
- Dual 8 or 16 numerical display
- Single 16 character display
- Right or left entry 16-byte display RAM
- Mode programmable from CPU
- Programmable scan timing
- Interrupt output on key entry

GENERAL DESCRIPTION

The Am8279 is a general purpose programmable keyboard and display I/O interface device designed for use with Am8080A/8085A microprocessors. The keyboard portion can provide a scanned interface to a 64 contact key matrix which can be expanded to 128. The keyboard portion will also interface to an array of sensors or a strobed interface keyboard, such as the Hall effect and Ferrite variety. Key depressions can be 2 key lockout or N key rollover. Keyboard entries are debounced and stored in an 8 character FIFO. If more than 8 characters are entered, over run status is set. Key entries set the interrupt output line to the CPU.

The display portion provides a scanned display interface for LED, incandescent and other popular display technologies. Both numeric and alphanumeric segment displays may be used as well as simple indicators. The Am8279 has a 16 x 8 display RAM which can be organized into a dual 16 x 4. The RAM can be loaded or interrogated by the CPU. Both right entry, calculator and left entry typewriter display formats are possible. Both read and write of the display RAM can be done with auto-increment of the display RAM address.

BLOCK DIAGRAM



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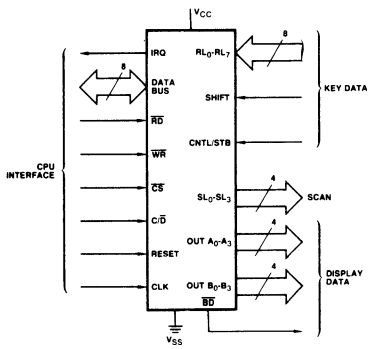
ORDERING INFORMATION

Package Type	Ambient Temperature Specification	Order Numbers	
Hermetic Dip	$0°C \leq T_A \leq +70°C$	AM8279CC	AM8279-5CC
Molded DIP		AM8279PC	AM8279-5PC

LOGIC SYMBOL

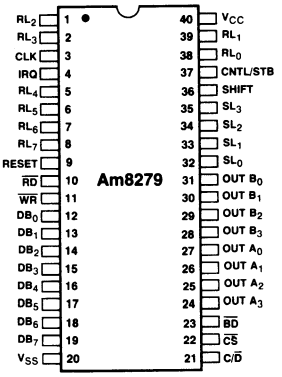


MOS-133

PIN NAMES

Name	I/O	Function
DB_0-DB_7	I/O	Data Bus (Bidirectional)
CLK	I	Clock Input
RESET	I	Reset Input
$\overline{CS}$	I	Chip Select
$\overline{RD}$	I	Read Input
$\overline{WR}$	I	Write Input
$C/\overline{D}$	I	Buffer Address
IRQ	O	Interrupt Request Output
SL_0-SL_3	O	Scan Lines
RL_0-RL_7	I	Return Lines
SHIFT	I	Shift Input
CNTL/STB	I	Control/Strobe Input
OUT A_0-A_3	O	Display (A) Outputs
OUT B_0-B_3	O	Display (B) Outputs
$\overline{BD}$	O	Blank Display Output

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MOS-134

MAXIMUM RATINGS above which useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{CC} with Respect to V_{SS}	−0.5V to +7.0V
All Signal Voltages with Respect to V_{SS}	−0.5V to +7.0V
Power Dissipation	1W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

DC CHARACTERISTICS T_A = 0°C to +70°C, V_{SS} = 0V (Note 1)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{IL1}	Input Low Voltage for Return lines Only		−0.5		1.4	V
V_{IL2}	Input Low Voltage for All Others		−0.5		0.8	V
V_{IH1}	Input High Voltage for Return lines Only		2.2			V
V_{IH2}	Input High Voltage for All Others		2.0			V
V_{OL}	Output Low Voltage	Note 2			.45	V
V_{OH}	Output High Voltage on Interrupt Line	Note 3	3.5			V
I_{IL1}	Input Current on Shift, Control and Returns	$V_{IN} = V_{CC}$ $V_{IN} = 0V$			+10 −100	μA μA
I_{IL2}	Input Leakage Current on All Others	$V_{IN} = V_{CC}$ to 0V			±10	μA
I_{OFL}	Output Float Leakage	$V_{OUT} = V_{CC}$ to 0V			±10	μA
I_{CC}	Power Supply Current				120	mA

Notes: 1. Am8279, V_{CC} = +5.0V ±5%; Am8279-5, V_{CC} = +5.0V ±10%.
2. Am8279, I_{OL} = 1.6mA; Am8279-5, I_{OL} = 2.2mA.
3. Am8279, I_{OH} = −100μA; Am8279-5, I_{OH} = −400μA.

CAPACITANCE

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = V_{CC}$		5	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = V_{CC}$		10	20	pF

AC CHARACTERISTICS (T_A = 0°C to 70°C, V_{SS} = 0V) (Note 1)

BUS PARAMETERS

Read Cycle:

Parameter	Description	Am8279 Min.	Am8279 Max.	Am8279-5 Min.	Am8279-5 Max.	Units
t_{AR}	Address Stable Before $\overline{READ}$	50		0		ns
t_{RA}	Address Hold Time for $\overline{READ}$	5		0		ns
t_{RR}	$\overline{READ}$ Pulse Width	420		250		ns
t_{RD}	Data Delay from $\overline{READ}$ (Note 2)		300		150	ns
t_{AD}	Address to Data Valid (Note 2)		450		250	ns
t_{DF}	$\overline{READ}$ to Data Floating	10	100	10	100	ns
t_{RCY}	Read Cycle Time	1		1		μs

Write Cycle:

Parameter	Description	Am8279 Min.	Am8279 Max.	Am8279-5 Min.	Am8279-5 Max.	Units
t_{AW}	Address Stable Before $\overline{WRITE}$	50		0		ns
t_{WA}	Address Hold Time for $\overline{WRITE}$	20		0		ns
t_{WW}	$\overline{WRITE}$ Pulse Width	400		250		ns
t_{DW}	Data Set-up Time for $\overline{WRITE}$	300		150		ns
t_{WD}	Data Hold Time for $\overline{WRITE}$	40		0		ns

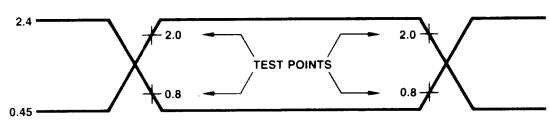
Notes: 1. Am8279, V_{CC} = +5.0V ±5%; Am8279-5, V_{CC} = +5.0V ±10%.
2. Am8279, C_L = 100pF; Am8279-5, C_L = 150pF.

Other Timings:

Parameter	Description	Am8279 Min.	Am8279 Max.	Am8279-5 Min.	Am8279-5 Max.	Units
$t_{\phi W}$	Clock Pulse Width	230		120		ns
t_{CY}	Clock Period	500		320		ns

Keyboard Scan Time	5.1msec	Digit-on Time	480μsec
Keyboard Debounce Time	10.3msec	Blanking Time	160μsec
Key Scan Time	80μsec	Internal Clock Cycle	10μsec
Display Scan Time	10.3msec		

INPUT WAVEFORMS FOR AC TESTS



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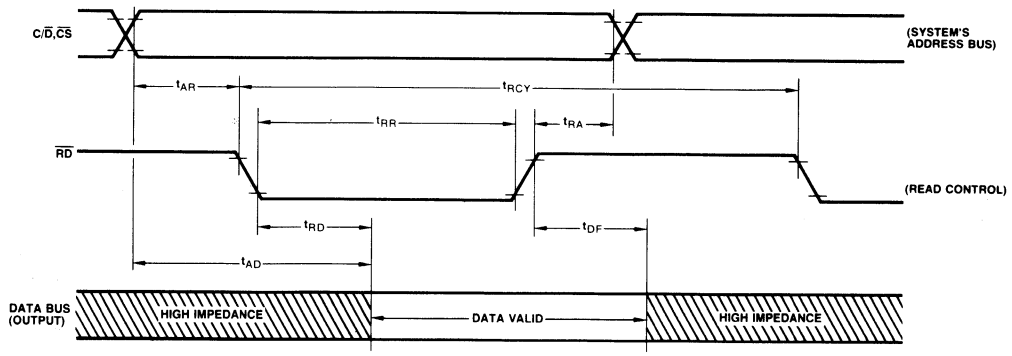
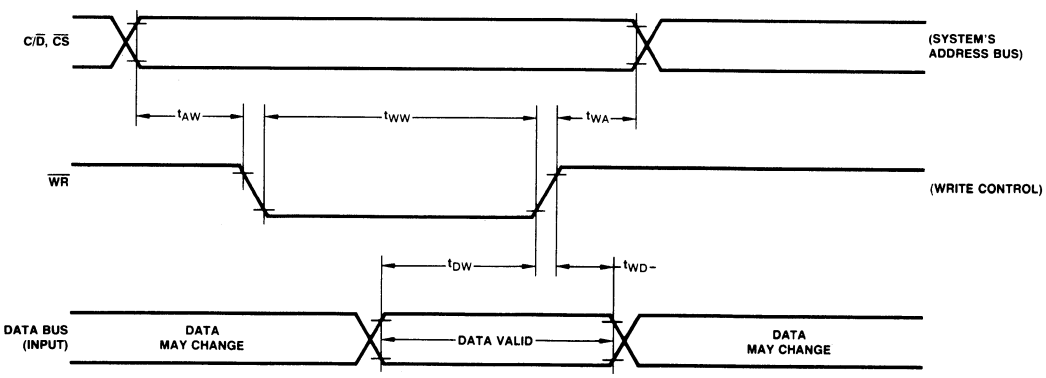
WAVEFORMS

READ OPERATION



MOS-136

WRITE OPERATION



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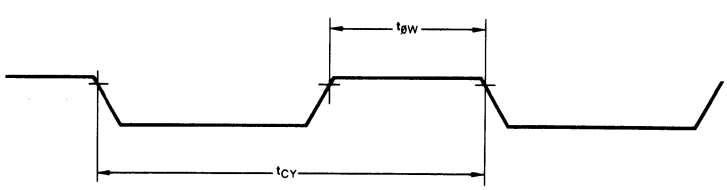
CLOCK INPUT



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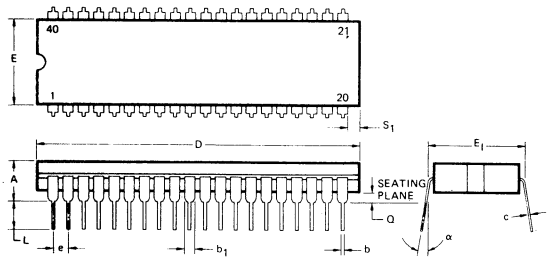
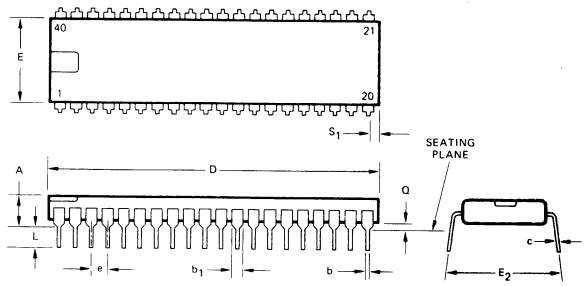
PHYSICAL DIMENSIONS

40-Pin Cerdip



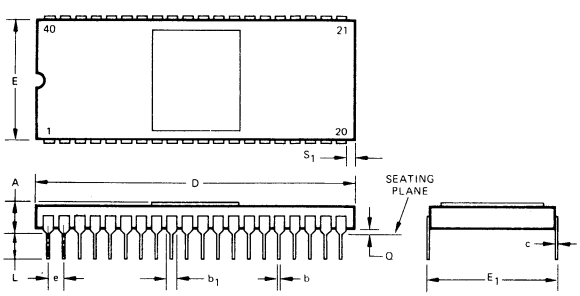
Reference Symbol	Inches	
	Min.	Max.
A	.150	.225
b	.016	.020
b_1	.045	.065
c	.009	.011
D	2.020	2.100
E	.510	.550
E_1	.600	.630
e	.090	.110
L	.120	.150
Q	.015	.060
S_1	.005	

40-Pin Molded DIP



Reference Symbol	Inches	
	Min.	Max.
A	.150	.200
b	.015	.020
b_1	.055	.065
c	.009	.011
D	2.050	2.080
E	.530	.550
E_2	.585	.700
e	.090	.110
L	.015	.060
Q	.015	.060
S_1	.040	.070

40-Pin Hermetic DIP



Reference Symbol	Inches	
	Min.	Max.
A	.100	.200
b	.015	.022
b_1	.030	.060
c	.008	.013
D	1.960	2.040
E	.550	.610
E_1	.590	.620
e	.090	.110
L	.120	.160
Q	.020	.060
S_1	.005	

Am9044 • Am9244

4096 x 1 Static R/W Random Access Memory

DISTINCTIVE CHARACTERISTICS

- **LOW OPERATING POWER (MAX)**
  Am9044/Am9244 385mW (70mA)
  Am90L44/Am92L44 275mW (50mA)
- **LOW STANDBY POWER (MAX)**
  Am92L44 110mW (20mA)
- Access times down to 200ns (max)
- Military temperature range available to 250ns (max)
- Am9044 is a direct plug-in replacement for 4044
- Am9244 pin and function compatible with Am9044 and 4044 plus $\overline{CS}$ power down feature
- Fully static – no clocking
- Identical access and cycle time
- High output drive – 4.0mA sink current @ 0.4V
- TTL identical interface logic levels
- 100% MIL-STD-883 reliability assurance testing

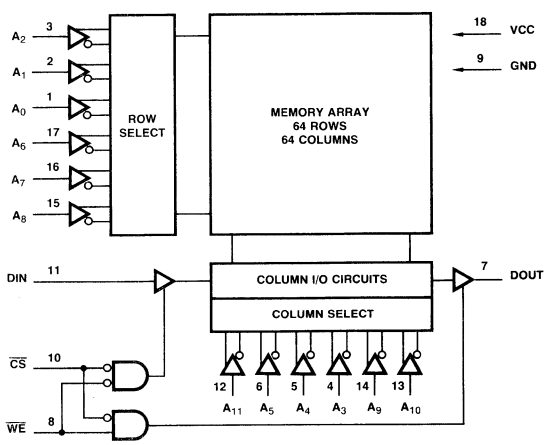
GENERAL DESCRIPTION

The Am9044 and Am9244 are high performance, static, N-Channel, read/write, random access memories organized as 4096 x 1. Operation is from a single 5V supply, and all input/output levels are identical to standard TTL specifications. Low power versions of both devices are available with power savings of about 30%. The Am9044 and Am9244 are the same except that the Am9244 offers an automatic $\overline{CS}$ power down feature.

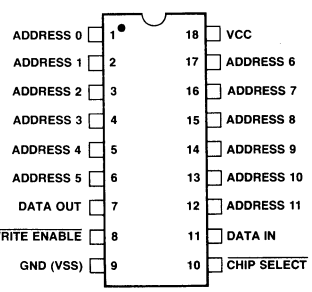
The Am9244 remains in a low power standby mode as long as $\overline{CS}$ remains high, thus reducing its power requirements. The Am9244 power decreases from 385mW to 165mW in the standby mode, and the Am92L44 from 275mW to 110mW. The $\overline{CS}$ input does not affect the power dissipation of the Am9044.

Data readout is not destructive and the same polarity as data input. $\overline{CS}$ provides for easy selection of an individual package when the outputs are OR-tied. The outputs of 4.0mA for Am9244 and Am9044 provide increased short circuit current for improved compacitive drive.

BLOCK DIAGRAM



CONNECTION DIAGRAM



Top View
Pin 1 is marked for orientation.

ORDERING INFORMATION

Ambient Temperature	Package Type	ICC Current Level	Access Times							
			Am9044				Am9244			
			450ns	300ns	250ns	200ns	450ns	300ns	250ns	200ns
0°C ≤ T_A ≤ +70°C	Plastic	70mA	AM9044BPC	AM9044CPC	AM9044DPC	AM9044EPC	AM9244BPC	AM9244CPC	AM9244DPC	AM9244EPC
		50mA	AM90L44BPC	AM90L44CPC	AM90L44DPC		AM92L44BPC	AM92L44CPC	AM92L44DPC	
	Hermetic	70mA	AM9044BDC	AM9044CDC	AM9044DDC	AM9044EDC	AM9244BDC	AM9244CDC	AM9244DDC	AM9244EDC
		50mA	AM90L44BDC	AM90L44CDC	AM90L44DDC		AM92L44BDC	AM92L44CDC	AM92L44DDC	
−55°C ≤ T_A ≤ +125°C	Hermetic	90mA	AM9044BDM	AM9044CDM	AM9044DDM		AM9244BDM	AM9244CDM	AM9244DDM	
		60mA	AM90L44BDM	AM90L44CDM			AM92L44BDM	AM92L44CDM		

MAXIMUM RATINGS beyond which useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
VCC with Respect to VSS	−0.5V to +7.0V
All Signal Voltages with Respect to VSS	−0.5V to +7.0V
Power Dissipation (Package Limitation)	1.0W
DC Output Current	10mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	VSS	VCC	Part Number	Ambient Temperature	VSS	VCC
Am9044DC/PC Am90L44DC/PC Am9244DC/PC Am92L44DC/PC	$0°C \leq T_A \leq +70°C$	0V	+5.0V ±10%	Am9044DM Am90L44DM Am9244DM Am92L44DM	$-55°C \leq T_A \leq +125°C$	0V	+5.0V ±10%

ELECTRICAL CHARACTERISTICS over operating range

Parameter	Description	Test Conditions			Am9244XX Am92L44XX Min.	Typ.	Max.	Am9044XX Am90L44XX Min.	Typ.	Max.	Units
IOH	Output High Current	VOH = 2.4V	VCC = 4.5V	70°C	−1.0			−1.0			mA
		VOH = 2.4V	VCC = 4.5V	125°C	−.4			−.4			
IOL	Output Low Current	VOL = 0.4V	$T_A = +70°C$		4.0			4.0			mA
			$T_A = +125°C$		3.2			3.2			
VIH	Input High Voltage				2.0		VCC	2.0		VCC	Volts
VIL	Input Low Voltage				−0.5		0.8	−0.5		0.8	Volts
IIX	Input Load Current	VSS ≤ VI ≤ VCC					10			10	μA
IOZ	Output Leakage Current	0.4V ≤ VO ≤ VCC Output Disabled	$T_A = +125°C$		−50		50	−50		50	μA
			$T_A = +70°C$		−10		10	−10		10	
CI	Input Capacitance (Note 1)	Test Frequency = 1.0MHz $T_A = 25°C$, All pins at 0V				3.0	5.0		3.0	5.0	pF
CI/O	I/O Capacitance (Note 1)					5.0	6.0		5.0	6.0	

ELECTRICAL CHARACTERISTICS over operating range

Parameter	Description	Test Conditions		Am92L44 Typ.	Am92L44 Max.	Am9244 Typ.	Am9244 Max.	Am90L44 Typ.	Am90L44 Max.	Am9044 Typ.	Am9044 Max.	Units
ICC	VCC Operating Supply Current	Max. VCC $\overline{CS} \leq$ VIL for Am9244/92L44	$T_A = 0°C$		50		70		50		70	mA
			$T_A = -55°C$		60		80		60		80	
IPD	Automatic $\overline{CS}$ Power Down Current	Max. V_{CC} ($\overline{CS} \geq V_{IH}$)	$T_A = 0°C$		20		30		–		–	mA
			$T_A = -55°C$		22		33		–		–	

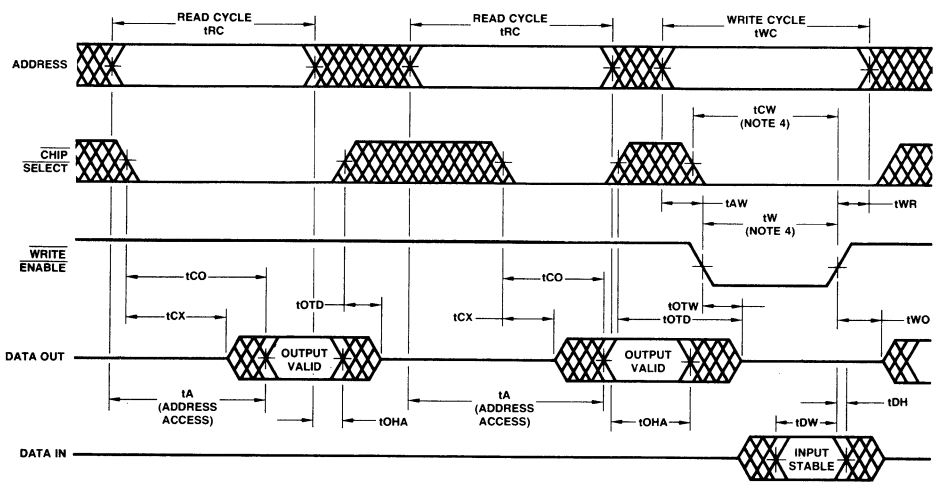
Notes:

1. Typical values are for T_A = 25°C, nominal supply voltage and nominal processing parameters.
2. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
3. Test conditions assume signal transition times of 10ns or less, timing reference levels of 1.5V and output loading of one standard TTL gate plus 100pF.
4. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
5. Chip Select access time (t_{CO}) is longer for the Am9244 than for the Am9044. The specified address access time will be valid only when Chip Select is low soon enough for t_{CO} to elapse.

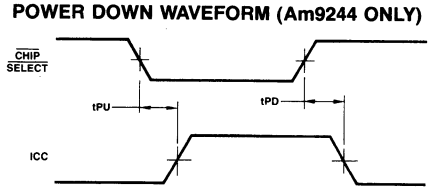
SWITCHING CHARACTERISTICS over operating range (Note 3)

Parameter	Description		Am9044B Am9244B Min.	Am9044B Am9244B Max.	Am9044C Am9244C Min.	Am9044C Am9244C Max.	Am9044D Am9244D Min.	Am9044D Am9244D Max.	Am9044E Am9244E Min.	Am9044E Am9244E Max.	Units
Read Cycle											
tRC	Address Valid to Address Do Not Care Time (Read Cycle Time)		450		300		250		200		ns
tA	Address Valid to Data Out Valid Delay (Address Access Time)			450		300		250		200	ns
tCO	Chip Select Low to Data Out Valid (Note 5)	Am9044		100		100		70		70	ns
		Am9244		450		300		250		200	ns
tCX	Chip Select Low to Data Out On		20		20		20		20		ns
tOTD	Chip Select High to Data Out Off			100		80		60		60	ns
tOHA	Address Unknown to Data Out Unknown Time		20		20		20		20		ns
Write Cycle											
tWC	Address Valid to Address Do Not Care Time (Write Cycle Time)		450		300		250		200		ns
tW	Write Enable Low to Write Enable High Time (Note 4)	Am9044	200		150		100		100		ns
		Am9244	250		200		150		150		ns
tWR	Write Enable High to Address Do Not Care Time		0		0		0		0		ns
tOTW	Write Enable Low to Data Out Off Delay			100		80		60		60	ns
tDW	Data In Valid to Write Enable High Time		200		150		100		100		ns
tDH	Write Enable Low to Data In Do Not Care Time		0		0		0		0		ns
tAW	Address Valid to Write Enable Low Time		0		0		0		0		ns
tPD	Chip Select High to Power Low Delay (Am9244 only)			200		150		100		100	ns
tPU	Chip Select Low to Power High Delay (Am9244 only)		0		0		0		0		ns
tCW	Chip Select Low to Write Enable High Time (Note 4)	Am9044	200		150		100		100		ns
		Am9244	250		200		150		150		ns
tWO	Write Enable High To Output Turn On			100		100		70		70	ns

SWITCHING WAVEFORMS

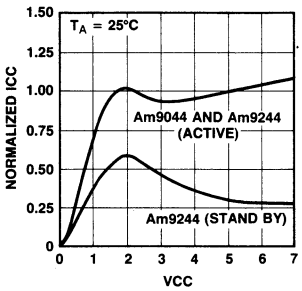


POWER DOWN WAVEFORM (Am9244 ONLY)

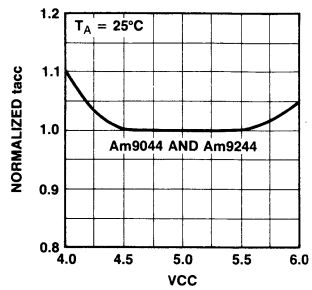


TYPICAL CHARACTERISTICS

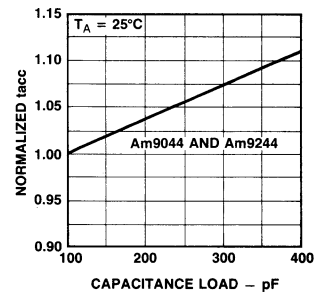
Typical ICC Versus VCC Characteristics



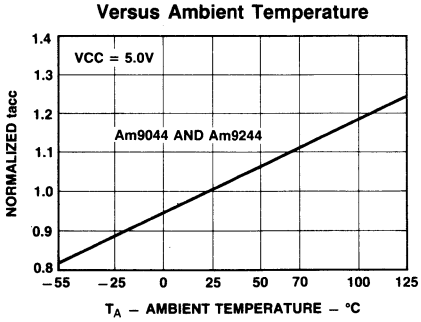
Typical tacc Versus VCC Characteristics



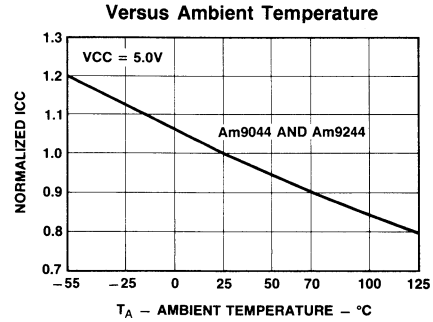
Typical C Load Versus Normalized tacc Characteristics



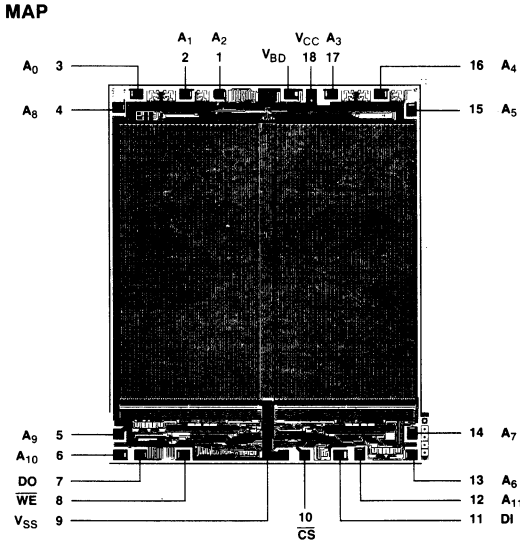
Normalized tacc Versus Ambient Temperature



Normalized ICC Versus Ambient Temperature



BIT MAP

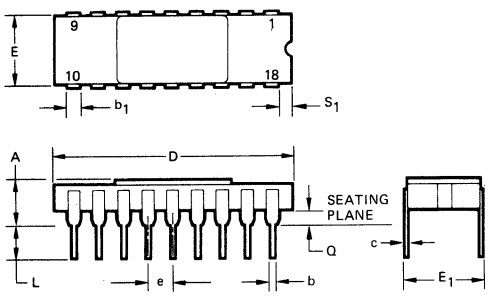


Address Designators	
External	Internal
A0	A2
A1	A1
A2	A0
A3	A8
A4	A9
A5	A10
A6	A3
A7	A4
A8	A5
A9	A7
A10	A6
A11	A11

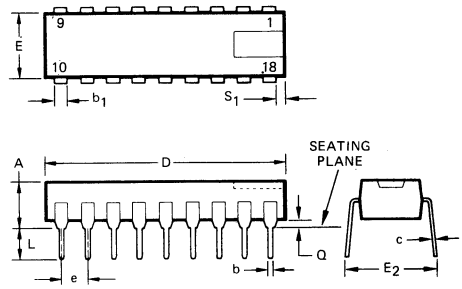
Figure 1. Bit Mapping Information.

PHYSICAL DIMENSIONS
Dual-In-Line

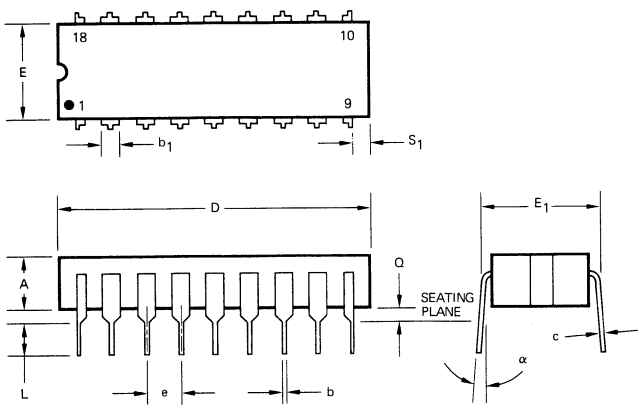
Side-Brazed



Plastic



Cerdip



Reference Symbol	Inches					
	Cerdip		Side-Brazed		Molded	
	Min.	Max.	Min.	Max.	Min.	Max.
A	.130	.200	.100	.200	.150	.200
b	.016	.020	.015	.022	.015	.020
b_1	.050	.070	.040	.065	.055	.065
c	.009	.011	.008	.013	.009	.011
D	.870	.920	.850	.930	.895	.925
E	.280	.310	.260	.310	.240	.260
E_1 or E_2	.290	.320	.290	.320	.310	.385
e	.090	.110	.090	.110	.090	.110
L	.125	.150	.125	.160	.125	.150
Q	.015	.060	.020	.060	.015	.060
S_1	.005		.005		.020	.040
α	3°	13°	0°	0°		

Am9114 • Am9124

1024 x 4 Static R/W Random Access Memory

DISTINCTIVE CHARACTERISTICS

- **LOW OPERATING POWER (MAX)**
  Am9124/Am9114 368mW (70mA)
  Am91L24/Am91L14 210mW (40mA)
- **LOW STANDBY POWER (MAX)**
  Am9124 158mW (30mA)
  Am91L24 105mW (20mA)
- Access times down to 200ns (max)
- Military temperature range available to 300ns (max)
- Am9114 is a direct plug-in replacement for 2114
- Am9124 pin and function compatible with Am9114 and 2114, plus $\overline{CS}$ power down feature
- Fully static – no clocking
- Identical access and cycle time
- High output drive –
  4.0mA sink current @ 0.4V – 9124
  3.2mA sink current @ 0.4V – 9114
- TTL identical input/output levels
- 100% MIL-STD-883 reliability assurance testing

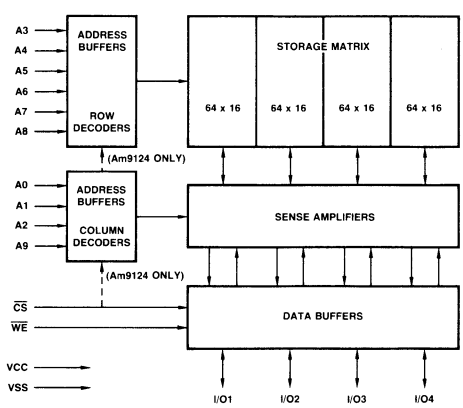
GENERAL DESCRIPTION

The Am9114 and Am9124 are high performance, static, N-Channel, read/write, random access memories organized as 1024 x 4. Operation is from a single 5V supply, and all input/output levels are identical to standard TTL specifications. Low power versions of both devices are available with power savings of over 40%. The Am9114 and Am9124 are the same except that the Am9124 offers an automatic $\overline{CS}$ power down feature.

The Am9124 remains in a low power standby mode as long as $\overline{CS}$ remains high, thus reducing its power requirements. The Am9124 power decreases from 368mW to 158mW in the standby mode, and the Am91L24 from 210mW to 105mW. The $\overline{CS}$ input does not affect the power dissipation of the Am9114. (See Figure 1, page 4).

Data readout is not destructive and the same polarity as data input. $\overline{CS}$ provides for easy selection of an individual package when the outputs are OR-tied. The outputs of 4.0mA for Am9124 and 3.2mA for Am9114 provides increased short circuit current for improved capacitive drive.

BLOCK DIAGRAM



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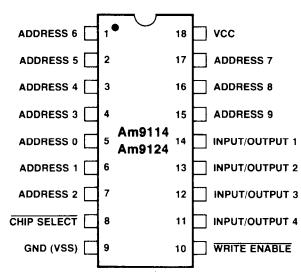
CONNECTION DIAGRAM



Top View
Pin 1 is marked for orientation.

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ORDERING INFORMATION

Ambient Temperature	Package Type	ICC Current Level	Access Times					
			Am9114			Am9124 (Power Down Option)		
			450ns	300ns	200ns	450ns	300ns	200ns
$0°C \leq T_A \leq 70°C$	Plastic	70mA	Am9114BPC	Am9114CPC	Am9114EPC	Am9124BPC	Am9124CPC	Am9124EPC
		40mA	Am91L14BPC	Am91L14CPC	Am91L14EPC	Am91L24BPC	Am91L24CPC	Am91L24EPC
	Hermetic	70mA	Am9114BDC	Am9114CDC	Am9114EDC	Am9124BDC	Am9124CDC	Am9124EDC
		40mA	Am91L14BDC	Am91L14CDC	Am91L14EDC	Am91L24BDC	Am91L24CDC	Am91L24EDC
$-55°C \leq T_A \leq +125°C$	Hermetic	80mA	Am9114BDM	Am9114CDM		Am9124BDM	Am9124CDM	
		50mA	Am91L14BDM	Am91L14CDM		Am91L24BDM	Am91L24CDM	

MAXIMUM RATINGS beyond which useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{CC} with Respect to V_{SS}	−0.5V to +7.0V
All Signal Voltages with Respect to V_{SS}	−0.5V to +7.0V
Power Dissipation (Package Limitation)	1.0W
DC Output Current	10mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	V_{SS}	V_{CC}	Part Number	Ambient Temperature	V_{SS}	V_{CC}
Am9114DC/PC Am91L14DC/PC Am9124DC/PC Am91L24DC/PC	$0°C \leq T_A \leq +70°C$	0V	+5.0V ± 5%	Am9114DM Am91L14DM Am9124DM Am91L24DM	$-55°C \leq T_A \leq +125°C$	0V	+5.0V ± 10%

ELECTRICAL CHARACTERISTICS over operating range

Parameter	Description	Test Conditions		Am9124XX Am91L24XX Min.	Typ.	Max.	Am9114XX Am91L14XX Min.	Typ.	Max.	Units
I_{OH}	Output High Current	V_{OH} = 2.4V	V_{CC} = 4.75V	−1.4			−1.0			mA
		V_{OH} = 2.2V	V_{CC} = 4.5V	−1.0			−1.0			
I_{OL}	Output Low Current	V_{OL} = 0.4V	T_A = +70°C	4.0			3.2			mA
			T_A = +125°C	3.2			2.4			
V_{IH}	Input High Voltage			2.0		V_{CC}	2.0		V_{CC}	Volts
V_{IL}	Input Low Voltage			−0.5		0.8	−0.5		0.8	Volts
I_{IX}	Input Load Current	$V_{SS} \leq V_I \leq V_{CC}$				10			10	μA
I_{OZ}	Output Leakage Current	0.4V ≤ $V_O \leq V_{CC}$ Output Disabled	T_A = +125°C	−50		50	−50		50	μA
			T_A = +70°C	−10		10	−10		10	
I_{OS}	Output Short Circuit Current	(Note 2)	0°C to +70°C			95			75	mA
			−55°C to +125°C			115			75	
CI	Input Capacitance (Note 1)	Test Frequency = 1.0MHz			3.0	5.0		3.0	5.0	pF
CI/O	I/O Capacitance (Note 1)	T_A = 25°C, All pins at 0V			5.0	6.0		5.0	6.0	

ELECTRICAL CHARACTERISTICS over operating range

Parameter	Description	Test Conditions		Am91L24 Typ.	Max.	Am9124 Typ.	Max.	Am91L14 Typ.	Max.	Am9114 Typ.	Max.	Units
I_{CC}	V_{CC} Operating Supply Current	Max. V_{CC}, $\overline{CS} \leq V_{IL}$ for Am9124/91L24	T_A = 25°C		35		65		35		65	mA
			T_A = 0°C		40		70		40		70	
			T_A = −55°C		50		80		50		80	
I_{PD}	Automatic $\overline{CS}$ Power Down Current	Max. V_{CC} ($\overline{CS} \geq V_{IH}$)	T_A = 25°C		18		27		–		–	mA
			T_A = 0°C		20		30		–		–	
			T_A = −55°C		22		33		–		–	

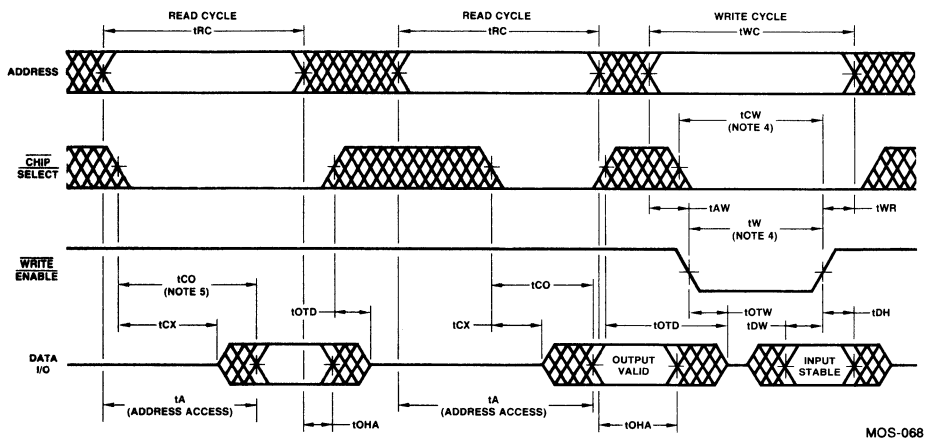
Notes:

1. Typical values are for T_A = 25°C, nominal supply voltage and nominal processing parameters.
2. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
3. Test conditions assume signal transition times of 10ns or less, timing reference levels of 1.5V and output loading of one standard TTL gate plus 100pF.
4. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
5. Chip Select access time (t_{CO}) is longer for the Am9124 than for the Am9114. The specified address access time will be valid only when Chip Select is low soon enough for t_{CO} to elapse.

SWITCHING CHARACTERISTICS over operating range (Note 3)

Parameter	Description		Am9114B Am9124B Min.	Am9114B Am9124B Max.	Am9114C Am9124C Min.	Am9114C Am9124C Max.	Am9114E Am9124E Min.	Am9114E Am9124E Max.	Unit
Read Cycle									
tRC	Address Valid to Address Do Not Care Time (Read Cycle Time)		450		300		200		ns
tA	Address Valid to Data Out Valid Delay (Address Access Time)			450		300		200	
tCO	Chip Select Low to Data Out Valid (Note 5)	Am9114		120		100		70	
		Am9124		420		280		185	
tCX	Chip Select Low to Data Out On		20		20		20		
tOTD	Chip Select High to Data Out Off			100		80		60	
tOHA	Address Unknown to Data Out Unknown Time		50		50		50		
Write Cycle									
tWC	Address Valid to Address Do Not Care Time (Write Cycle Time)		450		300		200		ns
tW	Write Enable Low to Write Enable High Time (Note 4)	Am9114	200		150		120		
		Am9124	250		200		150		
tWR	Write Enable High to Address Do Not Care Time		0		0		0		
tOTW	Write Enable Low to Data Out Off Delay			100		80		60	
tDW	Data In Valid to Write Enable High Time		200		150		120		
tDH	Write Enable Low to Data In Do Not Care Time		0		0		0		
tAW	Address Valid to Write Enable Low Time		0		0		0		
tPD	Chip Select High to Power Low Delay (Am9124 only)			200		150		100	
tPU	Chip Select Low to Power High Delay (Am9124 only)		0		0		0		
tCW	Chip Select Low to Write Enable High Time (Note 4)	Am9114	200		150		120		
		Am9124	250		200		150		

SWITCHING WAVEFORMS



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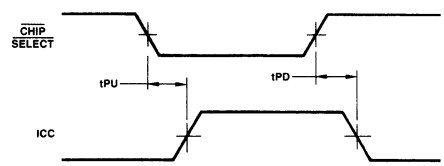
POWER DOWN WAVEFORM (Am9124 ONLY)



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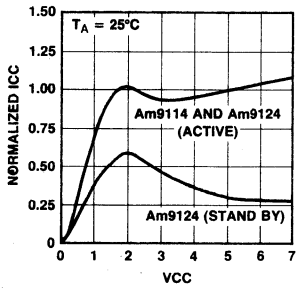
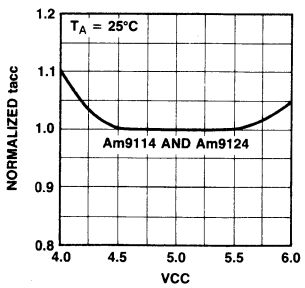
TYPICAL CHARACTERISTICS

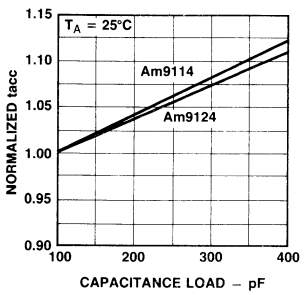
Typical ICC Versus VCC Characteristics



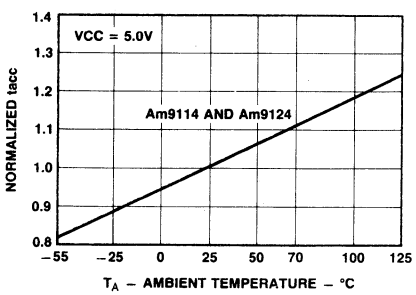
Typical tacc Versus VCC Characteristics



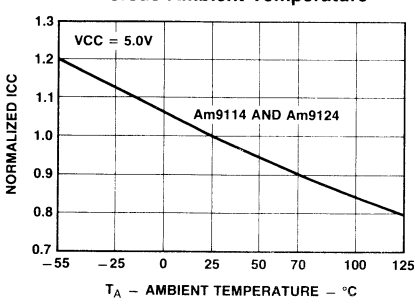
Typical C Load Versus Normalized tacc Characteristics



Normalized tacc Versus Ambient Temperature



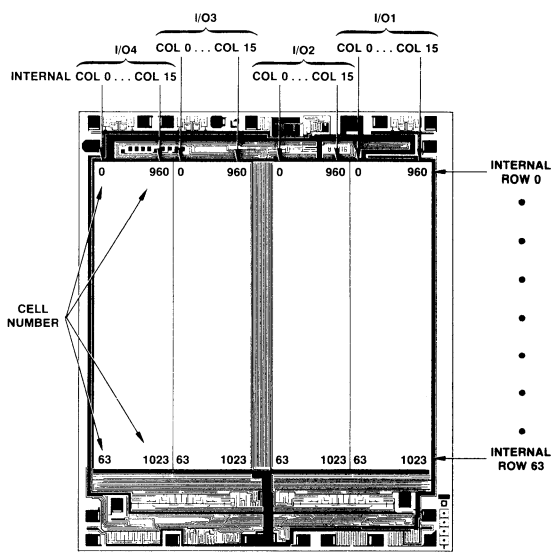
Normalized ICC Versus Ambient Temperature



Configuration	Part Number	Worst Case Current (mA at 0°C) 100% Duty Cycle	50% Duty Cycle
2K x 8	9114	280	280
	91L14	200	200
	9124	200	160
	91L24	140	110
4K x 12	9114	840	840
	91L14	600	600
	9124	480	420
	91L24	330	285
8K x 16	9114	2240	2240
	91L14	1600	1600
	9124	1120	1040
	91L24	760	700

Figure 1. Supply Current Advantages of Am9124.

BIT MAP

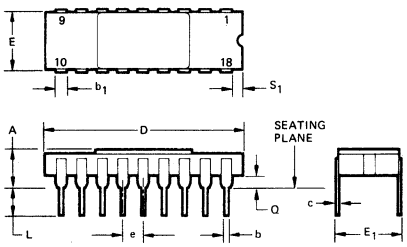


Address Designators	
External	Internal
A0	A9
A1	A8
A2	A7
A3	A0
A4	A1
A5	A2
A6	A3
A7	A4
A8	A5
A9	A6

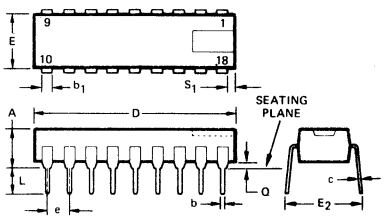
Figure 2. Bit Mapping Information.

PHYSICAL DIMENSIONS

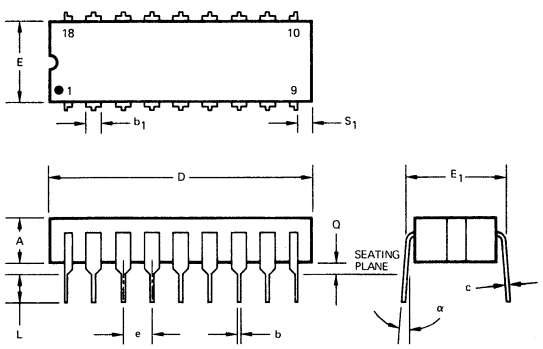
Side-Brazed (Military)



Plastic



Cerdip



Reference Symbol	INCHES					
	CERDIP		SIDE-BRAZED		MOLDED	
	Min.	Max.	Min.	Max.	Min.	Max.
A	.130	.200	.100	.200	.150	.200
b	.016	.020	.015	.022	.015	.020
b_1	.050	.070	.040	.065	.055	.065
c	.009	.011	.008	.013	.009	.011
D	.870	.920	.850	.930	.895	.925
E	.280	.310	.260	.310	.240	.260
E_1 or E_2	.290	.320	.290	.320	.310	.385
e	.090	.110	.090	.110	.090	.110
L	.125	.150	.125	.160	.125	.150
Q	.015	.060	.020	.060	.015	.060
S_1	.005		.005		.020	.040
α	3°	13°	0°	0°		

Am9016

16,384 x 1 Dynamic R/W Random Access Memory

DISTINCTIVE CHARACTERISTICS

- High density 16k x 1 organization
- Direct replacement for MK4116
- Worst-case refresh intervals at 70°C — 2ms for Am9016, 4ms for Am90R16
- Low maximum power dissipation — 462mW active, 20mW standby
- High speed operation — 200ns access, 375ns cycle
- ±10% tolerance on standard +12, +5, −5 voltages
- TTL compatible interface signals
- Three-state output
- RAS only, RMW and Page mode clocking options
- 128 cycle refreshing
- Unlatched data output
- Standard 16-pin, .3 inch wide dual in-line package
- Double poly N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

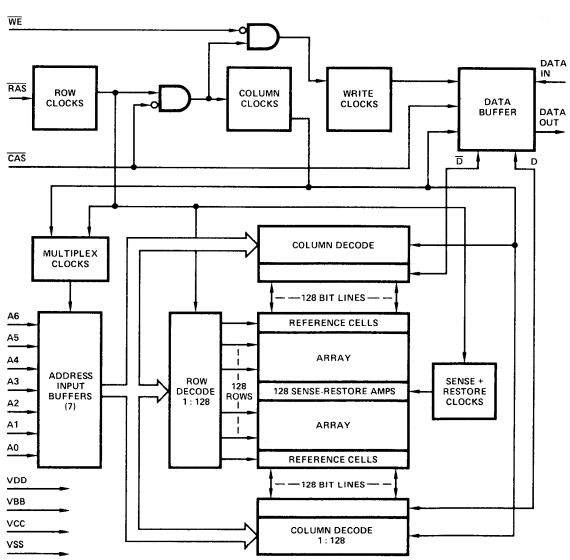
GENERAL DESCRIPTION

The Am9016 is a high speed, 16k-bit, dynamic, read/write random access memory. It is organized as 16,384 words by 1 bit per word and is packaged in a standard 16-pin DIP. The basic memory element is a single transistor cell that stores charge on a small capacitor. This mechanism requires periodic refreshing of the memory cells to maintain stored information..

All input signals, including the two clocks, are TTL compatible. The Row Address Strobe ($\overline{RAS}$) loads the row address and the Column Address Strobe ($\overline{CAS}$) loads the column address. The row and column address signals share 7 input lines. Active cycles are initiated when $\overline{RAS}$ goes low, and standby mode is entered when $\overline{RAS}$ goes high. In addition to normal read and write cycles, other types of operations are available to improve versatility, performance, and power dissipation.

The three-state output buffer turns on when the column access time has elapsed and turns off after $\overline{CAS}$ goes high. Input and output data are the same polarity.

BLOCK DIAGRAM



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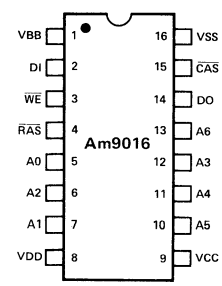
CONNECTION DIAGRAM



Top View
Pin 1 is marked for orientation.

A0 – A6	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
DI	DATA IN
DO	DATA OUT
$\overline{RAS}$	ROW ADDRESS STROBE
VDD	POWER (+12V)
VCC	POWER (+5V)
VSS	GROUND
VBB	POWER (−5V)
$\overline{WE}$	WRITE ENABLE

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ORDERING INFORMATION

Ambient Temperature	Package Type	Refresh Interval	Access Time			
			300ns	250ns	200ns	150ns
0°C ≤ T_A ≤ +70°C	Hermetic DIP	2msec	AM9016CDC	AM9016DDC	AM9016EDC	AM9016FDC
		4msec	AM90R16CDC	AM90R16DDC	AM90R16EDC	AM90R16FDC

MAXIMUM RATINGS above which useful life may be impaired

Storage Temperature	−55°C to +150°C
Ambient Temperature under Bias	0°C to +70°C
Input Signal Voltages with Respect to VBB	−0.5V to +20V
VDD and VCC Supply Voltages with Respect to VBB	−0.5V to +20V
Power Dissipation	1.0W
Short Circuit Output Current	50mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulation of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling, and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Ambient Temperature	VDD	VCC	VSS	VBB
$0°C \leq T_A \leq +70°C$	+12V ±10%	+5V ±10%	0	−5.0V ±10%

ELECTRICAL CHARACTERISTICS over operating range (Notes 1, 11)

Parameters	Description		Test Conditions		Am9016X Am90R16X Min.	Typ.	Max.	Units
VOH	Output HIGH Voltage		IOH = −5.0mA		2.4		VCC	Volts
VOL	Output LOW Voltage		IOL = 4.2mA		VSS		0.40	Volts
VIH	Input HIGH Voltage for Address, Data In				2.4		7.0	Volts
VIHC	Input HIGH Voltage for $\overline{CAS}$, $\overline{RAS}$, $\overline{WE}$				2.7		7.0	Volts
VIL	Input LOW Voltage				−1.0		0.80	Volts
IIX	Input Load Current		VSS ≤ VI ≤ VCC		−10		10	µA
IOZ	Output Leakage Current		VSS ≤ VO ≤ VCC, Output OFF		−10		10	µA
ICC	VCC Supply Current		Output OFF (Note 4)		−10		10	µA
IBB	VBB Supply Current, Average		Standby, $\overline{RAS} \geq$ VIHC				100	µA
			Operating, Minimum Cycle Time				200	
IDD	VDD Supply Current, Average	Operating	$\overline{RAS}$ Cycling, $\overline{CAS}$ Cycling, Minimum Cycle Times	Am9016C			35	mA
				Am9016D			35	
				Am9016E			35	
		Page Mode	$\overline{RAS} \leq$ VIL, $\overline{CAS}$ Cycling, Minimum Cycle Times	Am9016C			27	
				Am9016D			27	
				Am9016E			27	
		$\overline{RAS}$ – Only Refresh	$\overline{RAS}$ Cycling, $\overline{CAS} \geq$ VIHC, Minimum Cycle Times	Am9016C			27	
				Am9016D			27	
				Am9016E			27	
		Standby	$\overline{RAS} \geq$ VIHC				1.5	
CI	Input Capacitance	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Inputs at 0V, f = 1MHz, Nominal Supply Voltages				10	pF
		Address, Data In					5.0	
CO	Output Capacitance		Output OFF				7.0	

SWITCHING CHARACTERISTICS over operating range (Notes 2, 3, 5, 10)

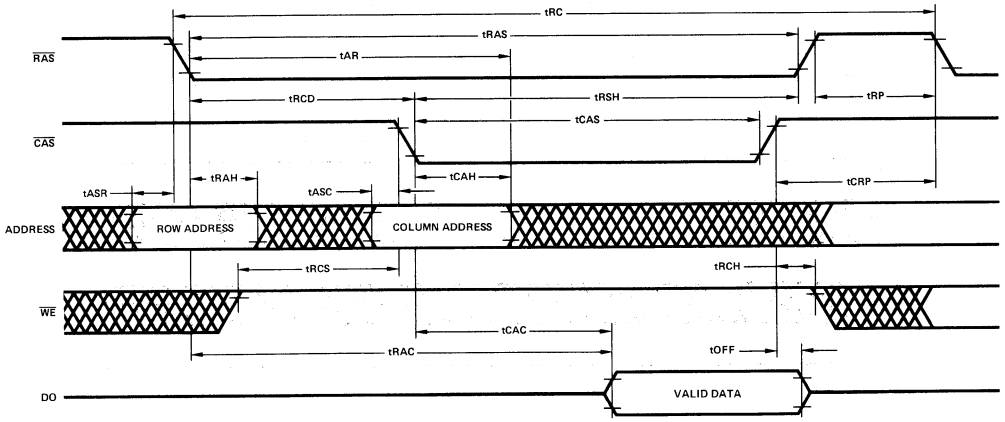
Parameters	Description	Renamed Parameter	Am9016C		Am9016D		Am9016E		Am9016F		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tAR	$\overline{RAS}$ LOW to Column Address Hold Time	TRELAX (C)	200		160		120		95		ns
tASC	Column Address Set-up Time	TAVCEL	−10		−10		−10		−10		ns
tASR	Row Address Set-up Time	TAVREL	0		0		0		0		ns
tCAC	Access Time from $\overline{CAS}$ (Note 6)	TCELQV		185		165		135	100		ns
tCAH	$\overline{CAS}$ LOW to Column Address Hold Time	TCELAX	85		75		55		45		ns
tCAS	$\overline{CAS}$ Pulse Width	TCELCEH	185	10,000	165	10,000	135	10,000	100	10,000	ns
tCP	Page Mode $\overline{CAS}$ Precharge Time	TCEHCEL	100		100		80		60		ns
tCRP	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	TCEHREL	−20		−20		−20		−20		ns
tCWD	$\overline{CAS}$ LOW to $\overline{WE}$ LOW Delay (Note 9)	TCELWL	145		125		95		70		ns
tCWL	$\overline{WE}$ LOW to $\overline{CAS}$ HIGH Set-up Time	TWLCEH	100		100		80		60		ns
tDH	$\overline{CAS}$ LOW or $\overline{WE}$ LOW to Data In Valid Hold Time (Note 7)	TCELDX or TWLDX	85		75		55		45		ns
tDHR	$\overline{RAS}$ LOW to Data In Valid Hold Time	TRELDX	200		160		120		95		ns
tDS	Data In Stable to $\overline{CAS}$ LOW or $\overline{WE}$ LOW Set-up Time (Note 7)	TDVCEL or TDVWL	0		0		0		0		ns
tOFF	$\overline{CAS}$ HIGH to Output OFF Delay	TCEHQZ	0	60	0	60	0	50	0	40	ns
tPC	Page Mode Cycle Time	TCELCEL (P)	295		275		225		170		ns
tRAC	Access Time from $\overline{RAS}$ (Note 6)	TRELQV		300		250		200		150	ns
tRAH	$\overline{RAS}$ LOW to Row Address Hold Time	TRELAX (R)	45		35		25		20		ns
tRAS	$\overline{RAS}$ Pulse Width	TRELREH	300	10,000	250	10,000	200	10,000	150	10,000	ns
tRC	Random Read or Write Cycle Time	TRELREL	460		410		375		375		ns
tRCD	$\overline{RAS}$ LOW to $\overline{CAS}$ LOW Delay (Note 6)	TRELCEL	35	115	35	85	25	65	20	50	ns
tRCH	Read Hold Time	TCEHWX	0		0		0		0		ns
tRCS	Read Set-up Time	TWHCEL	0		0		0		0		ns
tREF	Refresh Interval Am90R16			4		4		4		4	ms
	Refresh Interval Am9016			2		2		2		2	ms
tRP	$\overline{RAS}$ Precharge Time	TREHREL	150		150		120		100		ns
tRSH	$\overline{CAS}$ LOW to $\overline{RAS}$ HIGH Delay	TCELREH	185		165		135		100		ns
tRWC	Read/Write Cycle Time	TRELREL (R/W)	525		515		375		375		ns
tRWD	$\overline{RAS}$ LOW to $\overline{WE}$ LOW Delay (Note 9)	TRELWL	260		210		160		120		ns
tRWL	$\overline{WE}$ LOW to $\overline{RAS}$ HIGH Set-up Time	TWLREH	100		100		80		60		ns
tT	Transition Time		3	50	3	50	3	50	3	35	ns
tWCH	Write Hold Time	TCELWH	85		75		55		45		ns
tWCR	$\overline{RAS}$ LOW to Write Hold Time	TRELWH	200		160		120		95		ns
tWCS	$\overline{WE}$ LOW to $\overline{CAS}$ LOW Set-up Time (Note 9)	TWLCEL	−20		−20		−20		−20		ns
tWP	Write Pulse Width	TWLWH	85		75		55		45		ns

NOTES

1. Typical values are for T_A = 25°C, nominal supply voltages and nominal processing parameters.
2. Signal transition times are assumed to be 5ns. Transition times are measured between specified high and low logic levels.
3. Timing reference levels for both input and output signals are the specified worst-case logic levels.
4. VCC is used in the output buffer only. ICC will therefore depend only on leakage current and output loading. When the output is ON and at a logic high level, VCC is connected to the Data Out pin through an equivalent resistance of approximately 135Ω. In standby mode VCC may be reduced to zero without affecting stored data or refresh operations.
5. Output loading is two standard TTL loads plus 100pF capacitance.
6. Both $\overline{RAS}$ and $\overline{CAS}$ must be low to read data. Access timing will depend on the relative positions of their falling edges. When tRCD is less than the maximum value shown, access time depends on $\overline{RAS}$ and tRAC governs. When tRCD is more than the maximum value shown access time depends on $\overline{CAS}$ and tCAC governs. The maximum value listed for tRCD is shown for reference purposes only and does not restrict operation of the part.
7. Timing reference points for data input setup and hold times will depend on what type of write cycle is being performed and will be the later falling edge of $\overline{CAS}$ or $\overline{WE}$.
8. At least two initialization cycles that exercise both $\overline{RAS}$ and $\overline{CAS}$ should be performed after power-up and before valid operations are begun.
9. The tWCS, tRWD and tCWD parameters are shown for reference purposes only and do not restrict the operating flexibility of the part. When the falling edge of $\overline{WE}$ follows the falling edge of $\overline{CAS}$ by at most tWCS, the data output buffer will remain off for the whole cycle and an "early write" cycle is defined. When the falling edge of $\overline{WE}$ follows the falling edges of $\overline{RAS}$ and $\overline{CAS}$ by at least tRWD and tCWD respectively, the Data Out from the addressed cell will be valid at the access time and a "read/write" cycle is defined. The falling edge of $\overline{WE}$ may also occur at intermediate positions, but the condition and validity of the Data Out signal will not be known.
10. Switching characteristics are listed in alphabetical order.
11. All voltages referenced to VSS.

SWITCHING WAVEFORMS

READ CYCLE



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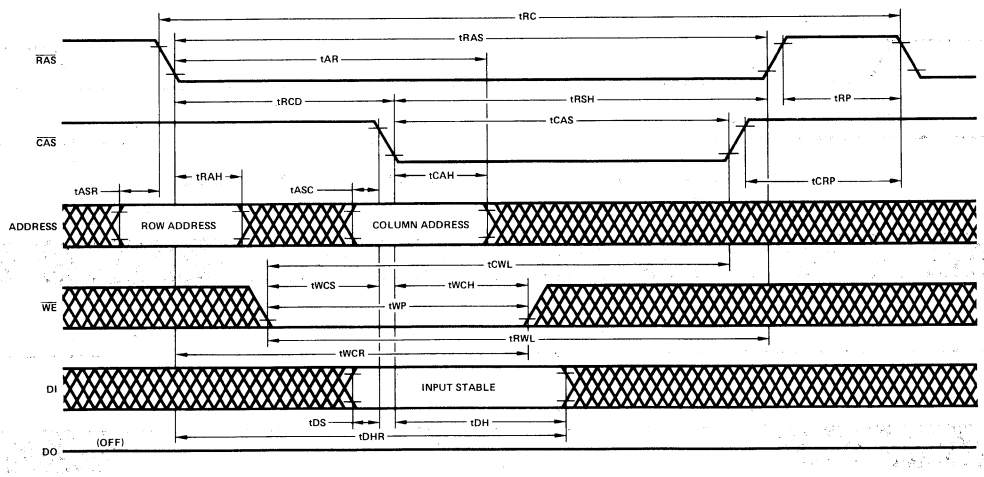
WRITE CYCLE (EARLY WRITE)



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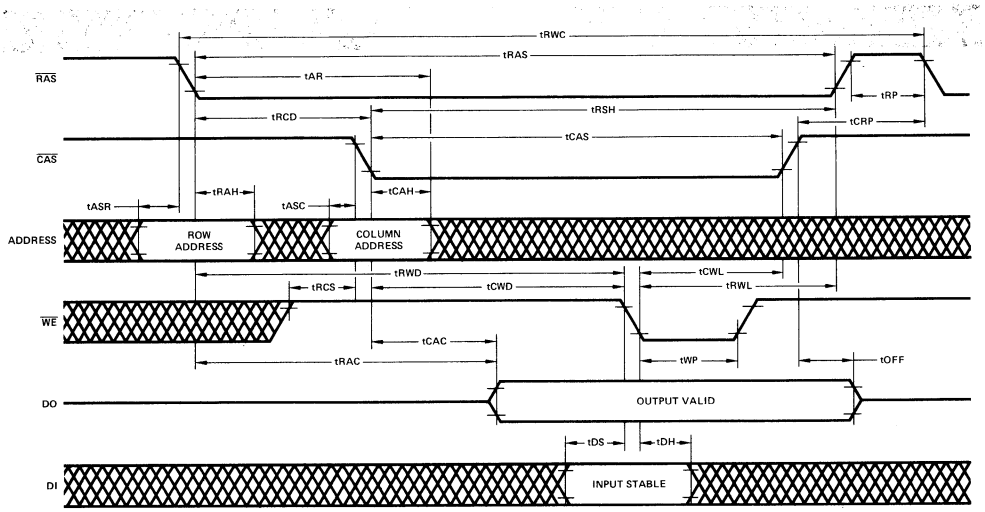
READ-WRITE/READ-MODIFY-WRITE CYCLE



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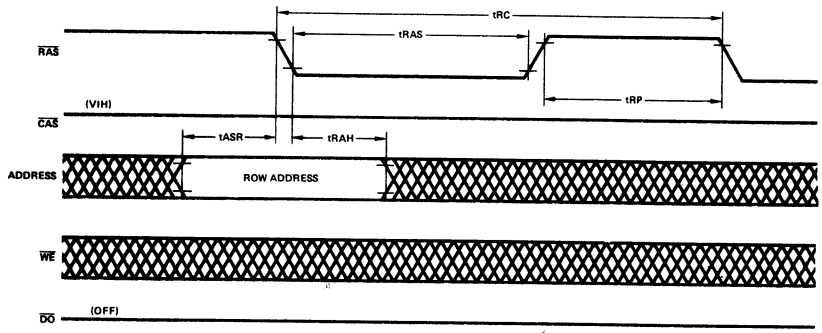
SWITCHING WAVEFORMS (Cont.)

$\overline{RAS}$ ONLY REFRESH CYCLE



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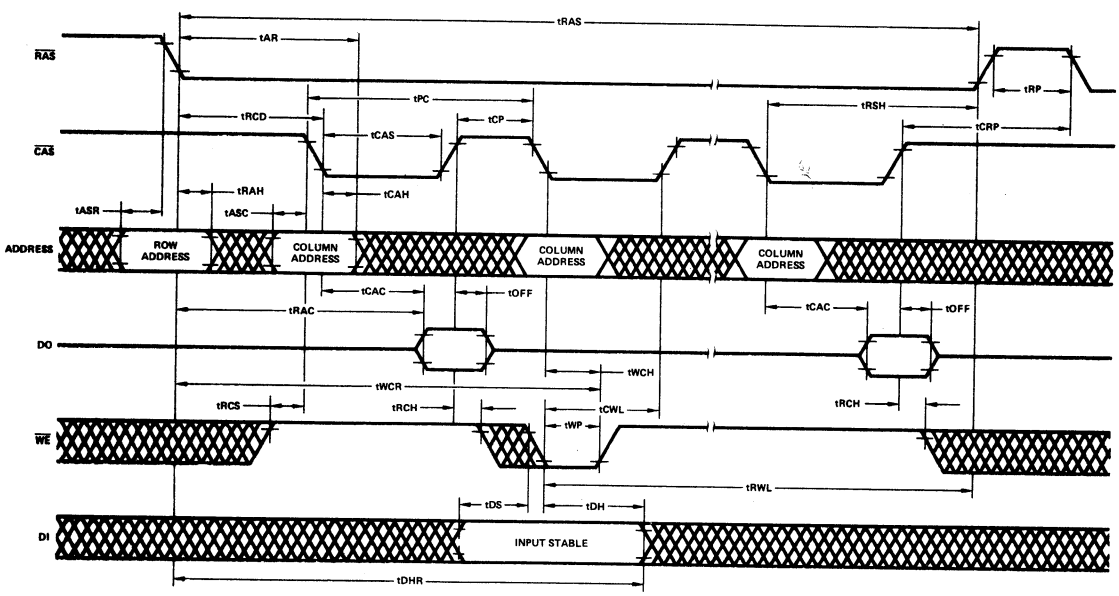
PAGE MODE CYCLE



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APPLICATION INFORMATION

The Am9016 electrical connections are such that if power is applied with the device installed upside down it will be permanently damaged. Precautions should be taken to avoid this mishap.

OPERATING CYCLES

Random read operations from any location hold the $\overline{WE}$ line high and follow this sequence of events:

1) The row address is applied to the address inputs and $\overline{RAS}$ is switched low.
2) After the row address hold time has elapsed, the column address is applied to the address inputs and $\overline{CAS}$ is switched low.
3) Following the access time, the output will turn on and valid read data will be present. The data will remain valid as long as $\overline{CAS}$ is low.
4) $\overline{CAS}$ and $\overline{RAS}$ are then switched high to end the operation. A new cycle cannot begin until the precharge period has elapsed.

Random write operations follow the same sequence of events, except that the $\overline{WE}$ line is low for some portion of the cycle. If the data to be written is available early in the cycle, it will usually be convenient to simply have $\overline{WE}$ low for the whole write operation.

Sequential Read and Write operations at the same location can be designed to save time because re-addressing is not necessary. A read/write cycle holds $\overline{WE}$ high until a valid read is established and then strobes new data in with the falling edge of $\overline{WE}$.

After the power is first applied to the device, the internal circuit requires execution of at least two initialization cycles which exercise both $\overline{RAS}$ and $\overline{CAS}$ before valid memory accesses are begun.

The Am9016 draws most of its power as transients that occur as a result of address strobe switching. Thus, power dissipation for a given part will be a function of strobe duty cycles. The Am9016E may be operated at a maximum cycle rate of 375ns in an ambient environment of +70°C. Memory read or memory write cycles may also be reduced from 375ns to as low as 330ns when the ambient temperature is maintained at +70°C. Figure 1 shows cycle time versus ambient temperature relationship.

Maximum Ambient Temperature Versus Cycle Rate

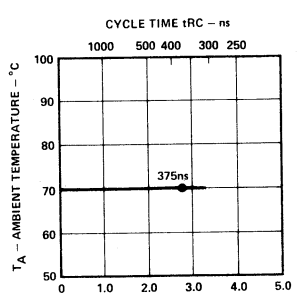

Figure 1.

ADDRESSING

14 address bits are required to select one location out of the 16,384 cells in the memory. Two groups of 7 bits each are multiplexed onto the 7 address lines and latched into the internal address registers. Two negative-going external clocks are used to control the multiplexing. The Row Address Strobe ($\overline{RAS}$) enters the row address bits and the Column Address Strobe ($\overline{CAS}$) enters the column address bits.

When $\overline{RAS}$ is inactive, the memory enters its low power standby mode. Once the row address has been latched, it need not be changed for successive operations within the same row, allowing high-speed page-mode operations.

Page-mode operations first establish the row address and then maintain $\overline{RAS}$ low while $\overline{CAS}$ is repetitively cycled and designated operations are performed. Any column address within the selected row may be accessed in any sequence. The maximum time that $\overline{RAS}$ can remain low is the factor limiting the number of page-mode operations that can be performed.

Multiplexed addressing does not introduce extra delays in the access path. By inserting the row address first and the column address second, the memory takes advantage of the fact that the delay path through the memory is shorter for column addresses. The column address does not propagate through the cell matrix as the row address does and it can therefore arrive somewhat later than the row address without impacting the access time.

REFRESH

The Am9016 is a dynamic memory and each cell must be refreshed at least once every refresh interval in order to maintain the cell contents. Any operation that accesses a row serves to refresh all 128 cells in the row. Thus the refresh requirement is met by accessing all 128 rows at least once every refresh interval. This may be accomplished, in some applications, in the course of performing normal operations. Alternatively, special refresh operations may be initiated. These special operations could be simply additional conventional accesses or they could be "$\overline{RAS}$-only" cycles. Since only the rows need to be addressed, $\overline{CAS}$ may be held high while $\overline{RAS}$ is cycled and the appropriate row addresses are input. Power required for refreshing is minimized and simplified control circuitry will often be possible.

DATA INPUT/OUTPUT

Data is written into a selected cell by the combination of $\overline{WE}$ and $\overline{CAS}$ while $\overline{RAS}$ is low. The later negative transition of $\overline{WE}$ or $\overline{CAS}$ strobes the data into the internal register. In a write cycle, if the $\overline{WE}$ input is brought low prior to $\overline{CAS}$, the data is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the cycle is a read/write cycle then the data set-up and hold times are referenced to the negative edge of $\overline{WE}$.

In the read cycle the data is read by maintaining $\overline{WE}$ in the high state throughout the portion of the memory cycle in which $\overline{CAS}$ is low. The selected valid data will appear at the output within the specified access time.

DATA OUTPUT CONTROL

Any time $\overline{CAS}$ is high the data output will be off. The output contains either one or zero during read cycle after the access time has elapsed. Data remains valid from the access time until $\overline{CAS}$ is returned to the high state. The output data is the same polarity as the input data.

APPLICATION INFORMATION (Cont.)

The user can control the output state during write operations by controlling the placement of the $\overline{WE}$ signal. In the "early write" cycle (see note 9) the output is at a high impedance state throughout the entire cycle.

POWER CONSIDERATIONS

$\overline{RAS}$ and/or $\overline{CAS}$ can be decoded and used as a chip select signal for the Am9016 but overall system power is minimized if $\overline{RAS}$ is used for this purpose. The devices which do not receive $\overline{RAS}$ will be in low power standby mode regardless of the state of $\overline{CAS}$.

Figure 2 shows the change in IDD supply current as a function of operating cycle rate.

At all times the Absolute Maximum Rating Conditions must be observed. During power supply sequencing VBB should never be more positive than VSS when power is applied to VDD.

Maximum IDD Versus Cycle Rate

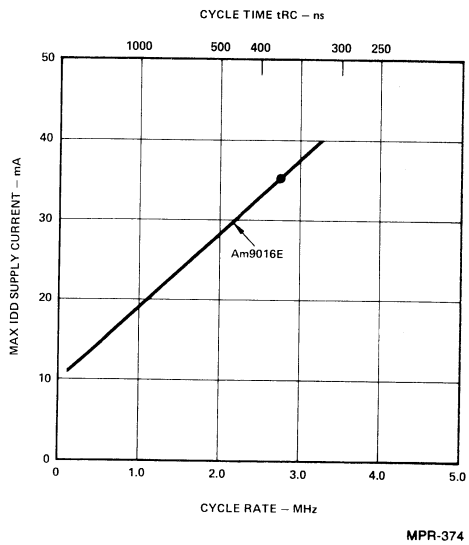

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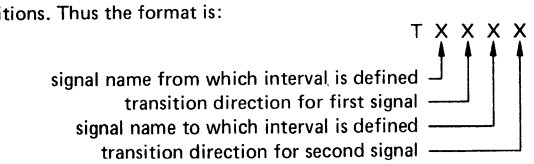
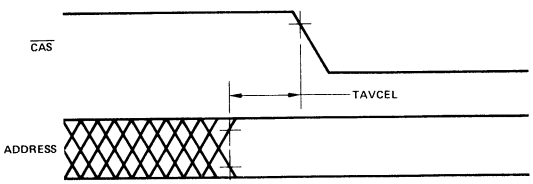
Figure 2.

PARAMETER ABBREVIATIONS

The Switching Characteristics table includes an extra column of parameter abbreviations. They illustrate a new type of specification nomenclature designed to help clarify signal symbols and make data sheet information more consistent.

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors that specify two signal points arranged in a 'from-to' sequence that define a timing interval. The descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:



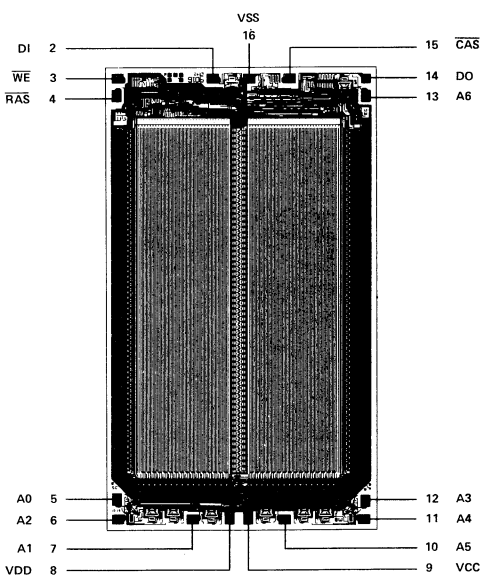


The drawing shows a column address setup time defined as TAVCEL, Address Valid to Column Enable Low time.

The signal definitions used in this data sheet are:
A = Address
D = Data In
Q = Data Out
W = Write Enable
RE = Row Address Strobe
CE = Column Address Strobe

The transition definitions used in this data sheet are:
H = transition to high
L = transition to low
V = transition to valid
X = transition to invalid or don't care
Z = transition to off (high impedance)

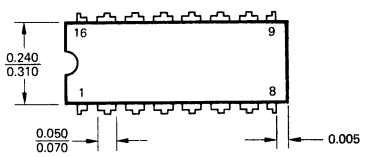
Metallization and Pad Layout

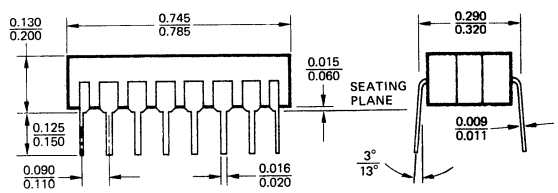


DIE SIZE 0.136" X 0.233"

PHYSICAL DIMENSIONS
Dual-In-Line

16-Pin Hermetic





Am9218/8316E

2048 x 8 Read Only Memory

DISTINCTIVE CHARACTERISTICS

- 2048 x 8 organization
- Plug-in replacement for 8316E
- Access times as fast as 350 ns
- Fully capacitive inputs — simplified driving
- 3 fully programmable Chip Selects — increased flexibility
- Logic voltage levels compatible with TTL
- Three-state output buffers — simplified expansion
- Drives two full TTL loads
- Single supply voltage — +5.0V
- Low power dissipation
- N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

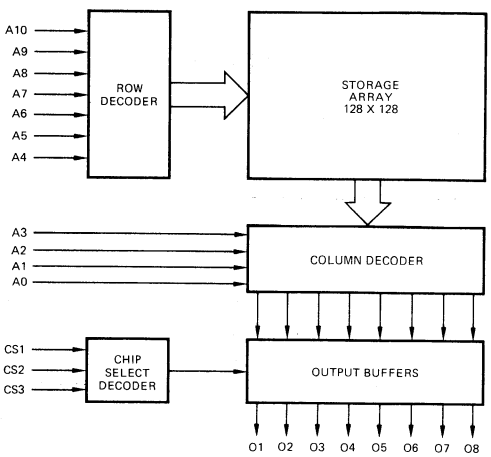
FUNCTIONAL DESCRIPTION

The Am9218 devices are high performance, 16384-bit, static, mask programmed, read only memories. Each memory is implemented as 2048 words by 8 bits per word. This organization simplifies the design of small memory systems and permits incremental memory sizes as small as 2048 words. The fast access times provided allow the ROM to service high performance microcomputer applications without stalling the processor.

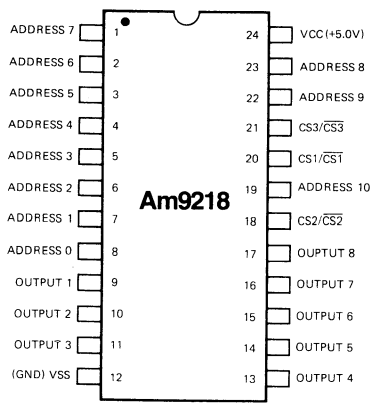
Three programmable Chip Select input signals are provided to control the output buffers. Each Chip Select polarity may be specified by the customer thus allowing the addressing of 8 memory chips without external gating. The outputs of unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am9218 devices and other three-state components.

These memories are fully static and require no clock signals of any kind. A selected chip will output data from a location specified by whatever address is present on the address input lines. Input and output voltage levels are compatible with TTL specifications.

BLOCK DIAGRAM



CONNECTION DIAGRAM



Top View

Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Ambient Temperature Specifications	Access Time	
		450ns	350ns
Hermetic DIP	0°C ≤ T_A ≤ +70°C	AM9218BDC/C8316E	AM9218CDC
		AM9218BCC	AM9218CCC
	−55°C ≤ T_A ≤ +125°C	AM9218BDM	
		AM9218BCM	
Plastic DIP	0°C ≤ T_A ≤ +70°C	AM9218APC/P8316E	AM9218CPC

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
VCC with Respect to VSS	+7.0V
DC Voltage Applied to Outputs	−0.5V to +7.0V
DC Input Voltage	−0.5V to +7.0V
Power Dissipation	1.0W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

ELECTRICAL CHARACTERISTICS

Am9218BDC, Am9218CDC, C8316A: $T_A = 0°C$ to $+70°C$, VCC = 5.0V ±5%

Parameters	Description	Test Conditions		Am9218XDC Min.	Am9218XDC Max.	C8316E Min.	C8316E Max.	Units
VOH	Output HIGH Voltage	9218	IOH = −200μA	2.4				Volts
		8316E	IOH = −100μA			2.4		
VOL	Output LOW Voltage	9218	IOL = 3.2mA		0.4			Volts
		8316E	IOL = 2.1mA				0.4	
VIH	Input HIGH Voltage			2.0	VCC + 1.0	2.0	VCC + 1.0	Volts
VIL	Input LOW Voltage			−0.5	0.8	−0.5	0.8	Volts
ILO	Output Leakage Current	Chip Disabled			10		10	μA
ILI	Input Leakage Current				10		10	μA
ICC	VCC Supply Current				70		95	mA

ELECTRICAL CHARACTERISTICS

Am9218BDM: $T_A = -55°C$ to $+125°C$, VCC = 5.0V ±10%

Parameters	Description	Test Conditions	Am9218B Min.	Am9218B Max.	Units
VOH	Output HIGH Voltage	IOH = −200μA	2.2		Volts
VOL	Output LOW Voltage	IOL = 3.2mA		0.45	Volts
VIH	Input HIGH Voltage		2.0	VCC + 1.0	Volts
VIL	Input LOW Voltage		−0.5	0.8	Volts
ILO	Output Leakage Current	Chip Disabled		10	μA
ILI	Input Leakage Current			10	μA
ICC	VCC Supply Current			80	mA

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

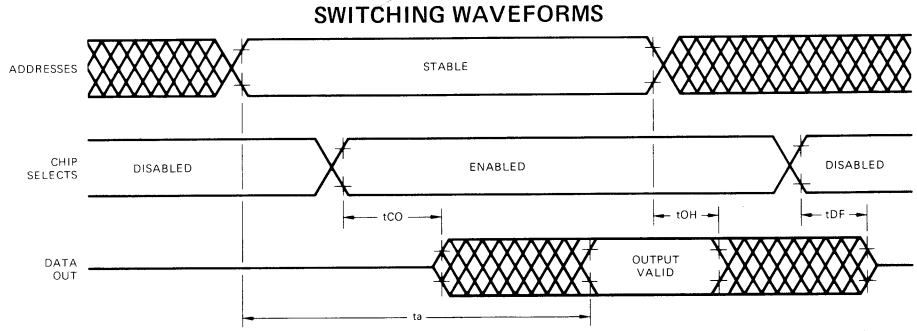
Am9218XDC/C8316E: $T_A = 0°C$ to $+70°C$, VCC = 5.0V ± 5%

Am9218BDM: $T_A = -55°C$ to $+125°C$, VCC = 5.0V ± 10%

Parameters	Description	Test Conditions	Am9218B Min.	Am9218B Max.	Am9218C Min.	Am9218C Max.	8316E Min.	8316E Max.	Units
ta	Address to Output Access Time	tr = tf = 20ns		450		350		450	ns
tCO	Chip Select to Output ON Delay	Output Load:		150		130		250	ns
tOH	Previous Read Data Valid with Respect to Address Change	one standard TTL gate plus 100pF (Note 1)	20		20		–		ns
tDF	Chip Select to Output OFF Delay			150		130		250	ns
CI	Input Capacitance	$T_A = 25°C$, f = 1.0MHz		7.0		7.0		7.0	pF
CO	Output Capacitance	All pins at 0V		7.0		7.0		7.0	pF

Notes: 1. Timing reference levels: High = 2.0V, Low = 0.8V.

SWITCHING WAVEFORMS



PROGRAMMING INSTRUCTIONS

CUSTOM PATTERN ORDERING INFORMATION

The Am9218 is programmed from punched cards, card coding forms or paper tape in card image format as shown below.
Logic "1" = a more positive voltage (normally +5.0 V)
Logic "0" = a more negative voltage (normally 0 V)

FIRST CARD

Column Number	Description
10 thru 29	Customer Name
32 thru 37	Total number of "1's" contained in the data. This is optional and should be left blank if not used.
50 thru 62	8316E or 9218
65 thru 72	Optional information

SECOND CARD

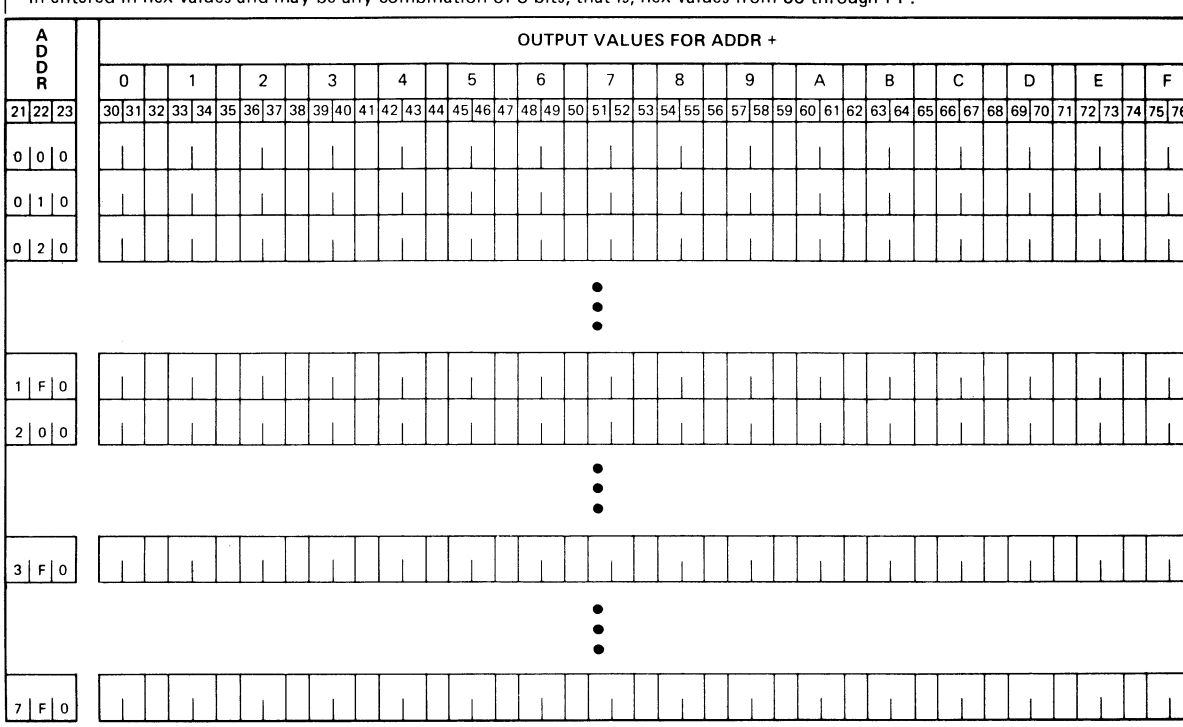
Column Number	Description
29	CS3 input required to select chip (0 or 1)
31	CS2 input required to select chip (0 or 1)
33	CS1 input required to select chip (0 or 1)

Two options are provided for entering the data pattern with the remaining cards.

OPTION 1 is the Binary Option where the address and data are presented in binary form on the basis of one word per card. With this option 2048 data cards are required.

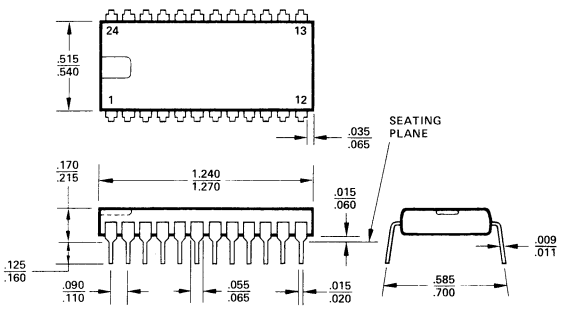
Column Number	
10, 12, 14, 16, 18 20, 22, 24, 26, 28, 30	Address input pattern with the most significant bit (A10) in column 10 and the least significant bit (A0) in column 30.
40, 42, 44, 46, 48, 50, 52, 54	Output pattern with the most significant bit (O8) in column 40 and the least significant bit (O1) in column 54.
73 thru 80	Coding these columns is not essential and may be used for card identification purposes.

OPTION 2 is the Hexadecimal Option and is a much more compact way of presenting the data. This format requires only 128 data cards. Each data card contains the 8-bit output information for 16 storage locations in the memory. The address indicated in columns 21, 22 and 23 is the address of the data presented in columns 30 and 31. Addresses for successive data are assumed to be in incremental ascending order from the initial address. Since the address in columns 21, 22 and 23 always points only to the first data on the card, column 23 is always zero. Columns 21 and 22 take all hex values from 00 through 7F: 128 cards in all. Data in entered in hex values and may be any combination of 8 bits, that is, hex values from 00 through FF.

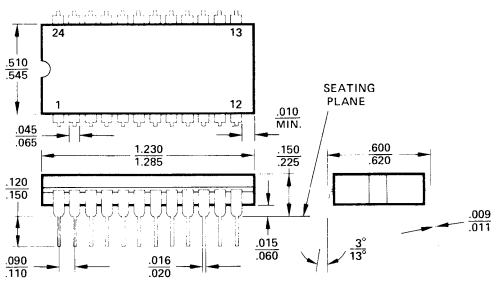


PHYSICAL DIMENSIONS
Dual-In-Line

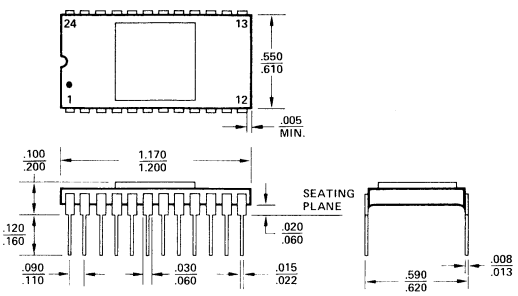
24-Pin Molded



24-Pin Hermetic



24-Pin Side Brazed



Am9232 • Am9233

4096 X 8 Read Only Memory

DISTINCTIVE CHARACTERISTICS

- 4096 X 8 organization
- No clocks or refresh required
- Access time selected to 300ns
- Fully capacitive inputs – simplified driving
- 2 mask programmable chip selects – increased flexibility
- Logic voltage levels compatible with TTL
- Three state output buffers – simplified expansion
- Drives two TTL loads
- Single +5 volt power supply
- Two different pinouts for universal application
- Low power dissipation
- 100% MIL-STD-883 reliability assurance testing
- Non-connect option on chip selects.

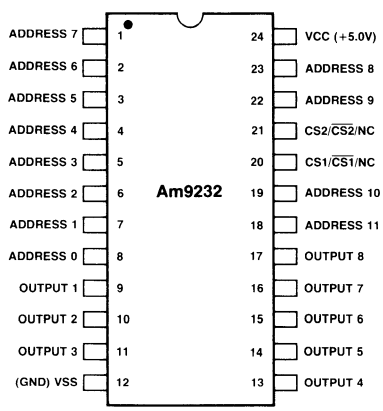
FUNCTIONAL DESCRIPTION

The Am9232/33 devices are high performance, 32,768-bit, static, mask programmed, read only memories. Each memory is implemented as 4096 words by 8 bits per word. This organization simplifies the design of small memory systems and permits incremental memory sizes of 4096 words. The fast access times provided allow the ROM to service high performance microcomputer applications without stalling the processor.

Two programmable Chip Select input signals are provided to control the output buffers. Each Chip Select polarity may be specified by the customer thus allowing the addressing of 4 memory chips without external gating. The outputs of unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am9232/33 devices and other three-state components.

These memories are fully static and require no clock signals of any kind. A selected chip will output data from a location specified by the address present on the address input lines. Input and output voltage levels are compatible with TTL specifications.

CONNECTION DIAGRAMS
Top Views



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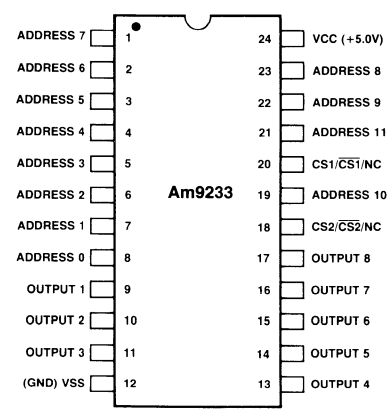


MOS-104

Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Ambient Temperature Specifications	Access Time	
		450ns	300ns
Molded	$0°C \leq T_A \leq +70°C$	AM9232/33BPC	AM9232/33CPC
Cerdip	$0°C \leq T_A \leq +70°C$	AM9232/33BCC	AM9232/33CCC
Side-Brazed Ceramic	$-55°C \leq T_A \leq +125°C$	AM9232/33BDM	
	$0°C \leq T_A \leq +70°C$	AM9232/33BDC	AM9232/33CDC

MAXIMUM RATINGS beyond which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
VCC with Respect to VSS	+7.0V
DC Voltage Applied to Outputs	−0.5V to +7.0V
DC Input Voltage	−0.5V to +7.0V
Power Dissipation (Package Limitation)	1.0W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	VCC	VSS
Am9232DC/PC/CC	$0°C \leq T_A \leq +70°C$	+5.0V ±5%	0V
Am9232/33DM	$-55°C \leq T_A \leq +125°C$	+5.0V ±10%	0V

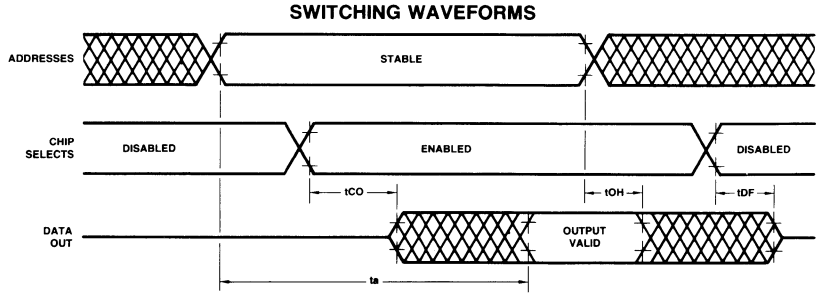
ELECTRICAL CHARACTERISTICS over operating range

Parameter	Description	Test Conditions		Am9232/Am9233 Min.	Am9232/Am9233 Max.	Unit
VOH	Output HIGH Voltage	IOH = −200μA	VCC = 4.75	2.4		Volts
			VCC = 4.50	2.2		
VOL	Output LOW Voltage	IOL = 3.2mA			0.4	Volts
VIH	Input HIGH Voltage			2.0	VCC+1.0	Volts
VIL	Input LOW Voltage			−0.5	0.8	Volts
I_{LI}	Input Load Current	VSS ≤ VI ≤ VCC			10	μA
IOZ	Output Leakage Current	VSS ≤ VO ≤ VCC Chip Disabled	+70°C		10	μA
			+125°C (DM)		50	
ICC	VCC Supply Current		0°C		80	mA
			−55°C (DM)		100	
CI	Input Capacitance	T_A = 25°C, f = 1.0MHz All pins at 0V			7.0	pF
CO	Output Capacitance				7.0	pF

SWITCHING CHARACTERISTICS over operating range

Parameter	Description	Test Conditions	Am9232/33B Min.	Am9232/33B Max.	Am9232/33C Min.	Am9232/33C Max.	Unit
ta	Address to Output Access Time	tr = tf = 20ns Output Load: one standard TTL gate plus 100pF (Note 1)		450		300	ns
tCO	Chip Select to Output ON Delay			150		120	ns
tOH	Previous Read Data Valid with Respect to Address Change		20		20		ns
tDF	Chip Select to Output OFF Delay			150		120	ns

SWITCHING WAVEFORMS



MOS-105

PROGRAMMING INTRUCTIONS

CUSTOM PATTERN ORDERING INFORMATION

The Am9232 is programmed from punched cards, card coding forms or paper tape in card image format as shown below.

Logic "1" = a more positive voltage (normally +5.0V)
Logic "0" = a more negative voltage (normally 0V)

FIRST CARD

Column Number	Description
10 thru 29	Customer Name
32 thru 37	Total number of "1's" contained in the data. This is optional and should be left blank if not used.
50 thru 62	9232 or 9233
65 thru 72	Optional information

SECOND CARD

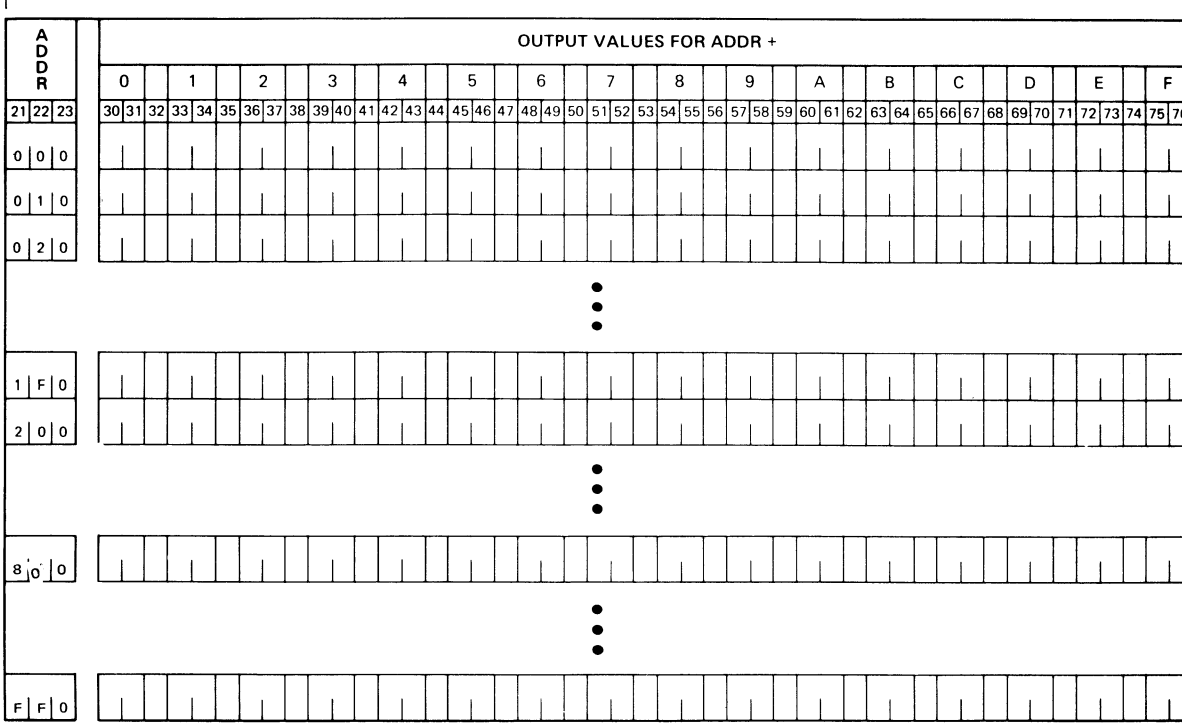
Column Number	Description
31	CS2 input required to select chip (0 or 1); If CS2 = NC, column 31 = 2.
33	CS1 input required to select chip (0 or 1); If CS1 = NC, column 33 = 2.

Two options are provided for entering the data pattern with the remaining cards.

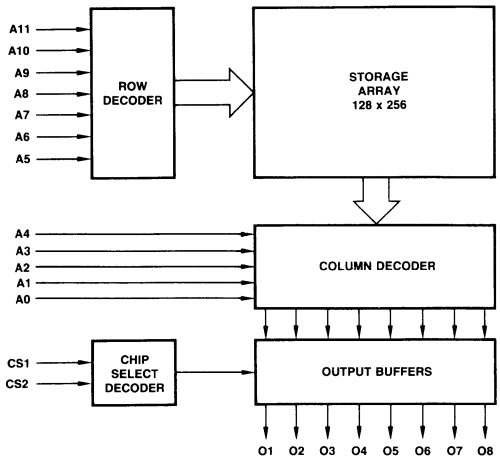
OPTION 1 is the Binary Option where the address and data are presented in binary form on the basis of one word per card. With this option 4096 data cards are required.

Column Number	
8, 10, 12, 14, 16, 18 20, 22, 24, 26, 28, 30	Address input pattern with the most significant bit (A11) in column 8 and the least significant bit (A0) in column 30.
40, 42, 44, 46, 48 50, 52, 54	Output pattern with the most significant bit (O8) in column 40 and the least significant bit (O1) in column 54.
73 thru 80	Coding these columns is not essential and may be used for card identification purposes.

OPTION 2 is the Hexadecimal Option and is a much more compact way of presenting the data. This format requires only 256 data cards. Each data card contains the 8-bit output information for 16 storage locations in the memory. The address indicated in columns 21, 22 and 23 is the address of the data presented in columns 30 and 31. Addresses for successive data are assumed to be in incremental ascending order from the initial address. Since the address in columns 21, 22 and 23 always points only to the first data on the card, column 23 is always zero. Columns 21 and 22 take all hex values from 00 through FF:256 cards in all. Data is entered in hex values and may be any combination of 8 bits, that is, hex values from 00 through FF.



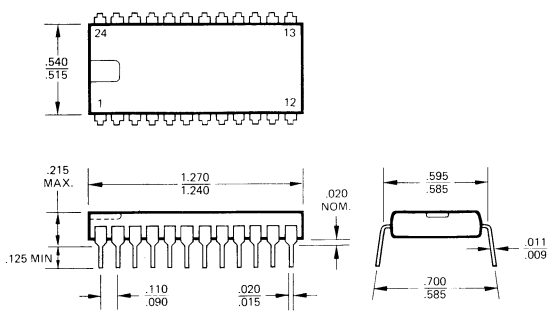
Am9232/Am9233
BLOCK DIAGRAM



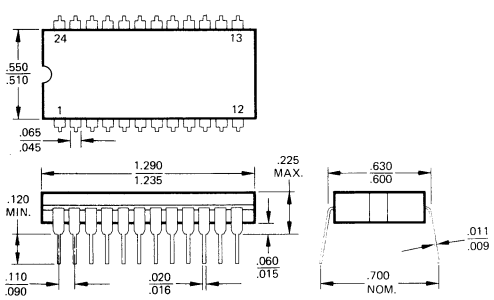
MOS-106

PHYSICAL DIMENSIONS

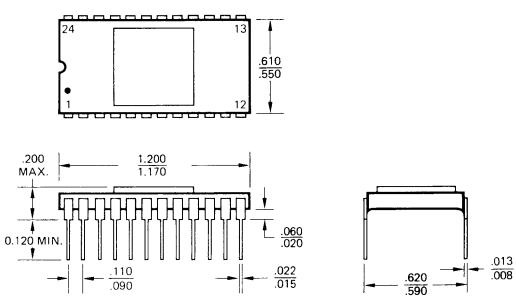
24-Pin Plastic DIP



24-Pin Cerdip



Dual-In-Line 24-Pin Side Brazed



Support and Peripheral Circuits

Am6070

Companding D-to-A Converter for Control Systems

Distinctive Characteristics

- Tested to μ-255 companding law
- Absolute accuracy specified – includes all errors over temperature range
- Settling time 300ns typical
- Ideal for multiplexed PCM, audio, and 8-bit μ-P systems
- Output dynamic range of 72 dB
- 12-bit accuracy and resolution around zero
- Sign plus 12-bit range with sign plus 7-bit coding
- Improved pin-for-pin replacement for DAC-76
- Microprocessor controlled operations
- Multiplying operation
- Negligible output noise
- Monotonicity guaranteed over entire dynamic range
- Wide output voltage compliance
- Low power consumption

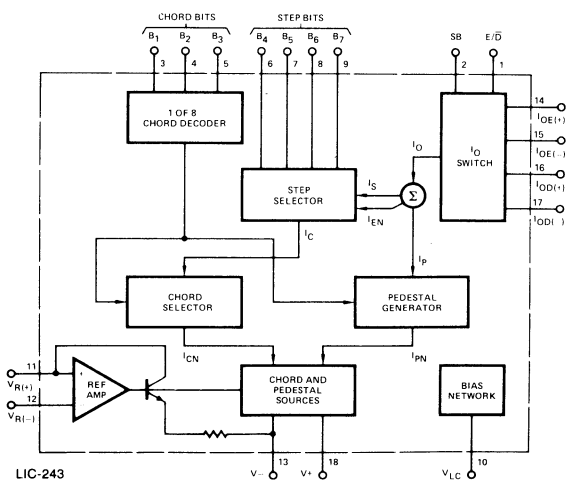
GENERAL DESCRIPTION

The Am6070 monolithic companding D/A converter achieves a 72dB dynamic range which is equivalent to that achieved by a 12-bit converter.

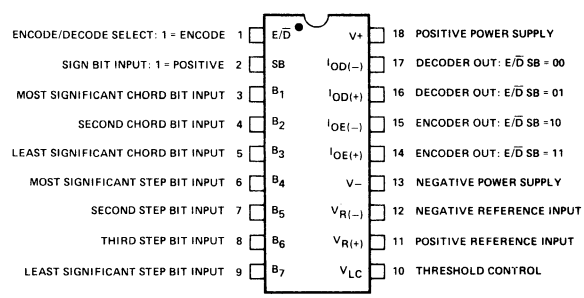
The transfer function of the Am6070 complies with the Bell system μ-255 companding law, and consists of 15 linear segments or chords. A particular chord is identified with the sign bit input, (SB) and three chord select input bits. Each chord contains 16 uniformly spaced linear steps which are determined by four step select input bits. Accuracy and monotonicity are assured by the internal circuit design and are guaranteed over the full temperature range.

Applications for the Am6070 include digital audio recording, servo-motor controls, electromechanical positioning, voice synthesis, secure communications, microprocessor controlled sound and voice systems, log sweep generators and various data acquisition systems.

FUNCTIONAL BLOCK DIAGRAM



CONNECTION DIAGRAM
Am6070



Top View
Pin 1 is marked for orientation.

LIC-244

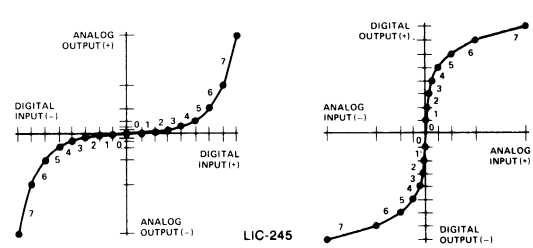
ORDERING INFORMATION

Part Number	Temperature	Accuracy
Am6070ADM	−55°C to +125°C	±1/2 step
Am6070DM	−55°C to +125°C	±1 step
Am6070ADC	0°C to +70°C	±1/2 step
Am6070DC	0°C to +70°C	±1 step

SIMPLIFIED CONVERSION TRANSFER FUNCTIONS

Decoder Characteristic

Encoder Characteristic



LIC-245

MAXIMUM RATINGS above which useful life may be impaired

V+ Supply to V− Supply	36V	Operating Temperature	
V_{LC} Swing	V− plus 8V to V+	MIL Grade	−55°C to +125°C
Output Voltage Swing	V− plus 8V to V− plus 36V	COM'L Grade	0°C to +70°C
Reference Inputs	V− to V+	Storage Temperature	−65°C to +150°C
Reference Input Differential Voltage	±18V	Power Dissipation $T_A \leq 100°C$	500mW
Reference Input Current	1.25mA	For $T_A > 100°C$ derate at	10mW/°C
Logic Inputs	V− plus 8V to V− plus 36V	Lead Soldering Temperature	300°C (60 sec)

GUARANTEED FUNCTIONAL SPECIFICATIONS

Resolution	±128 Steps
Monotonicity	For both groups of 128 steps and over full operating temperature range
Dynamic Range	72 dB, (20 log ($I_{7,15}/I_{0,1}$))

ELECTRICAL CHARACTERISTICS

These specifications apply for V+ = +15V, V− = −15V, I_{REF} = 528μA, 0°C ≤ T_A ≤ +70°C, for the commercial grade, −55°C ≤ T_A ≤ +125C, for the military grade, and for all 4 outputs unless otherwise specified.

Parameter	Description	Test Conditions	Am6070ADM / Am6070ADC Min.	Typ.	Max.	Am6070DM / Am6070DC Min.	Typ.	Max.	Units
t_S	Settling Time	To within ±1/2 step at T_A = 25°C output switched from I_{ZS} to I_{FS}		300	500		300	500	ns
	Chord Endpoint Accuracy	Guaranteed by output current error specified below.			±1/2			±1	Step
	Step Nonlinearity				±1/2			±1	Step
$I_{FS(D)}$	Full Scale Current Deviation				±1/2			±1	
$I_{FS(E)}$	From Ideal				±1/2			±1	
ΔI_O	Output Current Error	V_{REF} = 10.000V R_{REF+} = 18.94kΩ R_{REF-} = 20kΩ −5.0V ≤ V_{OUT} ≤ +18V Error referred to nominal values in Table 1.			±1/2			±1	Step
$I_{O(+)} - I_{O(-)}$	Full Scale Symmetry Error	V_{REF} = 10.000V R_{REF+} = 18.94kΩ R_{REF} = 20kΩ −5.0V ≤ V_{OUT} ≤ +18V Error referred to nominal values in Table 1		1/40 1/40	1/8 1/8		1/20 1/20	1/4 1/4	Step Step
I_{EN}	Encode Current	Additional output Encode/Decode = 1	3/8	1/2	5/8	1/4	1/2	3/4	Step
I_{ZS}	Zero Scale Current	Measured at selected output with 000 0000 input		1/40	1/4		1/20	1/2	Step
ΔI_{FS}	Full Scale Drift	Operating temperature range		±1/20	±1/4		±1/10	±1/2	Step
V_{OC}	Output Voltage Compliance	Full scale current change ≤1/2 step	−5.0		+18	−5.0		+18	Volts
I_{DIS}	Disable Current	Output leakage Output disabled by E/$\overline{D}$ and SB		5.0	50		5.0	50	nA
I_{FSR}	Output Current Range		0	2.0	4.2	0	2.0	4.2	mA
V_{IL}	Logic Input Levels Logic "0"	V_{LC} = 0V			0.8			0.8	Volts
V_{IH}	Logic Input Levels Logic "1"		2.0			2.0			
I_{IN}	Logic Input Current	V_{IN} = −5.0V to +18V			40			40	μA
V_{IS}	Logic Input Swing	V− = −15V	−5.0		+18	−5.0		+18	Volts
$I_{B\ REF-}$	Reference Bias Current			−1.0	−4.0		−1.0	−4.0	μA
di/dt	Reference Input Slew Rate		0.12	0.25		0.12	0.25		mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	V+ = 4.5 to 18V, V− = −15V	±1/20	±1/2		±1/20	±1/2		Step
$PSSI_{FS-}$		V− = 10.8 + −18V, V+ = 15V	±1/10	±1/2		±1/10	±1/2		Step
I+	Power Supply Current	V+ = +5.0 to +15V, V− = −15V		2.7	4.0		2.7	4.0	mA
I−		I_{FS} = 2.0mA		−6.7	−8.8		−6.7	−8.8	
P_D	Power Dissipation	V− = −15V, V_{OUT} = 0, V+ = 5.0V		114	152		114	152	mW
		I_{FS} = 2.0mA, V+ = +15V		141	192		141	192	

ELECTRICAL CHARACTERISTICS (Cont.)

TABLE 1
NOMINAL DECODER OUTPUT CURRENT LEVELS IN μA

	CHORD							
STEP	0	1	2	3	4	5	6	7
0	.000	8.250	24.750	57.750	123.75	255.75	519.75	1047.75
1	.500	9.250	26.750	61.750	131.75	271.75	551.75	1111.75
2	1.000	10.250	28.750	65.750	139.75	287.75	583.75	1175.75
3	1.500	11.250	30.750	69.750	147.75	303.75	615.75	1239.75
4	2.000	12.250	32.750	73.750	155.75	319.75	647.75	1303.75
5	2.500	13.250	34.750	77.750	163.75	335.75	679.75	1367.75
6	3.000	14.250	36.750	81.750	171.75	351.75	711.75	1431.75
7	3.500	15.250	38.750	85.750	179.75	367.75	743.75	1495.75
8	4.000	16.250	40.750	89.750	187.75	383.75	775.75	1559.75
9	4.500	17.250	42.750	93.750	195.75	399.75	807.75	1623.75
10	5.000	18.250	44.750	97.750	203.75	415.75	839.75	1687.75
11	5.500	19.250	46.750	101.750	211.75	431.75	871.75	1751.75
12	6.000	20.250	48.750	105.750	219.75	447.75	903.75	1815.75
13	6.500	21.250	50.750	109.750	227.75	463.75	935.75	1879.75
14	7.000	22.250	52.750	113.750	235.75	479.75	967.75	1943.75
15	7.500	23.250	54.750	117.750	243.75	495.75	999.75	2007.75
STEP SIZE	.5	1	2	4	8	16	32	64

TABLE 2
IDEAL DECODER OUTPUT VALUES EXPRESSED IN dB DOWN FROM FULL SCALE

	CHORD							
STEP	0	1	2	3	4	5	6	7
0	–	−47.73	−38.18	−30.82	−24.20	−17.90	−11.74	−5.65
1	−72.07	−46.73	−37.51	−30.24	−23.66	−17.37	−11.22	−5.13
2	−66.05	−45.84	−36.88	−29.70	−23.15	−16.87	−10.73	−4.65
3	−62.53	−45.03	−36.30	−29.18	−22.66	−16.40	−10.27	−4.19
4	−60.03	−44.29	−35.75	−28.70	−22.21	−15.96	−9.83	−3.75
5	−58.10	−43.61	−35.24	−28.24	−21.77	−15.53	−9.41	−3.33
6	−56.51	−42.98	−34.75	−27.80	−21.36	−15.13	−9.01	−2.94
7	−55.17	−42.39	−34.29	−27.39	−20.96	−14.74	−8.63	−2.56
8	−54.01	−41.84	−33.85	−26.99	−20.58	−14.37	−8.26	−2.19
9	−52.99	−41.32	−33.44	−26.61	−20.22	−14.02	−7.91	−1.84
10	−52.07	−40.83	−33.04	−26.25	−19.87	−13.68	−7.57	−1.51
11	−51.25	−40.37	−32.66	−25.90	−19.54	−13.35	−7.25	−1.18
12	−50.49	−39.93	−32.29	−25.57	−19.22	−13.03	−6.93	−0.87
13	−49.80	−39.51	−31.95	−25.25	−18.91	−12.73	−6.63	−0.57
14	−49.15	−39.11	−31.61	−24.94	−18.61	−12.43	−6.34	−0.28
15	−48.55	−38.73	−31.29	−24.63	−18.32	−12.15	−6.06	0.00

THEORY OF OPERATION

Functional Description

The Am6070 is an 8-bit, nonlinear, digital-to-analog converter with high impedance current outputs. The output current value is proportional to the product of the digital inputs and the input reference current. The full scale output current, I_{FS}, is specified by the input binary code 111 1111, and is a linear function of the reference current, I_{REF}. There are two operating modes, encode and decode, which are controlled by the Encode/Decode, (E/$\overline{D}$), input signal. A logic 1 applied to the E/$\overline{D}$ input places the Am6072 in the encode mode and current will flow into the $I_{OE(+)}$ or $I_{OE(-)}$ output, depending on the state of the Sign Bit (SB) input. A logic 0 at the E/$\overline{D}$ input places the Am6070 in the decode mode.

The transfer characteristic is a piece-wise linear approximation to the Bell System μ-225 logarithmic law which can be written as follows:

$$Y = 0.18 \ell n (1 + \mu |X|) \text{ sgn } (X)$$

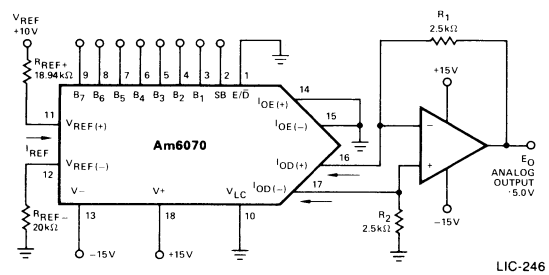
where: X = analog signal level normalized to unity (encoder input or decoder output)
Y = digital signal level normalized to unity (encoder output or decoder input)
μ = 255

The current flows from the external circuit into one of four possible analog outputs determined by the SB and E/$\overline{D}$ inputs. The output current transfer function can be represented by a total of 16 segments or chords addressable through the SB input and three chord select bits. Each chord can be further divided into 16 steps, all of the same size. The step size changes from one chord to another, with the smallest step of 0.5μA found in the first chord near zero output current, and the largest step of 64μA found in the last chord near full scale output current. This nonlinear feature provides exceptional accuracy for small signal levels near zero output current. The accuracy for signal amplitudes corresponding to chord 0 is equivalent to that of a 12-bit linear, binary D/A converter. However, the ratio (in dB) between the chord endpoint current, (Step 15), and the current which corresponds to the preceding step, (Step 14), is maintained at about 0.3dB over most of the dynamic range. The difference between the ratios of full scale current to chord endpoint currents of adjacent chords is similarly maintained at approximately 6dB over most of the dynamic range. Resulting signal-to-quantizing distortions due to non-uniform quantizing levels maintain an acceptably low value over a 40dB range of input speech signals. Note that the 72dB output dynamic range for the Am6070 corresponds to the dynamic range of a sign plus 12-bit linear, binary D/A converter.

In order to achieve a smoother transition between adjacent chords, the step size between these chord end points is equal to 1.5 times the step size of the lower chord. Monotonic operation is guaranteed by the internal device design over the entire output dynamic range by specifying and maintaining the chord end points and step size deviations within the allowable limits.

Operating Modes

The basic converter function is conversion of digital input data into a corresponding analog current signal, i.e., the basic function is digital-to-analog decoding. The basic decoder connection for a sign plus 7-bit input configuration is shown in Figure 1. The corresponding dynamic range is 72dB, and input-output characteristics conform to the standard decoder transfer function with output current values specified in Table 1. The E/$\overline{D}$ input enables switching between the encode, $I_{OE(+)}$ or $I_{OE(-)}$, and the decode, $I_{OD(+)}$ or $I_{OD(-)}$, outputs. A typical encode/decode test circuit is shown in Figure 2. This circuit is used for output current measurements. When the E/$\overline{D}$ input is high, (a logic 1), the converter will assume the encode operating mode and the output current will flow into one of the I_{OE} outputs (as determined by the SB input). When operating in the encode mode as shown in Figure 3, an offset current equal to a half step in each chord is required to obtain the correct encoder transfer characteristic. Since the size of this step varies from one chord to another, it cannot easily be added externally. As indicated in the block diagram this required half step of encode current,

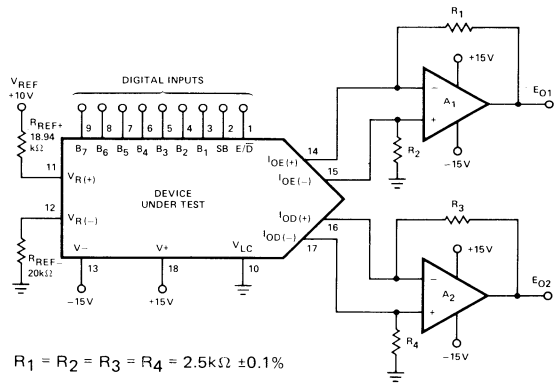


$I_{REF} = V_{REF}/R_{REF}$

IDEAL VALUES: $I_{REF} = 528\mu A$, $I_{FS} = 2007.75\mu A$

	E/$\overline{D}$	SB	B_1	B_2	B_3	B_4	B_5	B_6	B_7	E_O
POSITIVE FULL SCALE	0	1	1	1	1	1	1	1	1	5.019V
(+) ZERO SCALE +1 STEP	0	1	0	0	0	0	0	0	1	0.0012V
(+) ZERO SCALE	0	1	0	0	0	0	0	0	0	0V
( ) ZERO SCALE	0	0	0	0	0	0	0	0	0	0V
( ) ZERO SCALE +1 STEP	0	0	0	0	0	0	0	0	1	-0.0012V
NEGATIVE FULL SCALE	0	0	1	1	1	1	1	1	1	-5.019V

Figure 1. Detailed Decoder Connections.



$R_1 = R_2 = R_3 = R_4 = 2.5k\Omega \pm 0.1\%$

LINE SELECTION TABLE

TEST GROUP	E/$\overline{D}$	SB	OUTPUT MEASUREMENT	
1	1	1	$I_{OE(+)}$	(E_{O1}/R_1)
2	1	0	$I_{OE(-)}$	(E_{O1}/R_2)
3	0	1	$I_{OD(+)}$	(E_{O2}/R_3)
4	0	0	$I_{OD(-)}$	(E_{O2}/R_4)

Figure 2. Output Current DC Test Circuit.

I_{EN}, is automatically added to the I_{OE} output through the internal chip design. This additional current will, for example, make the ideal full scale current in the encode mode larger than the same current in the decode mode by 32μA. Similarly, the current levels in the first chord near the origin will be offset by 0.25μA, which will bring the ideal encode current value for step 0 on chord 0 to $\pm$0.25μA with respect to the corresponding decode current value of 0.0μA. This additional encode half step of current can be used for extension of the output dynamic range from 72dB to 78dB, when the converter is performing only the decode function. The corresponding decoder connection utilizes the E/$\overline{D}$ input as a ninth digital input and has the outputs $I_{OD(+)}$ and $I_{OE(+)}$ and the outputs $I_{OD(-)}$ and $I_{OE(-)}$ tied together, respectively.

When encoding or compression of an analog signal is required, the Am6070 can be used together with a Successive Approximation Register (SAR), comparator, and additional SSI logic elements to perform the A/D data conversion, as shown in Figure 3. The encoder transfer function, shown on page 1, characterizes this A/D converter system. The first task of this system is to determine the polarity of the incoming analog signal and to generate a corresponding SB input value. When the proper Start, $\overline{S}$, and Conversion Complete, $\overline{CC}$, signal levels are set, the first clock pulse sets the MSB output of the SAR, Am2502, to a logic 0 and sets all other parallel digital outputs to logic 1 levels. At the same time, the flip-flop is triggered, and its output provides the E/$\overline{D}$ input with a logic 0 level. No current flows into the I_{OE} outputs. This disconnects the converter from the comparator inputs, and the incoming analog signal can be compared with the ground applied to the opposite comparator input. The resulting comparator output is fed to the Am2502 serial data input, D, through an exclusive-or gate. At the same time, the second input to the same exclusive-or gate is held at a logic 0 level by the additional successive approximation logic shown in Figure 3. This exclusive-or gate inverts the comparator's outputs whenever a negative signal polarity is detected. This maintains the proper output current coding, i.e., all ones for full scale and all zeros for zero scale.

The second clock pulse changes the E/$\overline{D}$ input back to a logic 1 level because the $\overline{CC}$ signal changed. It also clocks the D input signal of the Am2502 to its MSB output, and transfers it to the SB input of the Am6070. Depending upon the SB input level, current will flow into the $I_{OE(+)}$ or $I_{OE(-)}$ output of the Am6070.

Nine total clock pulses are required to obtain a digital binary representation of the incoming analog signal at the eight Am2502 digital outputs. The resulting Am6070 analog output signal is compared with the analog input signal after each of the nine successive clock pulses. The analog signal should not be allowed to change its value during the data conversion time. In high speed systems, fast changes of the analog signals at the A/D system input are usually prevented by using sample and hold circuitry.

Additional Considerations and Recommendations

In Figure 1, an optional operational amplifier converts the Am6070 output current to a bipolar voltage output. When the SB input is a logic 1, sink current appears at the amplifier's negative input, and the amplifier acts as a current to voltage converter, yielding a positive voltage output. With the SB value at a logic 0, sink current appears at the amplifier's positive input. The amplifier behaves as a voltage follower, and the true current outputs will swing below ground with essentially no change in output current. The SB input steers current into the appropriate (+) or (−) output of the Am6070. The resulting operational amplifier's output in Figure 1 should ideally be symmetrical with resistors R1 and R2 matched.

In Figure 2, two operational amplifiers measure the currents of each of the four Am6070 analog outputs. Resistor tolerances of 0.1% give 0.1% output measurement error (approximately 2μA at full scale). The input offset currents of the A1 and A2 devices also increase output measurement error and this error is most significant near zero scale. The Am101A and 308 devices, for example, may be used for A1 and A2 since their maximum offset currents, which would add directly to the measurement error, are only 10nA and 1nA, respectively. The input offset voltages of the A1 and A2 devices, with output resistor values of

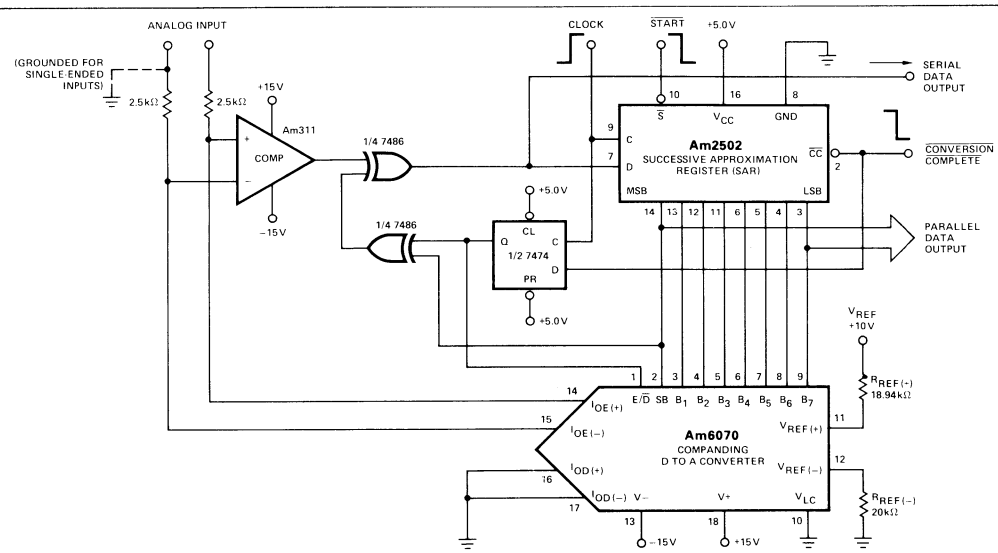


Figure 3. Detailed Encoder Connections.

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2.5kΩ, also contribute to the output measurement error by a factor of 400nA for every mV of offset at the A1 and A2 outputs. Therefore, to minimize error, the offset voltages of A1 and A2 should be nulled.

The recommended operating range for the reference current I_{REF} is from 0.1mA to 1.0mA. The full scale output current, I_{FS}, is a linear function of the reference current, and may be calculated from the equation $I_{FS} = 3.8\ I_{REF}$. This tight relationship between I_{REF} and I_{FS} alleviates the requirement for trimming the I_{REF} current if the R_{REF} resistors values are within ±1% of the calculated value. Lower values of I_{REF} will reduce the negative power supply current, (I−), and will increase the reference amplifier negative common mode input voltage range.

The ideal value for the reference current $I_{REF} = V_{REF}/R_{REF}$ is 528μA. The corresponding ideal full scale decode and encode current values are 2007.75μA and 2039.75μA, respectively. A percentage change from the ideal I_{REF} value produced by changes in V_{REF} or R_{REF} values produces the same percentage change in decode and encode output current values. The positive voltage supply, V+, may be used, with certain precautions, for the positive reference voltage V_{REF}. In this case, the reference resistor $R_{REF(+)}$ should be split into two resistors and their junction bypassed to ground with a capacitor of 0.01μF. The total resistor value should provide the reference current I_{REF} = 528μA. The resistor $R_{REF(-)}$ value should be approximately equal to the $R_{REF(+)}$ value in order to compensate for the errors caused by the reference amplifier's input offset current.

An alternative to the positive reference voltage applications shown in Figures 1, 2 and 3 is the application of a negative voltage to the $V_{R(-)}$ terminal through the resistor $R_{REF(-)}$ with the $R_{REF(+)}$ resistor tied to ground. The advantage of this arrangement is the presence of very high impedance at the $V_{R(-)}$ terminal while the reference current flows from ground through $R_{REF(+)}$ into the $V_{R(+)}$ terminal.

The Am6070 has a wide output voltage compliance suitable for driving a variety of loads. With I_{REF} = 528μA and V− = −15V, positive voltage compliance is +18V and negative voltage compliance is −5.0V. For other values of I_{REF} and V−, the negative voltage compliance, $V_{OC(-)}$, may be calculated as follows:

$$V_{OC(-)} = (V-) + (2 \bullet I_{REF} \bullet 1.5k\Omega) + 8.4V.$$

The following table contains $V_{OC(-)}$ values for some specific V−, I_{REF}, and I_{FS} values.

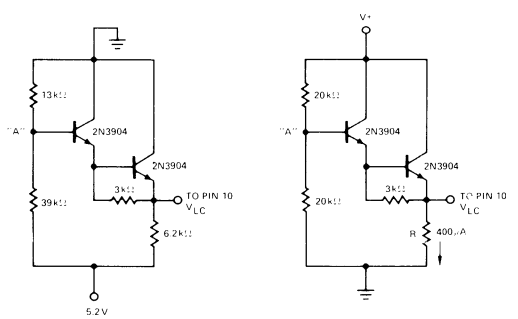
Negative Output Voltage Compliance $V_{OC(-)}$

V− \ I_{REF} (I_{FS})	264μA (1mA)	528μA (2mA)	1056μA (4mA)
−12V	−2.8V	−2.0V	−0.4V
−15V	−5.8V	−5.0V	−3.4V
−18V	−8.8V	−8.0V	−6.4V

The V_{LC} input can accommodate various logic input switching threshold voltages allowing the Am6070 to interface with various logic families. This input should be placed at a potential which is 1.4V below the desired logic input switching threshold. Two external discrete circuits which provide this function for non-TTL driven inputs are shown in Figure 4. For TTL-driven logic inputs, the V_{LC} input should be grounded. If negative voltages are applied at the digital logic inputs, they must have a value which is more positive than the sum of the chosen V− value and +10V.

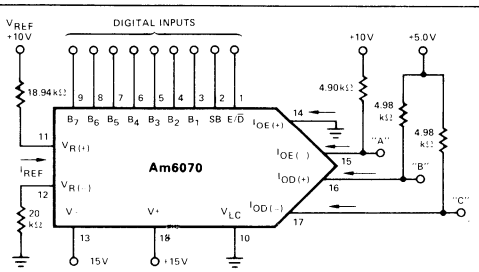
With a V− value chosen between −15V and −11V, the $V_{OC(-)}$, the input reference common mode voltage range, and the logic input negative voltage range are reduced by an amount equivalent to the difference between −15V and the V− value chosen.

With a V+ value chosen between +5V and +15V, the reference amplifier common mode positive voltage range and the V_{LC} input values are reduced by an amount equivalent to the difference between +15V and the V+ value chosen.



(See Notes 2 and 3)

Figure 4. Interfacing Circuits for ECL, CMOS, HTL, and NMOS Logic Inputs. LIC-249



INPUT CODE ($E/\overline{D}$, SB, B_1, . . . , B_7)	OUTPUT VOLTAGE (V) "A"	"B"	"C"	DIFF
10 111 1111	0			
10 110 1111	+5.02	N.A	N.A	N.A
10 000 0000	+10.00			
01 111 1111		5.00	+5.00	10.00
01 110 1111		+0.02	+5.00	4.98
01 000 0000	N.A	+5.00	+5.00	0
00 000 0000		+5.00	+5.00	0
00 110 1111		+5.00	+0.02	+4.98
00 111 1111		+5.00	5.00	+10.00

Figure 5. Resistive Output Connections. LIC-250

Notes: 2. Set the voltage "A" to the desired logic input switching threshold.
3. Allowable range of logic threshold is typically −5V to +13.5V when operating the companding DAC on ±15V supplies.

ADDITIONAL DECODE OUTPUT CURRENT TABLES

Table 3
Normalized Decoder Output (Sign Bit Excluded)

Step (S) \ Chord (C)		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0	33	99	231	495	1023	2079	4191
1	0001	2	37	107	247	527	1087	2207	4447
2	0010	4	41	115	263	559	1151	2335	4703
3	0011	6	45	123	279	591	1215	2463	4959
4	0100	8	49	131	295	623	1279	2591	5215
5	0101	10	53	139	311	655	1343	2719	5471
6	0110	12	57	147	327	687	1407	2847	5727
7	0111	14	61	155	343	719	1471	2975	5983
8	1000	16	65	163	359	751	1535	3103	6239
9	1001	18	69	171	375	783	1599	3231	6495
10	1010	20	73	179	391	815	1663	3359	6751
11	1011	22	77	187	407	847	1727	3487	7007
12	1100	24	81	195	423	879	1791	3615	7263
13	1101	26	85	203	439	911	1855	3743	7519
14	1110	28	89	211	455	943	1919	3871	7775
15	1111	30	93	219	471	975	1983	3999	8031
Step Size		2	4	8	16	32	64	128	256

The normalized decode current, ($I_{C,S}$), is calculated using:

$I_{C,S} = 2(2^C(S + 16.5) - 16.5)$

where C = chord number; S = step number. The ideal decode current, (I_{OD}), in μA is calculated using:

$I_{OD} = (I_{C,S}/I_{7,15(norm.)}) \bullet I_{FS}$ (μA)

where $I_{C,S}$ is the corresponding normalized current. To obtain normalized encode current values the corresponding normalized half-step value should be added to all entries in Table 3.

Table 4
Normalized Encode Level (Sign Bit Excluded)

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	1	35	103	239	511	1055	2143	4319
1	0001	3	39	111	255	543	1119	2271	4575
2	0010	5	43	119	271	575	1183	2399	4831
3	0011	7	47	127	287	607	1247	2527	5087
4	0100	9	51	135	303	639	1311	2655	5343
5	0101	11	55	143	319	671	1375	2783	5599
6	0110	13	59	151	335	703	1439	2911	5855
7	0111	15	63	159	351	735	1503	3039	6111
8	1000	17	67	167	367	767	1567	3167	6367
9	1001	19	71	175	383	799	1631	3295	6623
10	1010	21	75	183	399	831	1695	3423	6879
11	1011	23	79	191	415	863	1759	3551	7135
12	1100	25	83	199	431	895	1823	3679	7391
13	1101	27	87	207	447	927	1887	3807	7647
14	1110	29	91	215	463	959	1951	3935	7903
15	1111	31	95	223	479	991	2015	4063	8159
Step Size		2	4	8	16	32	64	128	256

$I_{C,S} = 2[2^C (S + 17) - 16.5]$

C = chord no. (0 through 7)
S = step no. (0 through 15)

Table 5
Decoder Step Size Summary

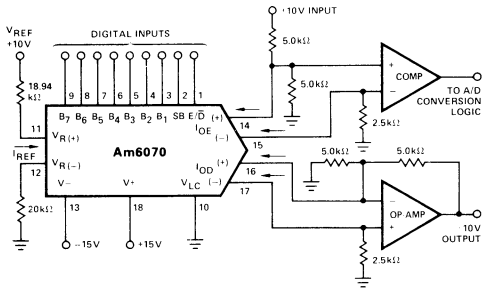
Chord	Step Size Normalized to Full Scale	Step Size in μA with 2007.75μA FS	Step Size as a % of Full Scale	Step Size in dB at Chord Endpoints	Step Size as a % of Reading at Chord Endpoints	Resolution & Accuracy of Equivalent Binary DAC
0	2	0.5	0.025%	0.60	6.67%	Sign + 12 Bits
1	4	1.0	0.05%	0.38	4.30%	Sign + 11 Bits
2	8	2.0	0.1%	0.32	3.65%	Sign + 10 Bits
3	16	4.0	0.2%	0.31	3.40%	Sign + 9 Bits
4	32	8.0	0.4%	0.29	3.28%	Sign + 8 Bits
5	64	16.0	0.8%	0.28	3.23%	Sign + 7 Bits
6	128	32.0	1.6%	0.28	3.20%	Sign + 6 Bits
7	256	64.0	3.2%	0.28	3.19%	Sign + 5 Bits

Table 6
Decoder Chord Size Summary

Chord	Chord Endpoints Normalized to Full Scale	Chord Endpoints in μA with 2007.75μA FS	Chord Endpoints as a % of Full Scale	Chord Endpoints in dB Down from Full Scale
0	30	7.5	0.37%	–48.55
1	93	23.25	1.16%	–38.73
2	219	54.75	2.73%	–31.29
3	471	117.75	5.86%	–24.63
4	975	243.75	12.1%	–18.32
5	1983	495.75	24.7%	–12.15
6	3999	999.75	49.8%	–6.06
7	8031	2007.75	100%	0

BASIC CIRCUIT CONNECTIONS

±10V RANGE ENCODER/DECODER CONNECTIONS



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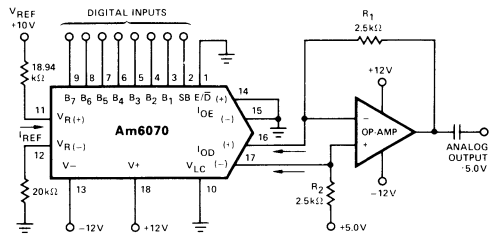
COMPLIANCE EXTENSION USING AC COUPLED OUTPUT



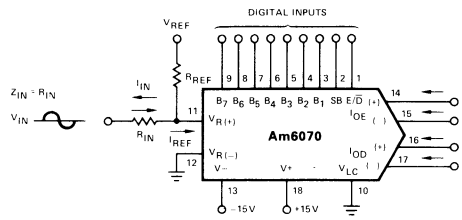
IDEAL VALUES:

$I_{REF} = 528\mu A$

$I_{FS} = 2007.75\mu A$

LIC-252

LOW INPUT IMPEDANCE CONNECTION

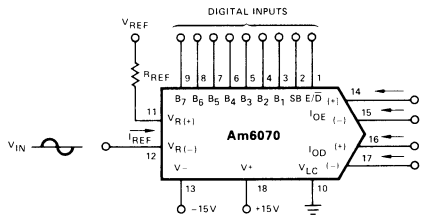


$I_{REF} = V_{IN}/R_{IN} + V_{REF}/R_{REF}$

$I_{FS} \approx 4 \bullet I_{REF}$

LIC-253

HIGH INPUT IMPEDANCE CONNECTION

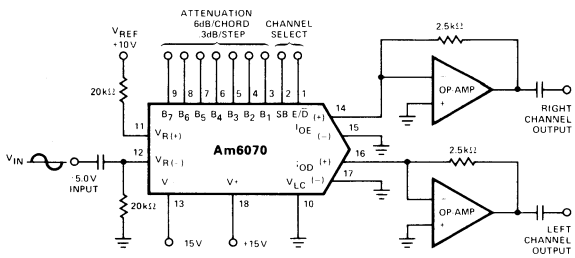


$I_{REF} = (V_{REF} - V_{IN})/R_{REF}$

$I_{FS} \approx 4 \bullet I_{REF}$

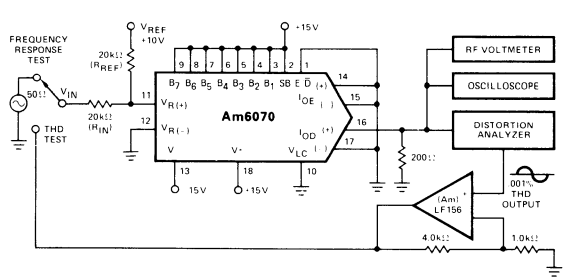
LIC-254

LOGARITHMIC DIGITAL GAIN CONTROL (Notes 4 & 5)



LIC-255

REFERENCE AMPLIFIER DYNAMIC TEST CIRCUIT

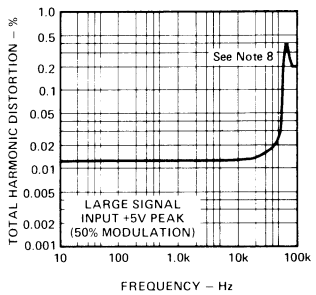


LIC-256

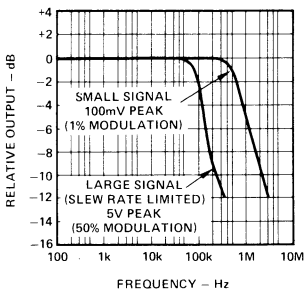
Notes: 4. Low distortion outputs are provided over a 72dB range.
5. Up to 4 channels of output may be selected by E/$\overline{D}$ and SB logic inputs.

TYPICAL PERFORMANCE CURVES

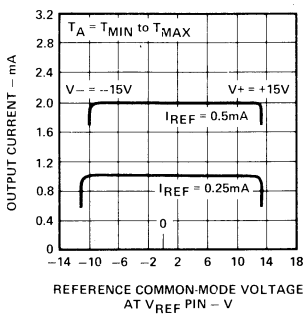
Reference Amplifier Total Harmonic Distortion Versus Frequency (80kHz Filter) (Notes 6, 7, 8)



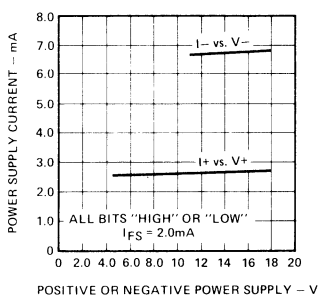
Reference Amplifier Input Frequency Response



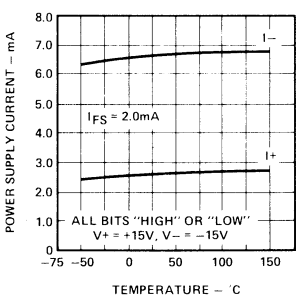
Reference Amplifier Input Common-Mode Range (Note 9)



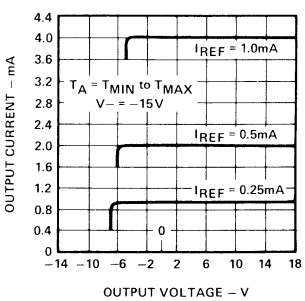
Power Supply Currents Versus Power Supply Voltages



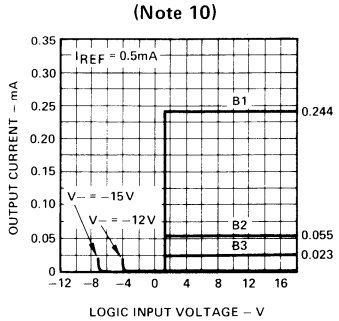
Power Supply Currents Versus Temperature



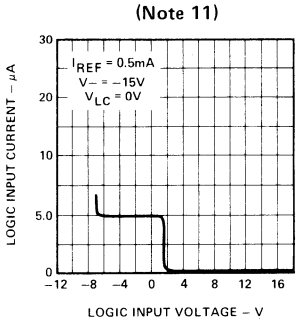
Output Current Versus Output Voltage (Output Voltage Compliance)



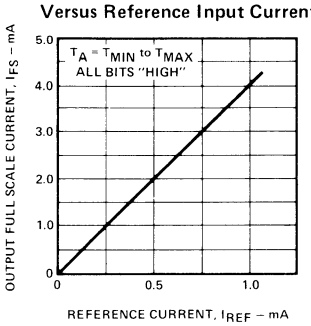
Bit Transfer Characteristics (Note 10)



Logic Input Current Versus Input Voltage and Logic Input Range (Note 11)



Output Full Scale Current Versus Reference Input Current



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Notes:
6. THD is nearly independent of the logic input code.
7. Similar results are obtained for a high input impedance connection using $V_{R(-)}$ as an input.
8. Increased distortion above 50kHz is due to a slew rate limiting effect which determines the large signal bandwidth. For an input of ±2.5V peak (25% modulation), the bandwidth is 100kHz.
9. Positive common mode range is always (V+) –1.5V.
10. All bits are fully switched with less than a half step error at switching points which are guaranteed to lie between 0.8V and 2.0V over the operating temperature range.
11. The logic input voltage range is independent of the positive power supply and logic inputs may swing above the supply.

APPLICATIONS

The companding D/A converter is particularly suited for applications requiring a wide dynamic range.

Systems requiring fine control resulting in a constant rate of change or set point controls are economically achieved using these devices.

Instrumentation, Control and μ-Processor based applications include:

- Digital data recording
- PCM telemetry systems
- Servo systems
- Function generation
- Data acquisition systems

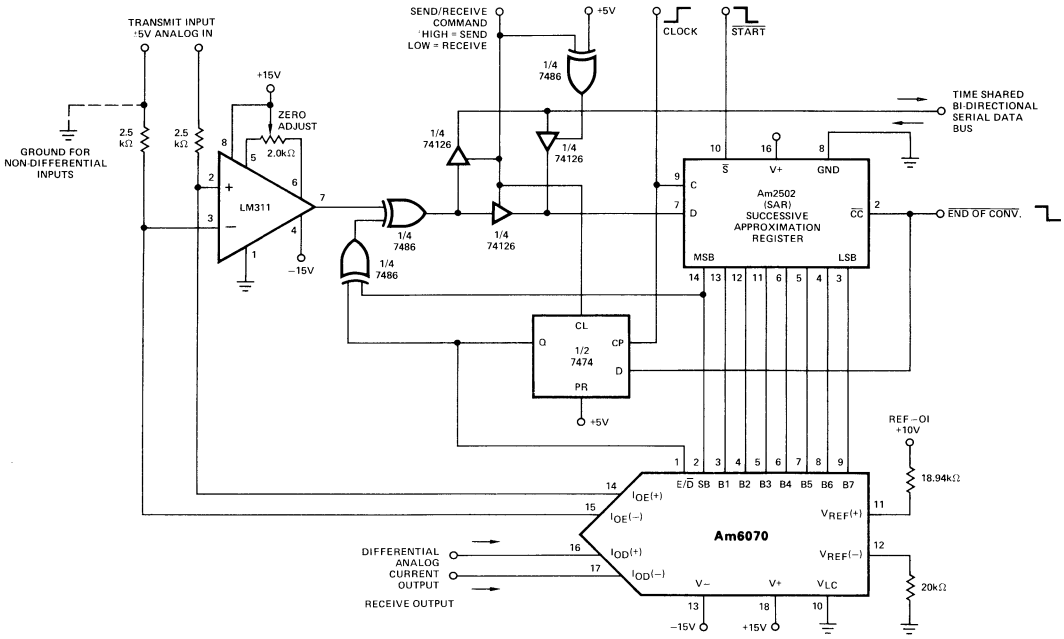
Telecommunications applications include:

- PCM Codec telephone systems
- Intercom systems
- Military voice communication systems
- Radar systems
- Voice Encryption

Audio Applications:

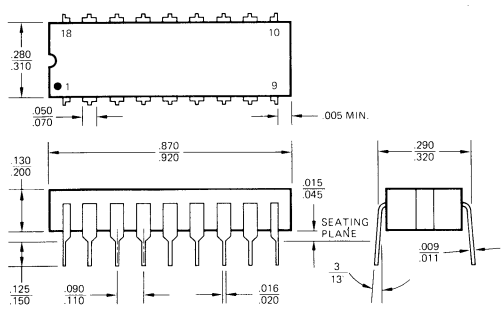
- Recording
- Multiplexing of analog signals
- Voice synthesis

SERIAL DATA TRANSCEIVING CONVERTER
(1/2 OF SYSTEM SHOWN)

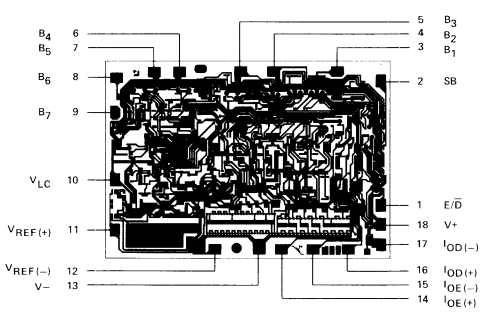


Notes:
1. Complementary send/receive commands are required for the two ends.
2. START must be held low for one clock cycle to begin a send or receive cycle.
3. The SAR is used as a serial-in/parallel out register in the receive mode.
4. CLOCK and START may be connected in parallel at both ends.
5. Conversion is completed in 9 clock cycles.
6. Receive output is available for one full clock cycle.

PHYSICAL DIMENSIONS
18-Pin Hermetic Dual-In-Line



Metallization and Pad Layout



80 X 114 Mils

Am6080

Microprocessor System Compatible 8-Bit High Speed Multiplying D/A Converter

DISTINCTIVE CHARACTERISTICS

- 8-Bit D/A with 8-Bit input data latch
- Compatible with most popular microprocessors including the Am9080A-4 and the Am2900
- Write, Chip Select and Data Enable logic on chip
- DAC appears as memory location to microprocessor
- MSB inversion under logic control
- Differential current output
- Choice of 6 coding formats
- Fast settling current output −160ns
- Nonlinearity to ±0.1% max over temperature range
- Full scale current pre-matched to ±1 LSB
- High output impedance and voltage compliance
- Low full scale current drift − ±5ppm/°C
- Wide range multiplying capability −2.0MHz bandwidth
- Direct interface to TTL, CMOS, NMOS
- High speed data latch − 80ns min write time

GENERAL DESCRIPTION

The Am6080 is a monolithic 8-bit multiplying Digital-to-Analog converter with an 8-bit data latch, chip select and other control signal lines which allow direct interface with microprocessor buses.

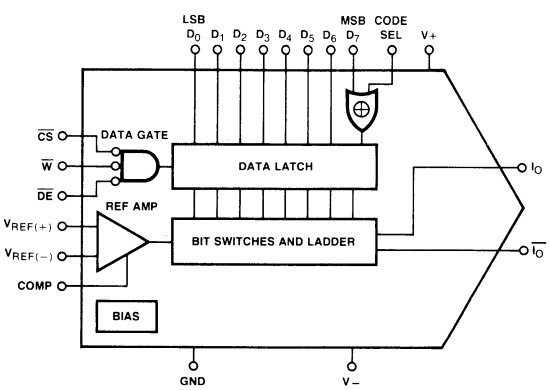
The converter allows a choice of 6 different coding formats. The most significant bit (D_7) can be inverted or non-inverted under the control of the code select input. The code control also provides a zero differential current output for 2's complement coding. A high voltage compliance, complementary current output pair is provided. The data latch is very high speed which makes the Am6080 capable of interfacing with high speed microprocessors.

Monotonic multiplying performance is maintained over a more than 40 to 1 reference current range. Matching within ±1 LSB between reference and full scale current eliminates the need for full scale trimming in most applications.

The Am6080 guarantees full 8-bit monotonicity. Nonlinearities as tight as 0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the full power supply voltage and temperature range.

Applications for the Am6080 include microprocessor compatible data acquisition systems and data distribution systems, 8-bit A/D converters, servo-motor and pen drivers, waveform generators, programmable attenuators, analog meter drivers, programmable power supplies, CRT display drivers and high speed modems.

EQUIVALENT CIRCUIT



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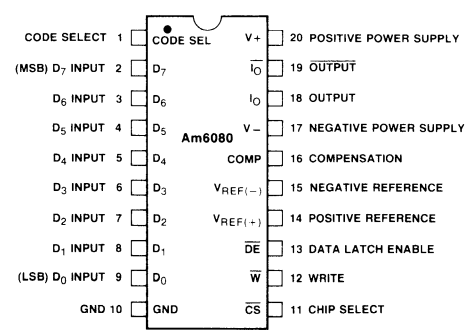
CONNECTION DIAGRAM
Top View



Pin 1 marked for orientation.

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ORDERING INFORMATION

Package Type	Temperature Range	Nonlinearity	Order Number
Hermetic DIP	−55°C to +125°C	.1%	Am6080ADM
		.19%	Am6080DM
Hermetic DIP	0°C to +70°C	.1%	Am6080ADC
		.19%	Am6080DC
Molded DIP		.1%	Am6080APC
		.19%	Am6080PC

MAXIMUM RATINGS

Operating Temperature		Power Supply Voltage	±18V
Am6080ADM, Am6080DM	−55°C to +125°C	Logic Inputs	−5V to +18V
Am6080ADC, Am6080DC Am6080APC, Am6080PC	0°C to +70°C	Analog Current Outputs	−12V to +18V
		Reference Inputs ($V_{14}V_{15}$)	V− to V+
Storage Temperature	−65°C to +150°C	Reference Input Differential Voltage (V_{14} to V_{15})	±18V
Lead Temperature (Soldering, 60 sec)	300°C	Reference Input Current (I_{14})	1.25mA

ELECTRICAL CHARACTERISTICS

These specifications apply for $V_+ = +5V$, $V_- = -15V$, $I_{REF} = 0.5mA$, over the operating temperature range unless otherwise specified. Output characteristics refer to all outputs.

				Am6080A			Am6080			
Parameter	**Description**		**Conditions**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
	Resolution			8	8	8	8	8	8	bits
	Monotonicity			8	8	8	8	8	8	bits
D.N.L.	Differential Nonlinearity			–	–	±0.19	–	–	±0.39	%FS
N.L.	Nonlinearity			–	–	±0.1	–	–	±0.19	%FS
I_{FS}	Full Scale Current		$V_{REF} = 10.000V$ $R_{14} = R_{15} = 20.000k\Omega$ $T_A = 25°C$	1.984	1.992	2.000	1.976	1.992	2.008	mA
TCI_{FS}	Full Scale Tempco			–	±5	±20	–	±10	±40	ppm/°C
				–	.0005	±.002	–	.001	±.004	%FS/°C
V_{OC}	Output Voltage Compliance			−10	–	+18	−10	–	+18	Volts
I_{FSS}	Full Scale Symmetry		$I_{FS1} - \overline{I_{FS1}}$	–	±0.1	±1.0	–	±0.2	±2.0	μA
I_{ZS}	Zero Scale Current			–	0.01	0.4	–	0.01	0.8	μA
I_{RR}	Reference Current Range		V− = −5V	0	0.5	0.55	0	0.5	0.55	mA
			V− = −15V	0	0.5	1.1	0	0.5	1.1	
V_{IL}	Logic Input Levels	Logic "0"		–	–	0.8	–	–	0.8	Volts
V_{IH}		Logic "1"		2.0	–	–	2.0	–	–	
I_{IN}	Logic Input Current		V_{IN} = −5V to +18V	–	–	40	–	–	40	μA
V_{IS}	Logic Input Swing		V− = −15V	−5	–	+18	−5	–	+18	Volts
I_{15}	Reference Bias Current			–	−0.5	−2.0	–	−0.5	−2.0	μA
dI/dt	Reference Input Slew Rate		$R_{14(EQ)} = 800\Omega$ CC = 0pF	4.0	8.0	–	4.0	8.0	–	mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity		V+ = +4.5V to +5.5V, V− = −15V	–	±0.0003	±0.01	–	±0.0005	±0.01	%FS
$PSSI_{FS-}$			V− = −13.5V to − 16.5V, V+ = +5V	–	±0.0005	±0.01	–	±0.0005	±0.01	
V+	Power Supply Range		$I_{REF} = 0.5mA$, $V_{OUT} = 0V$	4.5	–	18	4.5	–	18	Volts
V−				−18	–	−4.5	−18	–	−4.5	
I+	Power Supply Current		V+ = +5V, V− = −5V	–	9.8	14.7	–	9.8	14.7	mA
I−				–	−7.4	−9.9	–	−7.4	−9.9	
I+			V+ = +5V, V− = −15V	–	9.8	14.7	–	9.8	14.7	
I−				–	−7.4	−9.9	–	−7.4	−9.9	
I+			V+ = +15V, V− = −15V		9.8	14.7	–	9.8	14.7	
I−				–	−7.4	−9.9	–	−7.4	−9.9	
P_D	Power Dissipation		V+ = +5V, V− = −5V	–	86	123	–	86	123	mW
			V+ = +5V, V− = −15V	–	160	222	–	160	222	
			V+ = +15V, V− = −15V	–	258	369	–	258	369	

Am6080 FUNCTIONAL PIN DESCRIPTION

Symbol	Function
D_0-D_7	D_0-D_7 are the input bits 1-8 to the input data latch. Data is transferred to the data latch when $\overline{CS}$, $\overline{DE}$, and $\overline{W}$ are active and is latched when any of the enable signals go inactive.
$\overline{CS}$	Chip Select – This active low input signal enables the Am6080. Writing into the data latch occurs only when the device is selected.
$\overline{W}$	Write – This active low control signal enables the data latch when the $\overline{CS}$ and $\overline{DE}$ inputs are active.
$\overline{DE}$	Data Latch Enable – This active low input is used to enable the data latch. The $\overline{CS}$, $\overline{DE}$, and $\overline{W}$ must be active in order to write into the data latch.
CODE SEL	Code Select – When CODE SEL = 0, the MSB (D_7) is inverted and 1 LSB balance current is added to the $\overline{I_O}$ output.
$V_{REF(+)}$ $V_{REF(-)}$	Positive and negative reference voltage to the reference bias amplifier. These differential inputs allow the use of positive, negative and bipolar references.
COMP	Compensation – Frequency compensating terminal for the reference amplifier.
I_O, $\overline{I_O}$	These are high impedance complementary current outputs. The sum of these currents is always equal to I_{FS}

FUNCTION TABLES

DATA LATCH CONTROL

$\overline{CS}$	$\overline{W}$	$\overline{DE}$	Data Latch
0	0	0	Transparent
X	X	1	Latched
X	1	X	Latched
1	X	X	Latched

X = Don't Care

CODE SELECT

CODE SEL	Function
0	MSB Inverted (Note 1)
1	MSB Non-inverted

Note 1. LSB balance current is added to the $\overline{I_O}$ output.

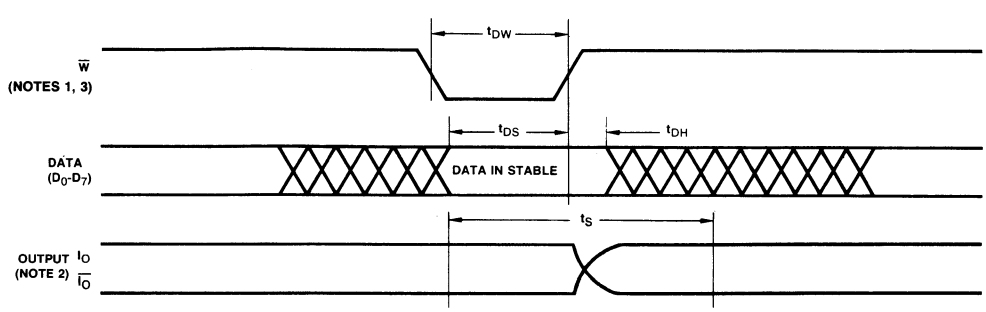
AC CHARACTERISTICS

$V_+ = +5V$, $V_- = -15V$, $I_{REF} = 0.5mA$, $R_L < 500\Omega$, $C_L < 15pF$ over the operating temperature range unless otherwise specified

Parameter	Description		Conditions	Commercial Temp. Grades Min.	Typ.	Max.	Military Temp. Grades Min.	Typ.	Max.	Unit
t_S	Settling Time, All Bits Switched		$T_A = 25°C$ Settling to ±½LSB		160			160		ns
t_{PLH}	Propagation Delay	Each bit	$T_A = 25°C$ 50% to 50%		80	160		80	160	ns
t_{PHL}		All bits switched			80	160		80	160	
t_{DH}	Data Hold Time		See timing diagram	10	−30		10	−30		ns
t_{DS}	Data Set Up Time		See timing diagram	80	35		100	35		ns
t_{DW}	Data Write Time		See timing diagram	80	35		100	35		ns

Notes: 1. t_{DW} is the overlap of $\overline{W}$ low, $\overline{CS}$ low, and $\overline{DE}$ low. All three signals must be low to enable the latch. Any signal going inactive latches the data.
2. t_S is measured with the latches open from the time the data becomes stable on the inputs to the time when the outputs are settled to within ±1/2 LSB. All bits switched on or off.
3. The internal time delays from $\overline{CS}$, $\overline{W}$ and $\overline{DE}$ inputs to the enabling of the latches are all equal.

TIMING DIAGRAM



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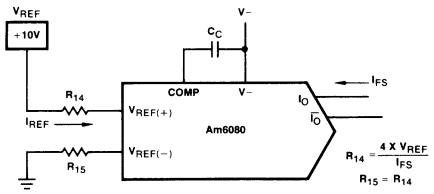
APPLICATION HINTS:

1. Reference current and reference resistor.

There is a 1 to 4 scale up between the reference current (I_{REF}) and the full scale output current (I_{FS}). If $V_{REF} = +10V$ and $I_{FS} = 2mA$, the value of the R_{14} is:

$$R_{14} = \frac{4 \times 10\ Volt}{2mA} = 20K\Omega$$



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2. Reference amplifier compensation.

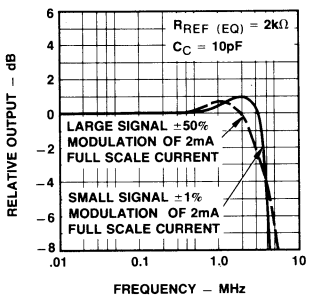
For AC reference applications, a minimum value compensation capacitor (C_C) is normally used. The value of this capacitor depends on R_{15}. The minimum values to maximize bandwidth without oscillation are as follows:

Table 2
Compensation Capacitor
(I_{FS} = 2mA, I_{REF} = 0.5mA)

R_{REF} (kΩ)	C_C (pF)
10	50
5	25
2	10
1	5
.5	0

A 0.01μF capacitor is recommended for the fixed reference operation.

Reference Amplifier Frequency Response



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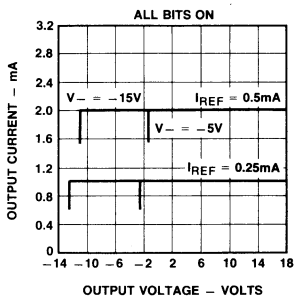
Output Voltage Compliance



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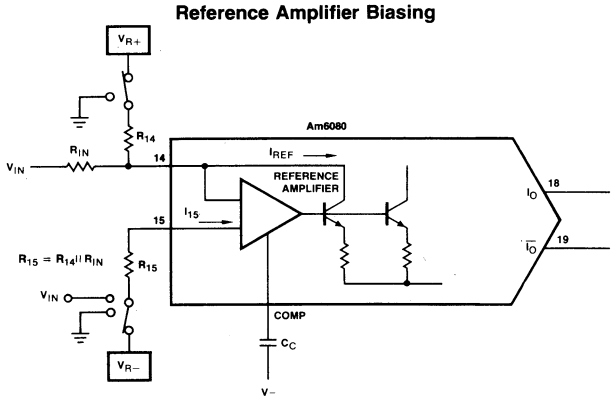
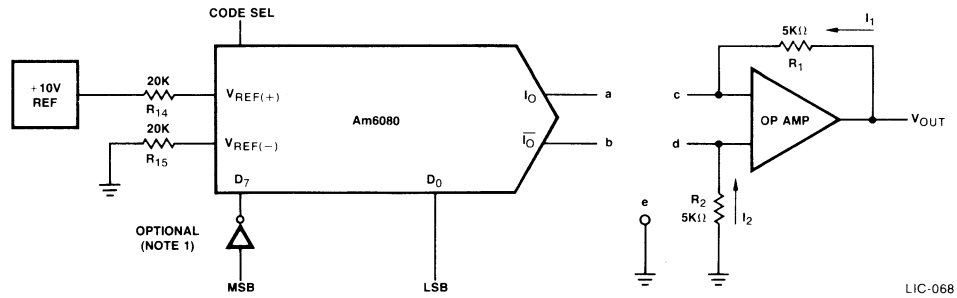
Reference Amplifier Biasing



Reference Configuration	R_{14}	R_{15}	R_{IN}	C_C	I_{REF}
Positive Reference	V_{R+}	0V	N/C	.01μF	V_{R+}/R_{14}
Negative Reference	0V	V_{R-}	N/C	.01μF	$-V_{R-}/R_{14}$
Lo Impedance Bipolar Reference	V_{R+}	0V	V_{IN}	(Note 1)	$(V_{R+}/R_{14}) + (V_{IN}/R_{IN})$ (Note 2)
Hi Impedance Bipolar Reference	V_{R+}	V_{IN}	N/C	(Note 1)	$(V_{R+} - V_{IN})/R_{14}$ (Note 3)
Pulsed Reference (Note 4)	V_{R+}	0V	V_{IN}	No Cap	$(V_{R+}/R_{14}) + (V_{IN}/R_{IN})$

Notes:
1. The compensation capacitor is a function of the impedance seen at the $+V_{REF}$ input and must be at least C = 5pFX $R_{14(eq)}$ in kΩ. For $R_{14} < 800\Omega$ no capacitor is necessary.
2. For negative values of V_{IN}, V_{R+}/R_{14} must be greater than $-V_{IN}$ Max/R_{IN} so that the amplifier is not turned off.
3. For positive values of V_{IN}, V_{R+} must be greater than V_{IN} Max so the amplifier is not turned off.
4. For pulsed operation, V_{R+} provides a DC offset and may be set to zero in some cases. The impedance at pin 14 should be 800Ω or less and an additional resistor may be connected from pin 14 to ground to lower the impedance.



CODE FORMAT		CODE SEL	CONNECTIONS	OUTPUT SCALE	OUT SEL	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	I_1 (mA)	I_2 (mA)	V_{OUT}
UNIPOLAR	Straight binary: one polarity with true input code, true zero output.	1	a-c b-e	Positive full scale	X	1	1	1	1	1	1	1	1	1.992	0	9.960
				Positive full scale − LSB	X	1	1	1	1	1	1	1	0	1.984	0	9.920
				Zero scale	X	0	0	0	0	0	0	0	0	.000	0	.000
	Complementary binary: one polarity with complementary input code, true zero output.	1	a-e b-c	Positive full scale	X	0	0	0	0	0	0	0	0	1.992	0	9.960
				Positive full scale − LSB	X	0	0	0	0	0	0	0	1	1.984	0	9.920
				Zero scale	X	1	1	1	1	1	1	1	1	.000	0	.000
SYMMETRICAL OFFSET	Straight offset binary: offset half scale, symmetrical about zero, no true zero output.	1	a-c b-d	Positive full scale	X	1	1	1	1	1	1	1	1	1.992	.000	9.960
				Positive full scale − LSB	X	1	1	1	1	1	1	1	0	1.984	.008	9.880
				(+) Zero scale	X	1	0	0	0	0	0	0	0	1.000	.992	.040
				(−) Zero scale	X	0	1	1	1	1	1	1	1	.992	1.000	−.040
				Negative full scale − LSB	X	0	0	0	0	0	0	0	1	.008	1.984	−9.880
				Negative full scale	X	0	0	0	0	0	0	0	0	.000	1.992	−9.960
	1's complement: offset half scale, symmetrical about zero, no true zero output MSB complemented. (need inverter at D_7)	1 (Note 1)	a-c b-d	Positive full scale	X	0	1	1	1	1	1	1	1	1.992	.000	9.960
				Positive full scale − LSB	X	0	1	1	1	1	1	1	0	1.984	.008	9.980
				(+) Zero scale	X	0	0	0	0	0	0	0	0	1.000	.992	.040
				(−) Zero scale	X	1	1	1	1	1	1	1	1	.992	1.000	−.040
				Negative full scale − LSB	X	1	0	0	0	0	0	0	1	.008	1.984	−9.880
				Negative full scale	X	1	0	0	0	0	0	0	0	.000	1.992	−9.960
OFFSET WITH TRUE ZERO	Offset binary: offset half scale, true zero output MSB complemented remainder add to I_O. (need inverter at D_7)	0 (Note 1)	a-c b-d	Positive full scale	X	1	1	1	1	1	1	1	1	1.992	.008	9.920
				Positive full scale − LSB	X	1	1	1	1	1	1	1	0	1.984	.016	9.840
				+ LSB	X	1	0	0	0	0	0	0	1	1.008	.992	.080
				Zero scale	X	1	0	0	0	0	0	0	0	1.000	1.000	.000
				− LSB	X	0	1	1	1	1	1	1	1	1.992	1.008	−.080
				Negative full scale + LSB	X	0	0	0	0	0	0	0	1	.008	1.992	−9.920
				Negative full scale	X	0	0	0	0	0	0	0	0	.000	2.000	−10.000
	2's complement: offset half scale true zero output MSB complemented.	0	a-c b-d	Positive full scale	X	0	1	1	1	1	1	1	1	1.992	.008	9.920
				Positive full scale − LSB	X	0	1	1	1	1	1	1	0	1.984	.016	9.840
				+1 LSB	X	0	0	0	0	0	0	0	1	1.008	.992	.080
				Zero scale	X	0	0	0	0	0	0	0	0	1.000	1.000	.000
				−1 LSB	X	1	1	1	1	1	1	1	1	.992	1.008	−.080
				Negative full scale + LSB	X	1	0	0	0	0	0	0	1	.008	1.992	−9.920
				Negative full scale	X	1	0	0	0	0	0	0	0	.000	2.000	−10.000

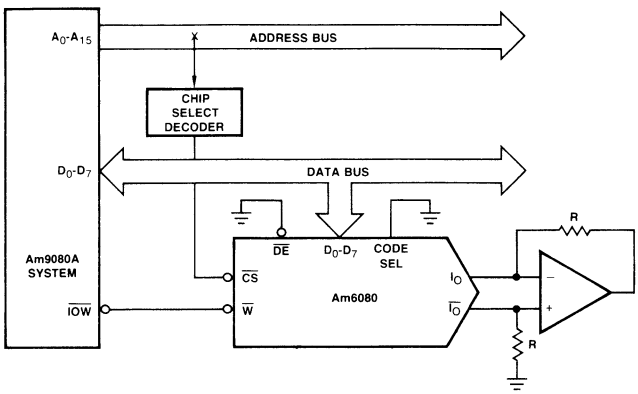
Note 1: An external inverter is necessary since the code select inverts the MSB and adds a 1 LSB balance current to $\overline{I_O}$. Only one of these features is desired for this code.

ADDITIONAL CODE MODIFICATIONS

1. Any of the offset binary codes may be complemented by reversing the output terminal pair.

SYSTEM APPLICATIONS

Am9080A DATA SYSTEM

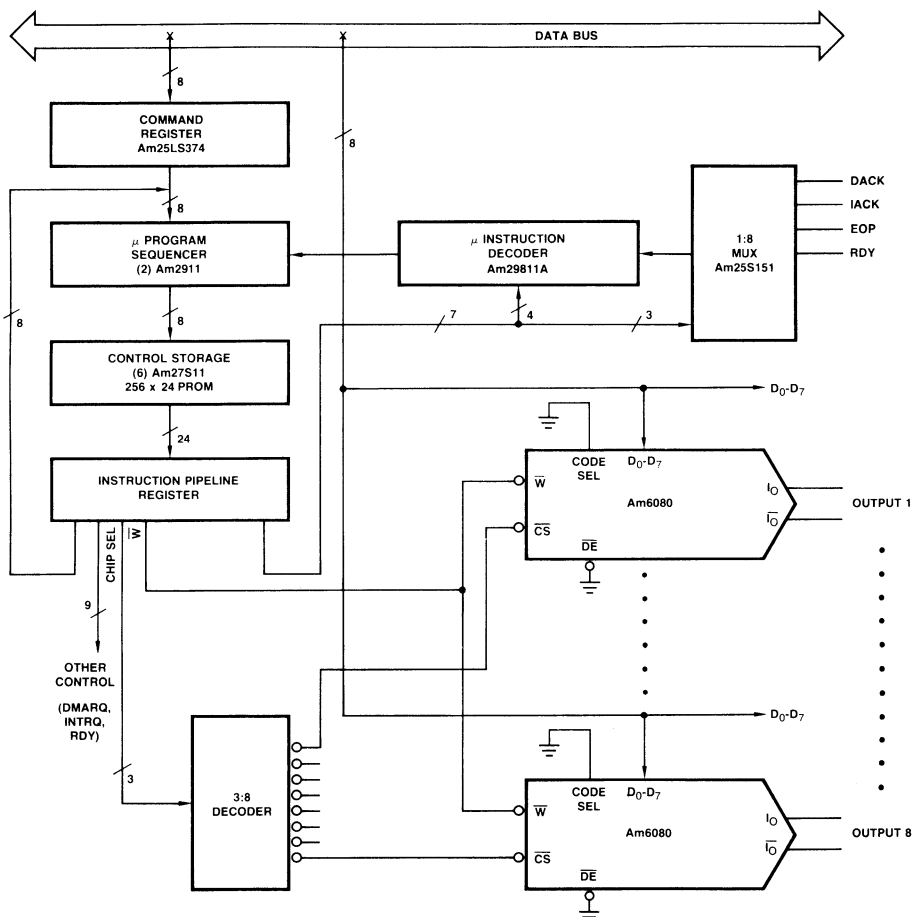


WRITING DATA INTO THE Am6080 (2's Complement)

```
PORT 1          :EQU OOH OUTPUT PORT ADDRESS
MOV A, M        :GET DATA FROM MEMORY
OUT 0 PORT1     :SEND DATA
```

LIC-069

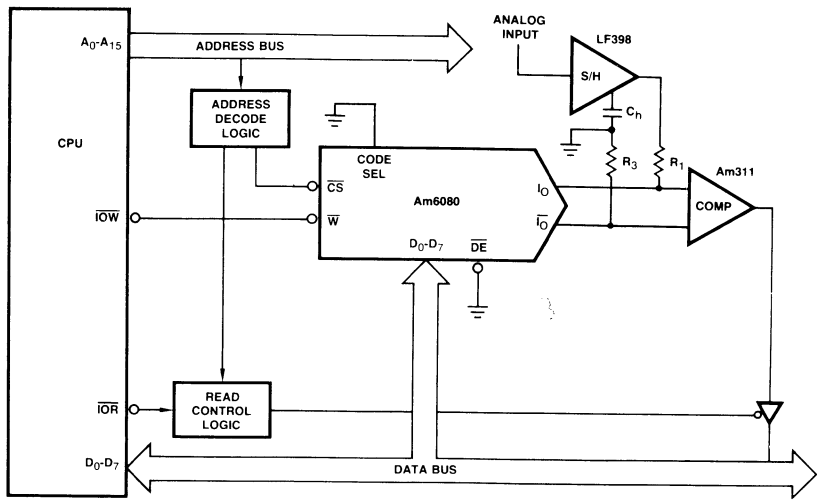
Am2900 DATA SYSTEM: MULTIPLE ANALOG INPUTS



LIC-070

SYSTEM APPLICATIONS (Cont.)

ANALOG/DIGITAL CONVERTER UNDER SOFTWARE CONTROL



LIC-071

Am9080A SOFTWARE FOR A/D CONVERSION USING Am6080.

```
SEQ     SOURCE STATEMENT
 0 PORT1    EQU 00H         ;6080 A/O PORT ADDRESS
 1 PORT3    EQU 02H         ;COMPARATOR ADDRESS
 2          ORG 3E50H
 3 START:   LXI SP,STAKS-16 ;INITIAL STAKS POINTER
 4 SAMPLE:  CALL ADCON      ;CALL A/D CONVERSATION
 5          JMP SAMPLE      ;NEXT SAMPLE
 6 ADCON:   XRA A           ;CLEAR ACC
 7          MOV D,A         ;CLEAR D REG
 8          STC             ;SET CARRY
 9          RAR             ;SET BIT 7 TO 1
10          MOV B,A         ;STORE TEST BIT AT B REGISTER
11 LOOP:    MOV E,A         ;STORE TEST WORD
12          OUT PORT1       ;OUTPUT TO A/D
```

```
SEQ     SOURCE STATEMENT
13          IN PORT3        ;INPUT FROM COMP
14          CRA A           ;SET SIGN FLAG
15          JM NEXT         ;IF SMALLER GO TO NEXT BIT
16          MOV D,E         ;SAVE RESULT
17 NEXT:    MOV A,B         ;GET NEXT TRIAL BIT
18          RAR             ;SHIFT RIGHT ONCE
19          RC              ;RETURN ON CARRY
20          MOV B,A         ;STORE TEST BIT
21          ADD D           ;ACCUMULATE RESULT
22          JMP LOOP        ;TRY NEXT BIT
23 STAKS:   DS 16
24          END START
```

APPLICATIONS

Instrumentation and Control

Data Acquisition
Data Distribution
Function Generation
Servo Controls
Programmable Power Supplies
Digital Zero Scale Calibration
Digital Full Scale Calibration
Digitally Controlled Offset Null

Signal Processing

CRT Displays
IF Gain Control
8 x 8 Digital Multiplication
Line Driver

A/D Converters

Ratiometric ADC
Differential Input ADC
Microprocessor Controlled ADC

Audio

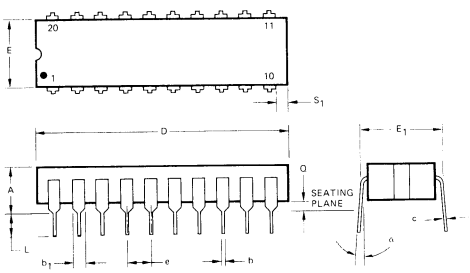
Music Distribution
Digitally Controlled Gain
Potentiometer Replacement
Digital Recording
Speech Digitizing

D/A Converters

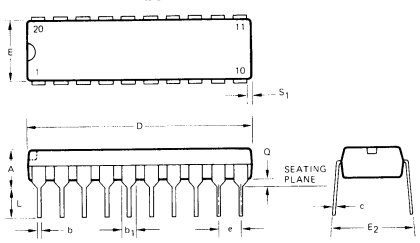
Single Quadrant Multiplying DAC
Two Quadrant Multiplying DAC
Four Quadrant Multiplying DAC

PHYSICAL DIMENSIONS
Dual-In-Line

20-Pin Hermetic



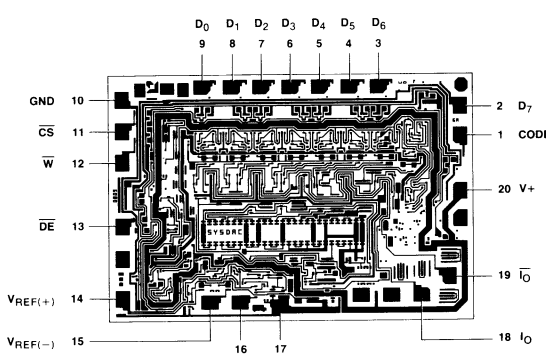
20-Pin Molded



Reference Symbol	Hermetic DIP		Plastic DIP	
	Min.	Max.	Min.	Max.
A	.140	.220	.150	.200
b	.016	.020	.015	.020
b_1	.050	.070	.055	.065
c	.009	.011	.009	.011
D	.935	.970	1.000	1.040
E	.245	.285	.250	.290
E_1	.290	.320	.310	.385
e	.090	.110	.090	.110
L	.125	.150	.125	.150
Q	.015	.045	.015	.060
S*	.005		.025	.035
α	3°	13°		

*From edge of end lead.
All dimensions in inches.

Metallization and Pad Layout



DIE SIZE
0.085" X 0.124"

Am6081

Microprocessor System Compatible 8-Bit High Speed Multiplying D/A Converter

DISTINCTIVE CHARACTERISTICS

- 8-Bit D/A with 8-Bit input data latch
- Compatible with most popular microprocessors including the Am9080A-4 and the Am2900
- Write, Chip Select and Data Enable logic on chip
- DAC appears as memory location to microprocessor
- MSB inversion under logic control
- Differential current outputs
- Output current mode multiplexer with logic selection
- 2-Bit status latch for output select and code select
- Choice of 8 coding formats
- Fast settling current output – 200ns
- Nonlinearity to ±0.1% max over temperature range
- Full scale current pre-matched to ±1 LSB
- High output impedance and voltage compliance
- Low full scale current drift – ±5ppm/°C
- Wide range multiplying capability –2.0MHz bandwidth
- Direct interface to TTL, CMOS, NMOS
- Output range selection with on chip multiplexer
- High speed data latch – 80ns min write time

GENERAL DESCRIPTION

The Am6081 is a monolithic 8-bit multiplying Digital-to-Analog converter with an 8-bit data latch, a 2-bit status latch, chip select and other control signal lines which allow direct interface with microprocessor buses.

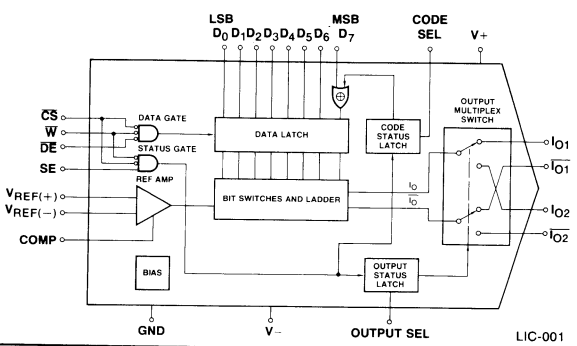
The converter allows a choice of 8 different coding formats. The most significant bit (D_7) can be inverted or non-inverted under the control of the code select input. The code control also provides a zero differential current output for 2's complement coding. A pair of high voltage compliance, dual complementary current output channels is provided and is selected by the output status command. The output multiplexer also allows analog bus connection of several converters, range or output load selection, and time-shared operation between D/A and A/D functions. The data and status latches are high speed which makes the Am6081 capable of interfacing with high speed microprocessors. The DE and SE control signals allow the data and status latches to be updated individually or simultaneously.

Monotonic multiplying performance is maintained over a more than 40 to 1 reference current range. Matching within ±1 LSB between reference and full scale current eliminates the need for full scale trimming in most applications.

The Am6081 guarantees full 8-bit monotonicity. Nonlinearities as tight as 0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the full power supply voltage and temperature range.

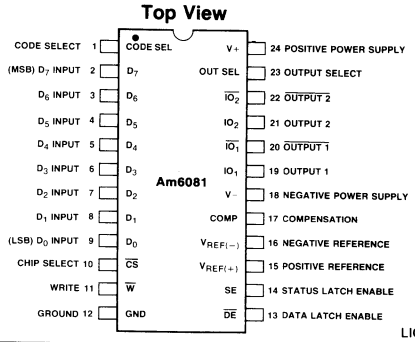
Applications for the Am6081 include microprocessor compatible data acquisition systems and data distribution systems, 8-bit A/D converters, servo-motor and pen drivers, waveform generators, programmable attenuators, analog meter drivers, programmable power supplies, CRT display drivers and high speed modems.

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM

Top View



LIC-002

ORDERING INFORMATION

Package Type	Temperature Range	Nonlinearity	Order Number
Hermetic DIP	–55°C to +125°C	±.1% ±.19%	AM6081ADM AM6081DM
Hermetic DIP	0°C to +70°C	±.1% ±.19%	AM6081ADC AM6081DC
Molded DIP	0°C to +70°C	±.1% ±.19%	AM6081APC AM6081PC

Am6081 FUNCTIONAL PIN DESCRIPTION

Symbol **Function**

$\overline{CS}$ Chip Select – This active low input signal enables the Am6081. Writing into the data or status latches occurs only when the device is selected.

$\overline{DE}$ Data Latch Enable – This active low input is used to enable the data latch. The $\overline{CS}$, $\overline{DE}$, and $\overline{W}$ must be active in order to write into the data latch.

SE Status Latch Enable – This active high input is used to enable the status latches. The $\overline{CS}$, SE, and $\overline{W}$ must be active in order to write into the status latches.

$\overline{W}$ Write – This active low control signal enables the data and status latches when the $\overline{CS}$, $\overline{DE}$, and SE inputs are active.

D_0-D_7 D_0-D_7 are the input bits 1-8 to the input data latch. Data is transferred to the data latch when $\overline{CS}$, $\overline{DE}$, and $\overline{W}$ are active and is latched when any of the enable signals go inactive.

CODE SEL Code Select – Input to the CODE SEL latch. The latch is transparent when $\overline{CS}$, SE and $\overline{W}$ are active and is latched when any of the above signals go inactive. When CODE SEL latch = 0, the MSB (D_7) is inverted and 1 LSB balance current is added to the $\overline{I_O}$ output.

OUT SEL Output Select – Input to the OUT SEL latch. The latch is transparent when $\overline{CS}$, SE and $\overline{W}$ are active and is latched when any of the above signals go inactive. When the OUT SEL latch is low, the channel 1 output pair (I_{O1}, $\overline{I_{O1}}$) is selected. When the OUT SEL latch is high, the channel 2 output pair (I_{O2}, $\overline{I_{O2}}$) is selected.

$V_{REF(+)}$ **$V_{REF(-)}$** Positive and negative reference voltage to the reference bias amplifier. These differential inputs allow the use of positive, negative and bipolar references.

COMP Compensation – Frequency compensating terminal for the reference amplifier.

I_{O1}, $\overline{I_{O1}}$ **I_{O2}, $\overline{I_{O2}}$** These high impedance current output pairs are selected by the output select latch. I_{O1} and I_{O2} are true outputs and $\overline{I_{O1}}$ and $\overline{I_{O2}}$ are complementary outputs.

FUNCTION TABLES

DATA LATCH CONTROL

$\overline{CS}$	$\overline{W}$	$\overline{DE}$	Data Latch
0	0	0	Transparent
X	X	1	Latched
X	1	X	Latched
1	X	X	Latched

STATUS LATCH CONTROL

$\overline{CS}$	$\overline{W}$	SE	CODE SEL and OUT SEL Latch
0	0	1	Transparent
X	X	0	Latched
X	1	X	Latched
1	X	X	Latched

CODE SELECT AND OUTPUT SELECT

CODE SEL	OUT SEL	Function
0	–	MSB Inverted (Note 1)
1	–	MSB Non-inverted
–	0	Output Channel 1
–	1	Output Channel 2

X = Don't Care

Note 1. 1 LSB balance current is added to the $\overline{I_O}$ output.

MAXIMUM RATINGS

Operating Temperature		Power Supply Voltage	±18V
Am6081ADM, Am6081DM	−55°C to +125°C	Logic Inputs	−5V to +18V
Am6081ADC, Am6081DC Am6081APC, Am6081PC	0°C to +70°C	Analog Current Outputs	−12V to +18V
		Reference Inputs (V_{15}, V_{16})	V− to V+
Storage Temperature	−65°C to +150°C	Reference Input Differential Voltage (V_{15} to V_{16})	±18V
Lead Temperature (Soldering, 60 sec)	300°C	Reference Input Current (I_{15})	1.25mA

GUARANTEED FUNCTIONAL SPECIFICATIONS

Resolution	8 bits
Monotonicity	8 bits

ELECTRICAL CHARACTERISTICS

These specifications apply for $V_+ = +5V$, $V_- = -15V$, $I_{REF} = 0.5mA$, over the operating temperature range unless otherwise specified. Output characteristics refer to all outputs.

Parameter	Description	Conditions	Am6081A Min.	Am6081A Typ.	Am6081A Max.	Am6081 Min.	Am6081 Typ.	Am6081 Max.	Unit
	Resolution	Straight coding/Sign Magnitude	8/9	8/9	8/9	8/9	8/9	8/9	bits
	Monotonicity	Straight coding/Sign Magnitude	8/9	8/9	8/9	8/9	8/9	8/9	bits
D.N.L.	Differential Nonlinearity		–	–	±0.19	–	–	±0.39	%FS
N.L.	Nonlinearity		–	–	±0.1	–	–	±0.19	%FS
I_{FS}	Full Scale Current	$V_{REF} = 10.000V$ $R_{15} = R_{16} = 20.000k\Omega$ $T_A = 25°C$	1.984	1.992	2.000	1.976	1.992	2.008	mA
TCI_{FS}	Full Scale Tempco		–	±5	±20	–	±10	±40	ppm/°C
			–	±.0005	±.002		±.001	±.004	%FS/°C
V_{OC}	Output Voltage Compliance		−10	–	+18	−10	–	+18	Volts
I_{FSS}	Full Scale Symmetry	$I_{FS1} - \overline{I_{FS1}}$ or $I_{FS2} - \overline{I_{FS2}}$	–	±0.1	±1.0	–	±0.2	±2.0	μA
I_{OSS}	Output Switch Symmetry	$I_{FS1} - I_{FS2}$ or $\overline{I_{FS1}} - \overline{I_{FS2}}$	–	±0.1	±1.0	–	±0.2	±2.0	μA
I_{ZS}	Zero Scale Current		–	0.01	0.4	–	0.01	0.8	μA
I_{DIS}	Output Disable Current	Output of mpx "Off" Channels	–	0.01	0.05	–	0.01	0.05	μA
I_{RR}	Reference Current Range	V− = −5V	0	0.5	0.55	0	0.5	0.55	mA
		V− = −15V	0	0.5	1.1	0	0.5	1.1	
V_{IL}	Logic Input Levels, Logic "0"		–	–	0.8	–	–	0.8	Volts
V_{IH}	Logic Input Levels, Logic "1"		2.0	–	–	2.0	–	–	
I_{IN}	Logic Input Current	V_{IN} = −5V to +18V	–	–	40	–	–	40	μA
V_{IS}	Logic Input Swing	V− = −15V	−5	–	+18	−5	–	+18	Volts
I_{16}	Reference Bias Current		–	−0.5	−2.0	–	−0.5	−2.0	μA
dI/dt	Reference Input Slew Rate	$R_{15(EQ)} = 800\Omega$ CC = 0pF	4.0	8.0	–	4.0	8.0	–	mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity	V+ = +4.5V to +5.5V, V− = −15V	–	±0.0005	±0.01	–	±0.0005	±0.01	%FS
$PSSI_{FS-}$		V− = −13.5V to − 16.5V, V+ = +5V	–	±0.0005	±0.01	–	±0.0005	±0.01	
V+	Power Supply Range	$I_{REF} = 0.5mA$, $V_{OUT} = 0V$	4.5	–	18	4.5	–	18	Volts
V−			−18	–	−4.5	−18	–	−4.5	
I+	Power Supply Current	V+ = +5V, V− = −5V	–	9.8	14.7	–	9.8	14.7	mA
I−			–	−7.4	−9.9	–	−7.4	−9.9	
I+		V+ = +5V, V− = −15V	–	9.8	14.7	–	9.8	14.7	
I−			–	−7.4	−9.9	–	−7.4	−9.9	
I+		V+ = +15V, V− = −15V		9.8	14.7	–	9.8	14.7	
I−			–	−7.4	−9.9	–	−7.4	−9.9	
P_D	Power Dissipation	V+ = +5V, V− = −5V	–	86	123	–	86	123	mW
		V+ = +5V, V− = −15V	–	160	222	–	160	222	
		V+ = +15V, V− = −15V	–	258	369	–	258	369	

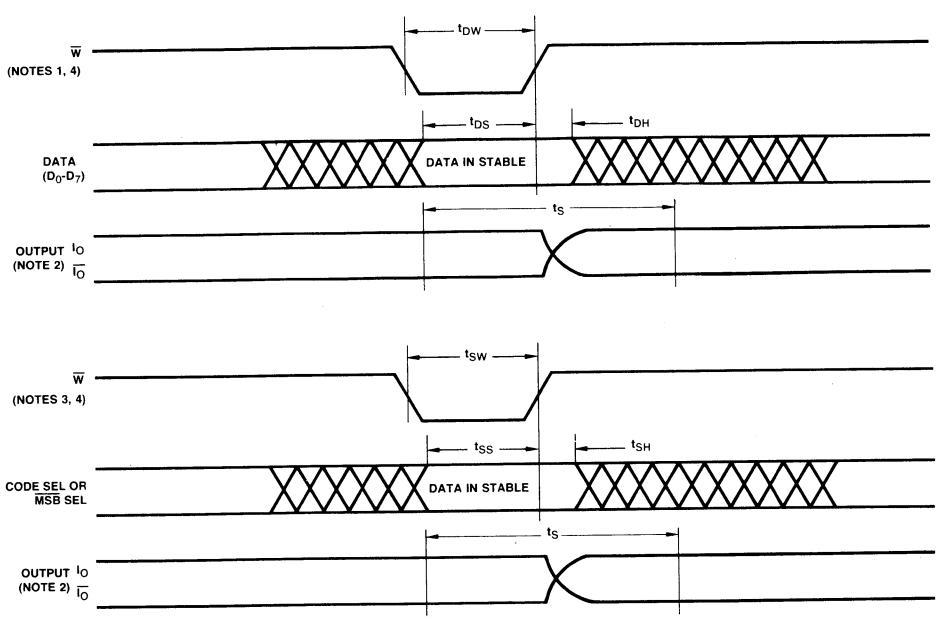
AC CHARACTERISTICS

$V_+ = +5V$, $V_- = -15V$, $I_{REF} = 0.5mA$, $R_L < 500\Omega$, $C_L < 15pF$ over the operating temperature range unless otherwise specified

Parameter	Description		Conditions	Commercial Temp. Grades Min.	Typ.	Max.	Military Temp. Grades Min.	Typ.	Max.	Unit
t_S	Settling Time, All Bits Switched		$T_A = 25°C$ Settling to ±½LSB		200			200		ns
t_{PLH}	Propagation Delay	Each bit	$T_A = 25°C$ 50% to 50%		90	180		90	180	ns
t_{PHL}		All bits switched			90	180		90	180	
t_{OS}	Output Switch Settling Time		$T_A = 25°C$ to ±1/2LSB of I_{FS}		250			250		ns
t_{OP}	Output Switch Propagation Delay		$T_A = 25°C$, 50% to 50%		150	300		150	300	ns
t_{DH}	Data Hold Time		See timing diagram	10	−30		10	−30		ns
t_{DS}	Data Set Up Time		See timing diagram	80	35		100	35		ns
t_{DW}	Data Write Time		See timing diagram	80	35		100	35		ns
t_{SH}	Status Hold Time		See timing diagram	10	−70		10	−70		ns
t_{SS}	Status Set Up Time		See timing diagram	200	100		230	100		ns
t_{SW}	Status Write Time		See timing diagram	200	100		230	100		ns

Notes:
1. t_{DW} is the overlap of $\overline{W}$ low, $\overline{CS}$ low, and $\overline{DE}$ low. All three signals must be low to enable the latch. Any signal going inactive latches the data.
2. t_S is measured with the latches open from the time the data becomes stable on the inputs to the time when the outputs are settled to within ±1/2 LSB. All bits switched on or off.
3. t_{SW} is the overlap of $\overline{W}$ low, $\overline{CS}$ low and SE high, all three signals must be active to enable the latch and any signal going inactive will latch the data.
4. The internal time delays from $\overline{CS}$, $\overline{W}$, SE and $\overline{DE}$ inputs to the enabling of the latches are all equal.

TIMING DIAGRAM



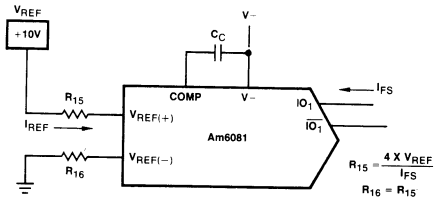
LIC-003

APPLICATION HINTS

1. Reference current and reference resistor

There is a 1 to 4 scale up between the reference current (I_{REF}) and the full scale output current (I_{FS}). If $V_{REF} = +10V$ and $I_{FS} = 2mA$, the value of the R_{15} is:

$$R_{15} = \frac{4 \times 10\ Volt}{2mA} = 20K\Omega$$



LIC-004

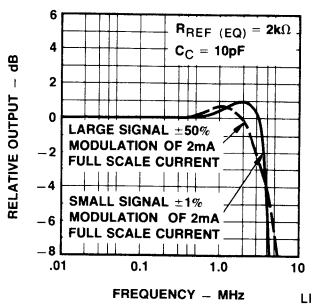
2. Reference amplifier compensation

For AC reference applications, a minimum value compensation capacitor (C_C) is normally used. The value of this capacitor depends on R_{15}. The minimum values to maximize bandwidth without oscillation are as follows:

Table 2
Compensation Capacitor
(I_{FS} = 2mA, I_{REF} = 0.5mA)

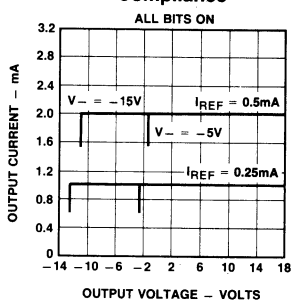
R_{REF} (kΩ)	C_C (pF)
20	100
10	50
5	25
2	10
1	5
.5	0

Reference Amplifier Frequency Response



LIC-005

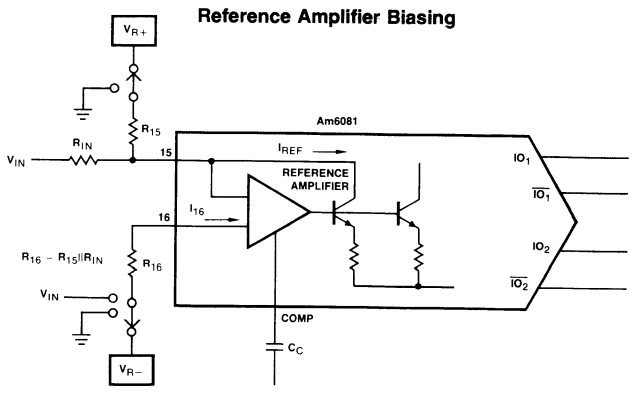
Output Voltage Compliance



LIC-006

A 0.01μF capacitor is recommended for the fixed reference operation.

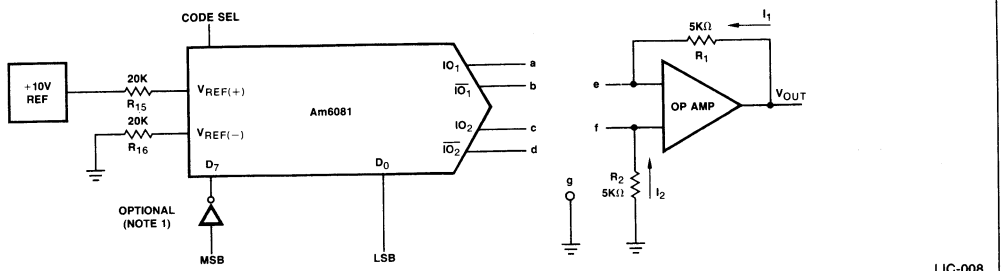
Reference Amplifier Biasing



LIC-007

Reference Configuration	R_{15}	R_{16}	R_{IN}	C_C	I_{REF}
Positive Reference	V_{R+}	0V	N/C	.01μF	V_{R+}/R_{15}
Negative Reference	0V	V_{R-}	N/C	.01μF	$-V_{R-}/R_{15}$
Lo Impedance Bipolar Reference	V_{R+}	0V	V_{IN}	(Note 1)	$(V_{R+}/R_{15}) + (V_{IN}/R_{IN})$ (Note 2)
Hi Impedance Bipolar Reference	V_{R+}	V_{IN}	N/C	(Note 1)	$(V_{R+} - V_{IN})/R_{15}$ (Note 3)
Pulsed Reference (Note 4)	V_{R+}	0V	V_{IN}	No Cap	$(V_{R+}/R_{15}) + (V_{IN}/R_{IN})$

Notes:
1. The compensation capacitor is a function of the impedance seen at the $+V_{REF}$ input and must be at least $C = 5pF \times R_{15(EQ)}$ (in kΩ). For $R_{15} < 800\Omega$ no capacitor is necessary.
2. For negative values of V_{IN}, V_{R+}/R_{15} must be greater than $-V_{IN}$ Max/R_{IN} so that the amplifier is not turned off.
3. For positive values of V_{IN}, V_{R+} must be greater than V_{IN} Max so the amplifier is not turned off.
4. For pulsed operation, V_{R+} provides a DC offset and may be set to zero in some cases. The impedance at pin 15 should be 800Ω or less and an additional resistor may be connected from pin 15 to ground to lower the impedance.



LIC-008

Note: Connect all unused outputs to ground.

CODE FORMAT		CODE SEL	OUT SEL	CON-NECTIONS	OUTPUT SCALE	OUT SEL	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	I_1 (mA)	I_2 (mA)	V_{OUT}
UNIPOLAR	Straight binary: one polarity with true input code, true zero output.	1	0	a-e b-g	Positive full scale	X	1	1	1	1	1	1	1	1	1.992	0	9.960
					Positive full scale − LSB	X	1	1	1	1	1	1	1	0	1.984	0	9.920
					Zero scale	X	0	0	0	0	0	0	0	0	.000	0	.000
			1	c-e d-g													
	Complementary binary: one polarity with complementary input code, true zero output.	1	0	a-g b-e	Positive full scale	X	0	0	0	0	0	0	0	0	1.992	0	9.960
					Positive full scale − LSB	X	0	0	0	0	0	0	0	1	1.984	0	9.920
					Zero scale	X	1	1	1	1	1	1	1	1	.000	0	.000
			1	c-g d-e													
SIGNED MAGNITUDE	Signed magnitude binary: 8 bits + sign reflected code, overlapping true zero output.	1		a-e c-f	Positive full scale	1	1	1	1	1	1	1	1	1	1.992	.000	9.960
					Positive full scale − LSB	1	1	1	1	1	1	1	1	0	1.984	.000	9.920
					(+) Zero scale	1	0	0	0	0	0	0	0	0	.000	.000	.000
					(−) Zero scale	0	0	0	0	0	0	0	0	0	.000	.000	.000
					Negative full scale − LSB	0	1	1	1	1	1	1	1	0	.000	1.984	−9.920
					Negative full scale	0	1	1	1	1	1	1	1	1	.000	1.992	−9.960
	Complementary signed magnitude: 8 bits + sign complementary reflected code, overlapping true zero output.	1		b-e d-f	Positive full scale	1	0	0	0	0	0	0	0	0	1.992	.000	9.960
					Positive full scale − LSB	1	0	0	0	0	0	0	0	1	1.984	.000	9.920
					(+) Zero scale	1	1	1	1	1	1	1	1	1	.000	.000	.000
					(−) Zero scale	0	1	1	1	1	1	1	1	1	.000	.000	.000
					Negative full scale − LSB	0	0	0	0	0	0	0	0	1	.000	1.984	−9.920
					Negative full scale	0	0	0	0	0	0	0	0	0	.000	1.992	−9.960
SYMMETRICAL OFFSET	Straight offset binary: offset half scale, symmetrical about zero, no true zero output.	1	0	a-e b-f	Positive full scale	X	1	1	1	1	1	1	1	1	1.992	.000	9.960
					Positive full scale − LSB	X	1	1	1	1	1	1	1	0	1.984	.008	9.880
					(+) Zero scale	X	1	0	0	0	0	0	0	0	1.000	.992	.040
					(−) Zero scale	X	0	1	1	1	1	1	1	1	.992	1.000	−.040
					Negative full scale − LSB	X	0	0	0	0	0	0	0	1	.008	1.984	−9.880
			1	c-e d-f	Negative full scale	X	0	0	0	0	0	0	0	0	.000	1.992	−9.960
	1's complement: offset half scale, symmetrical about zero, no true zero output MSB complemented. (need inverter at D_7)	1 (Note 1)	0	a-e b-f	Positive full scale	X	0	1	1	1	1	1	1	1	1.992	.000	9.960
					Positive full scale − LSB	X	0	1	1	1	1	1	1	0	1.984	.008	9.980
					(+) Zero scale	X	0	0	0	0	0	0	0	0	1.000	.992	.040
					(−) Zero scale	X	1	1	1	1	1	1	1	1	.992	1.000	−.040
					Negative full scale − LSB	X	1	0	0	0	0	0	0	1	.008	1.984	−9.880
			1	c-e d-f	Negative full scale	X	1	0	0	0	0	0	0	0	.000	1.992	−9.960
OFFSET WITH TRUE ZERO	Offset binary: offset half scale, true zero output MSB complemented remainder add to I_O. (need inverter at D_7)	0 (Note 1)	0	a-e b-f	Positive full scale	X	1	1	1	1	1	1	1	1	1.992	.008	9.920
					Positive full scale − LSB	X	1	1	1	1	1	1	1	0	1.984	.016	9.840
					+ LSB	X	1	0	0	0	0	0	0	1	1.008	.992	.080
					Zero scale	X	1	0	0	0	0	0	0	0	1.000	1.000	.000
					− LSB	X	0	1	1	1	1	1	1	1	1.992	1.008	−.080
					Negative full scale + LSB	X	0	0	0	0	0	0	0	1	.008	1.992	−9.920
			1	c-e d-f	Negative full scale	X	0	0	0	0	0	0	0	0	.000	2.000	−10.000
	2's complement: offset half scale true zero output MSB complemented.	0	0	a-e b-f	Positive full scale	X	0	1	1	1	1	1	1	1	1.992	.008	9.920
					Positive full scale − LSB	X	0	1	1	1	1	1	1	0	1.984	.016	9.840
					+1 LSB	X	0	0	0	0	0	0	0	1	1.008	.992	.080
					Zero scale	X	0	0	0	0	0	0	0	0	1.000	1.000	.000
					−1 LSB	X	1	1	1	1	1	1	1	1	.992	1.008	−.080
			1	c-e d-f	Negative full scale + LSB	X	1	0	0	0	0	0	0	1	.008	1.992	−9.920
					Negative full scale	X	1	0	0	0	0	0	0	0	.000	2.000	−10.000

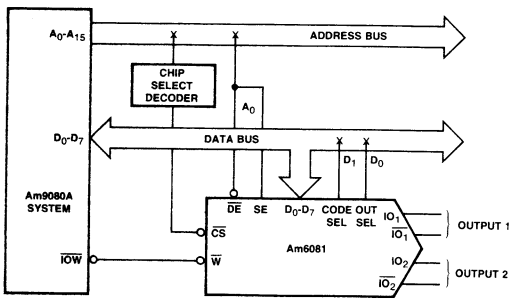
Note 1: An external inverter is necessary since the code select inverts the MSB and adds a 1 LSB balance current to $\overline{I_O}$. Only one of the two features is desired for these codes.

ADDITIONAL CODE MODIFICATIONS

1. Any of the offset binary codes may be complemented by reversing the output terminal pair.
2. The sign on any of the sign-magnitude codes may be changed by reversing the output terminal pair.
3. The polarity of the unipolar codes may be changed by driving the opposite side of the balanced load.

SYSTEM APPLICATIONS

Am9080A DATA SYSTEM: SEPARATE UPDATE OF DATA AND STATUS



SELECT OUTPUT PORT 1

```
MVI A, 2    : SET STATUS TO 0 (SELECT OUTPUT 1)
OUT 1       : SEND STATUS
MOV A, M    : GET DATA FROM MEMORY
OUT 0       : SEND DATA
```

SELECT OUTPUT PORT 2

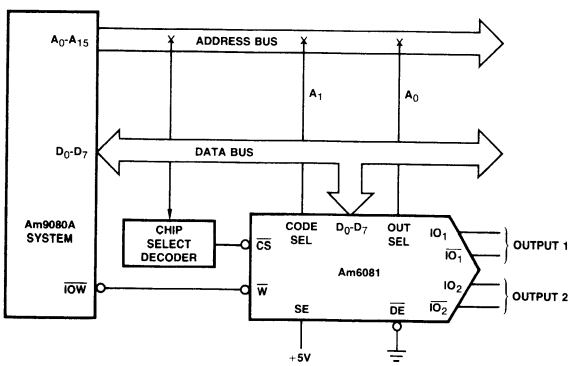
```
MVI A, 3    : SET STATUS TO 1 (SELECT OUTPUT 2)
OUT 1       : SEND STATUS
MOV A,M     : GET DATA FROM MEMORY
OUT 0       : SEND DATA
```

SELECT OUTPUT PORT 2 AND 2's COMPLEMENT CODE

```
MVI A, 1    : SET STATUS TO 3 (OUTPUT 2, MSB COMP)
OUT 1       : SEND STATUS
MOV A, M    : GET DATA FROM MEMORY
OUT 0       : SEND DATA
```

LIC-009

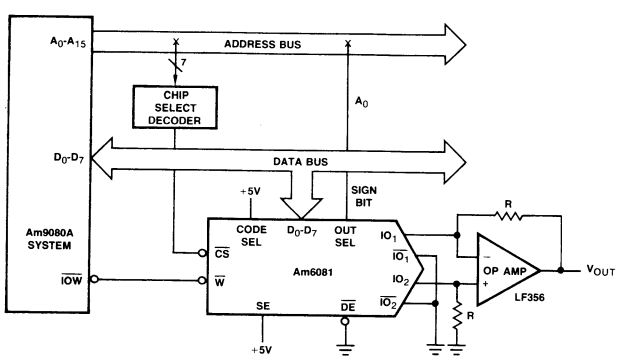
Am9080A DATA SYSTEM: SIMULTANEOUS UPDATE OF DATA AND STATUS




```
MOV A, M    : GET DATA IN ACCUMULATOR
OUT 0       : OUTPUT DATA TO PORT 1, 2'S COMPLEMENT
OUT 1       : OUTPUT DATA TO PORT 2, 2'S COMPLEMENT
OUT 2       : OUTPUT DATA TO PORT 1, STRAIGHT BINARY
OUT 3       : OUTPUT DATA TO PORT 2, STRAIGHT BINARY
```

LIC-010

Am9080A DATA SYSTEM: 8-BIT PLUS SIGN CONVERSION

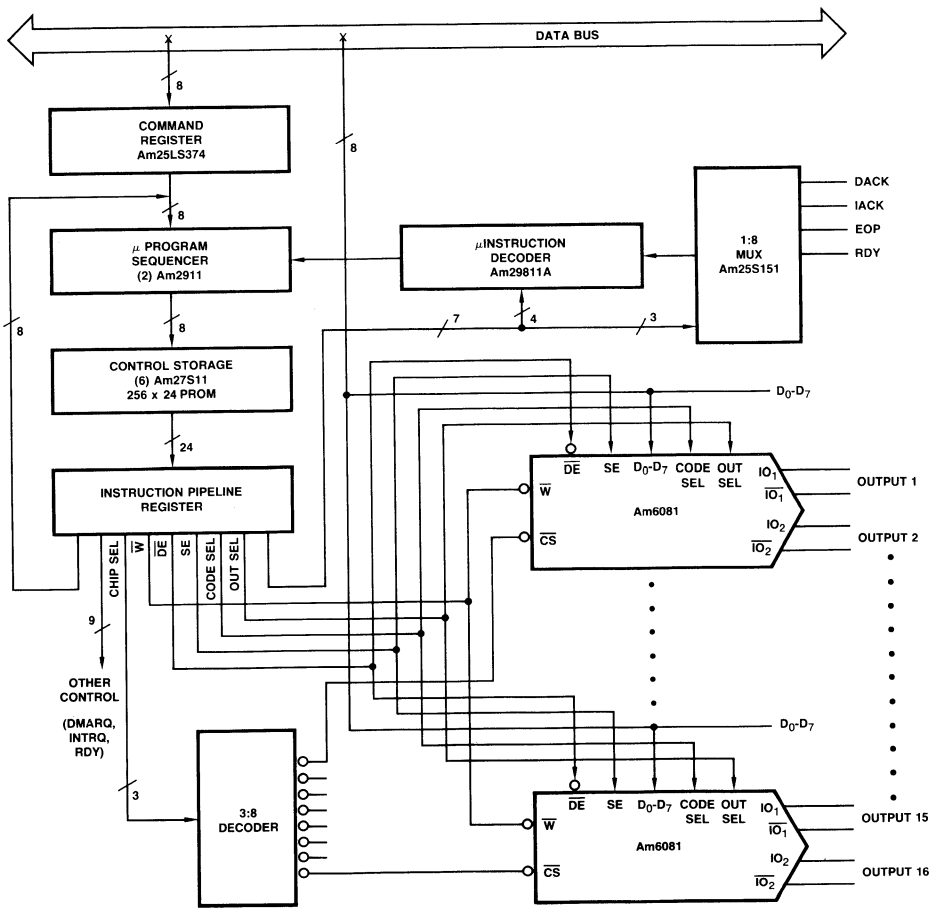



```
MOV A, M    : LOAD MAGNITUDE (8-BITS)
OUT 0       : SEND POSITIVE OUTPUT
OUT 1       : SEND NEGATIVE OUTPUT
```

LIC-011

SYSTEM APPLICATIONS (Cont.)

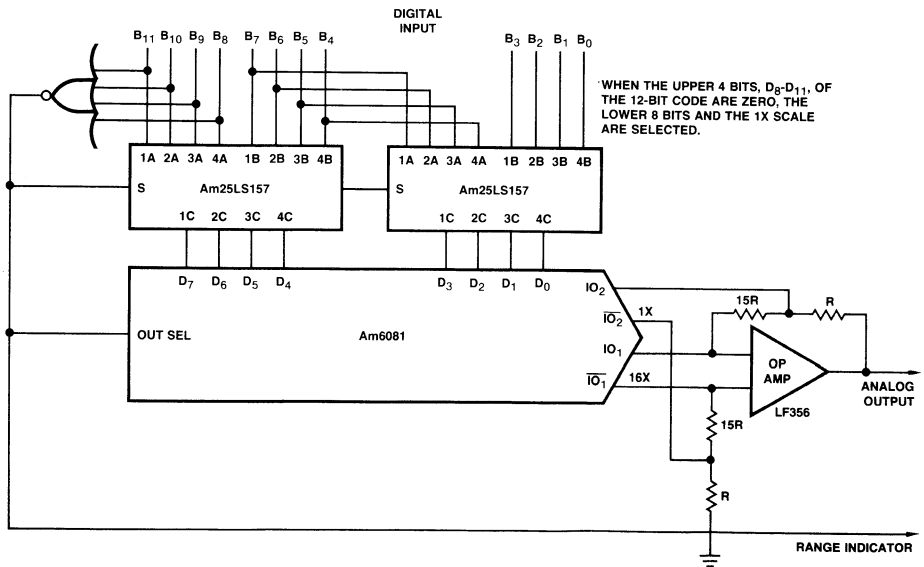
Am2900 DATA SYSTEM: MULTIPLE ANALOG OUTPUTS



LIC-012

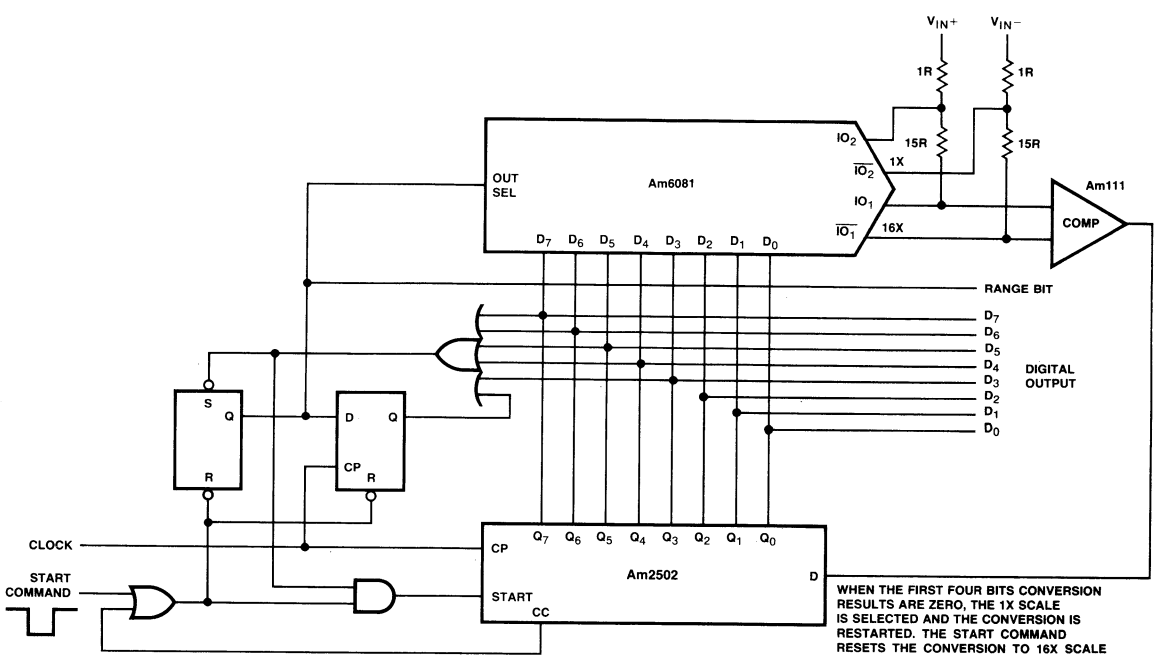
SYSTEM APPLICATIONS (Cont.)

D/A CONVERSION WITH 12-BIT DYNAMIC RANGE



LIC-013

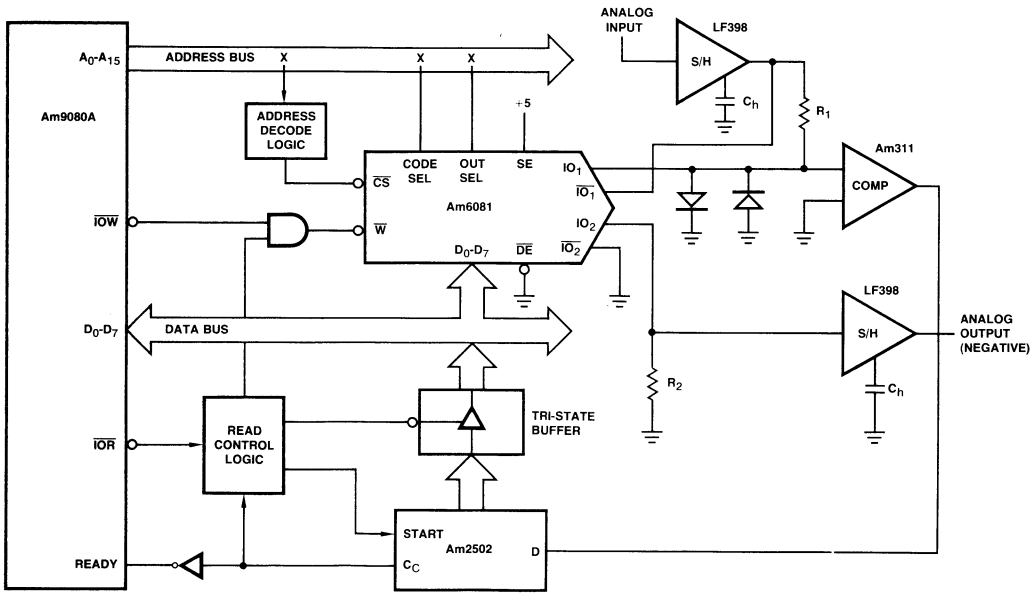
A/D CONVERSION WITH AUTO RANGING AND DIFFERENTIAL INPUT



LIC-014

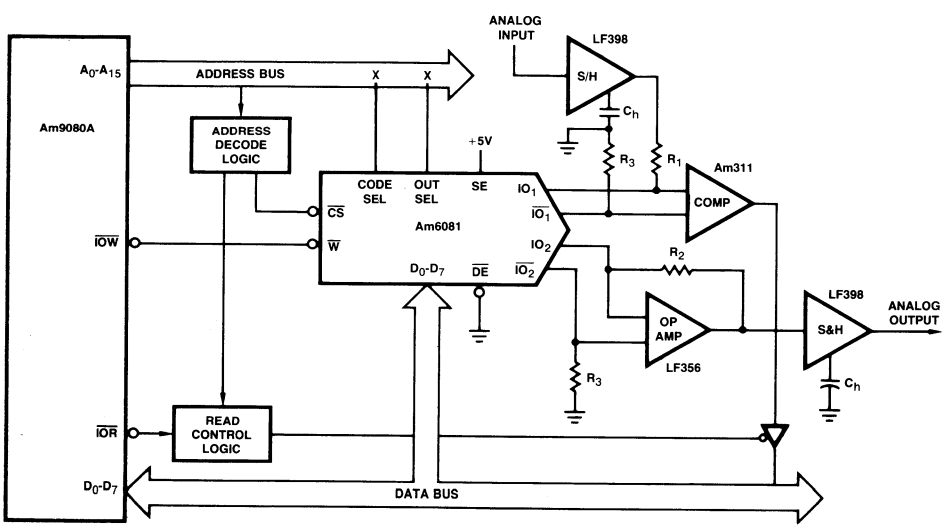
SYSTEM APPLICATIONS (Cont.)

ANALOG/DIGITAL TRANSCEIVER WITH HARDWARE CONTROLLED SUCCESSIVE APPROXIMATION A/D CONVERSION



LIC-015

ANALOG/DIGITAL TRANSCEIVER WITH SOFTWARE CONTROLLED A/D CONVERSION



LIC-016

Am9080A SOFTWARE FOR A/D AND D/A CONVERSION USING Am6081

```
SEQ     SOURCE STATEMENT
 0 PORT1   EQU 00H
 1 PORT3   EQU 02H
 2 PORT2   EQU 01H
 3         ORG 3E50H
 4 START:  LXI SP,STAKS-16   ;INITIAL STAKS POINTER
 5 SAMPLE: CALL ADCON        ;CALL A/D CONVERSATION
 6         CMA
 7         CALL DACON        ;CALL D/A CONVERSION
 8         JMP SAMPLE        ;NEXT SAMPLE
 9 ADCON:  XRA A             :CLEAR ACC
10         MOV D,A           ;CLEAR D REG
11         STC               ;SET CARRY
12         RAR               ;SET BIT 7 TO 1
13         MOV B,A           ;STORE TEST BIT AT B REGISTER
14 LOOP:   MOV E,A           ;STORE TEST WORD
15         CMA
16         OUT PORT1         ;OUTPUT TO A/D
17         IN PORT3          ;INPUT FROM COMP

SEQ     SOURCE STATEMENT
18         CMA
19         CRA A             ;SET SIGN FLAG
20         JM NEXT           ;IF SMALLER GO TO NEXT BIT
21         MOV D,E           ;SAVE RESULT
22 NEXT:   MOV A,B           ;GET NEXT TRIAL BIT
23         RAR               ;SHIFT RIGHT ONCE
24         RC                ;RETURN ON CARRY
25         MOV B,A           ;STORE TEST BIT
26         ADD D             ;ACCUMULATE RESULT
27         JMP LOOP          ;TRY NEXT BIT
28 DACON:  OUT PORT 2        ;OUTPUT TO D/A
29         MVI C,05H         ;LOAD C REG WITH TIME
30         DCR C             ;TIME DELAY
31         RZ                ;RETURN
32 FILT:   RET
33 STAKS:  DS 16
34         END START
```

ADVANCED MICRO DEVICES DATA CONVERSION PRODUCTS

Digital to Analog Converters

AmDAC-08	– 8-Bit High Speed Multiplying D/A Converter
Am1508/1408	– 8-Bit Multiplying D/A Converter
Am6070	– 8-Bit Companding D/A Converter for Control Systems (μ-law)
Am6071	– 8-Bit Companding D/A Converter for Control Systems (A-law)
Am6072	– 8-Bit Companding D/A Converter for Telecommunications (μ-law)
Am6073	– 8-Bit Companding D/A Converter for Telecommunicatons (A-law)
Am6080	– 8-Bit High Speed Multiplying D/A Converter System/Microprocessor Compatible
Am6081	– 8-Bit High Speed Multiplying D/A Converter System/Microprocessor Compatible
*Am6689	– 8-Bit, Ultra High Speed D/A Converter (ECL)
*Am6012	– 12-Bit High Speed Multiplying D/A Converter

Analog to Digital Converters

*Am6688	– 4-Bit Quantizer (Ultra High Speed A/D Converter)

Successive Approximation Registers

Am2502	– 8-Bit Successive Approximation Registers
Am2503	– 8-Bit Successive Approximation Registers
Am2504	– 12-Bit Successive Approximation Registers

Sample and Hold Amplifiers

LF198/398	–Monolithic Sample and Hold Amplifier
*Am6098	–Precision Sample and Hold Amplifier

Comparators

LM111/311	– Precision Voltage Comparator
LM119/319	– Dual Comparator
Am686	– High Speed Voltage Comparator

High Speed Operational Amplifiers

Am118/318	– High Speed Operational Amplifier
LF155/156/157	– JFET Input Operational Amplifiers
LF355/356/357	– JFET Input Operational Amplifiers

* To be announced.

APPLICATIONS

Instrumentation and Control

Data Acquisition
Data Distribution
Data Transceiver
Function Generation
Servo Controls
Programmable Power Supplies
Digital Zero Scale Calibration
Digital Full Scale Calibration
Digitally Controlled Offset Null

Signal Processing

CRT Displays
Floating Point Analog Processors
IF Gain Control
Four Quadrant Multiplexer
8 x 8 Digital Multiplication
Line Driver

A/D Converters

Ratiometric ADC
Differential Input ADC
Multiple Input Range ADC
Two Channel ADC
Microprocessor Controlled ADC

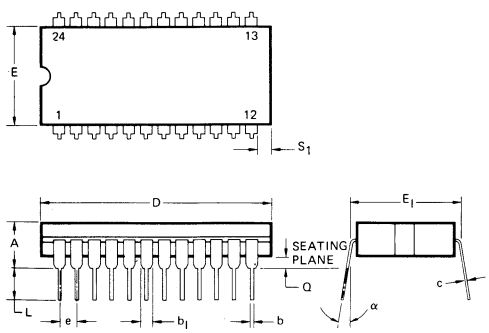
Audio

Music Distribution
Digitally Controlled Gain
Potentiometer Replacement
Digital Recording
Speech Digitizing

D/A Converters

Single Quadrant Multiplying DAC
Two Quadrant Multiplying DAC
Four Quadrant Multiplying DAC
Two Channel DAC
Multiple Output Range DAC

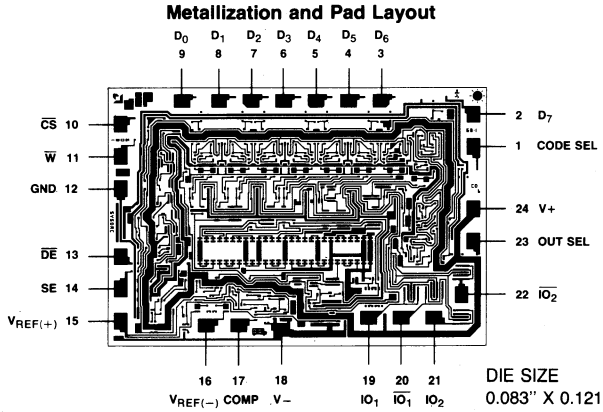
PHYSICAL DIMENSIONS
24-Pin Hermetic DIP



Reference Symbol	Inches	
	Min.	Max.
A	.150	.225
b	.016	.020
b_1	.045	.065
c	.009	.011
D	1.230	1.285
E	.510	.545
E_1	.600	.620
e	.090	.110
L	.120	.150
Q	.015	.060
S*	.010	
α	3°	13°

*From edge of end lead.

Metallization and Pad Layout



DIE SIZE
0.083" X 0.121"

Am9511
Arithmetic Processor

DISTINCTIVE CHARACTERISTICS

- Fixed point 16 and 32 bit operations
- Floating point 32 bit operations
- Binary data formats
- Add, Subtract, Multiply and Divide
- Trigonometric and inverse trigonometric functions
- Square roots, logarithms, exponentiation
- Float to fixed and fixed to float conversions
- Stack-oriented operand storage
- DMA or programmed I/O data transfers
- End signal simplifies concurrent processing
- General purpose 8-bit data bus interface
- Standard 24 pin package
- +12 volt and +5 volt power supplies
- Advanced N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

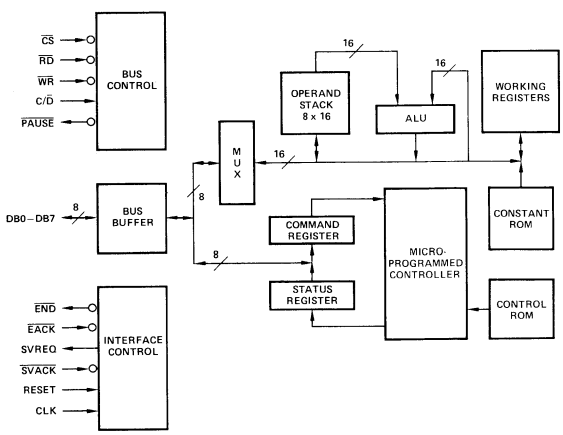
GENERAL DESCRIPTION

The Am9511 Arithmetic Processing Unit (APU) is a monolithic MOS/LSI device that provides high performance fixed and floating point arithmetic and a variety of floating point trigonometric and mathematical operations. It may be used to enhance the computational capability of a wide variety of processor-oriented systems.

All transfers, including operand, result, status and command information, take place over an 8-bit bidirectional data bus. Operands are pushed onto an internal stack and a command is issued to perform operations on the data in the stack. Results are then available to be retrieved from the stack, or additional commands may be entered.

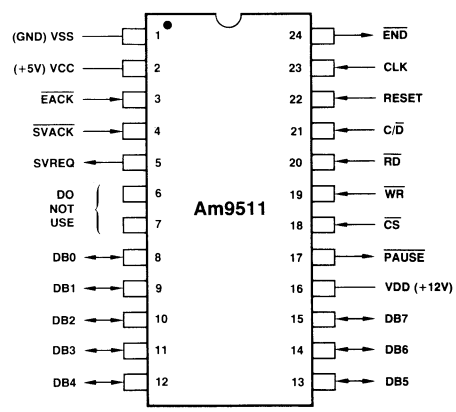
Transfers to and from the APU may be handled by the associated processor using conventional programmed I/O, or may be handled by a direct memory access controller for improved performance. Upon completion of each command, the APU issues an end of execution signal that may be used as an interrupt by the CPU to help coordinate program execution.

BLOCK DIAGRAM



MOS-046

CONNECTION DIAGRAM
Top View



Pin 1 is marked for orientation.

MOS-047

ORDERING INFORMATION

Package Type	Ambient Temperature	Clock Frequency		
		2MHz	3MHz	4MHz
Hermetic DIP	$0°C \leq T_A \leq +70°C$	Am9511DC	Am9511-1DC	Am9511-4DC
	$-55°C \leq T_A \leq +125°C$	Am9511DM	Am9511-1DM	

INTERFACE SIGNAL DESCRIPTION

VCC: +5 Volt power supply

VDD: +12 Volt power supply

VSS: Ground

CLK (Clock, Input)

An external timing source should be applied to the CLK pin. The Clock input may be asynchronous to the Read and Write control signals.

RESET (Reset, Input)

The active high Reset signal provides initialization for the chip. Reset terminates any operation in progress, clears the status register and places the Am9511 into the idle state. Stack contents are not affected by Reset. The Reset should be active for at least 5 clock periods following stable supply voltages and stable clock input. There is no internal power-on reset.

$\overline{CS}$ (Chip Select, Input)

$\overline{CS}$ is an active low input signal which conditions the read and write signals and thus enables communication with the data bus.

C/$\overline{D}$ (Command/Data, Input)

In conjunction with the $\overline{RD}$ and $\overline{WR}$ signals, the C/$\overline{D}$ control line establishes the type of transfers that are to be performed on the data bus.

C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	Function
0	1	0	Enter data byte into stack
0	0	1	Read data byte from stack
1	1	0	Enter command
1	0	1	Read status

$\overline{RD}$ (Read, Input)

The active low Read signal is conditioned by $\overline{CS}$ and indicates that information is to be transferred from internal locations to the data bus. $\overline{RD}$ and $\overline{WR}$ are mutually exclusive.

$\overline{WR}$ (Write, Input)

The active low Write signal is conditioned by $\overline{CS}$ and indicates that information is to be transferred from the data bus into internal locations. $\overline{RD}$ and $\overline{WR}$ are mutually exclusive.

$\overline{EACK}$ (End Acknowledge, Input)

This active low input clears the end of execution output signal ($\overline{END}$). If $\overline{EACK}$ is tied low, the $\overline{END}$ output will be a pulse that is less than one clock period wide.

$\overline{SVACK}$ (Service Acknowledge, Input)

This active low input clears the service request output (SVREQ).

$\overline{END}$ (End Execution, Output)

This active low, open-drain output indicates that execution of the previously entered command is complete. It can be used as an interrupt request and is cleared by $\overline{EACK}$, RESET or any read or write access to the Am9511.

SVREQ (Service Request, Output)

This active high output signal indicates that command execution is complete and that post execution service was requested in the previous command byte. It is cleared by $\overline{SVACK}$, by RESET, or by the end of a subsequent command that does not request service.

$\overline{PAUSE}$ (Pause, Output)

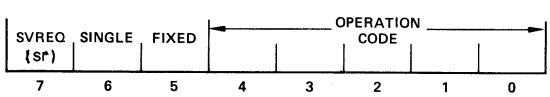
This active low output indicates that the Am9511 has not yet completed its information transfer with the host (or DMA) over the data bus. Whenever a data read or a status read operation is requested, $\overline{PAUSE}$ goes low. It returns high only after the data bus contains valid output data. When an existing command is still in the process of execution, and a data write, data read, or command write is requested, then $\overline{PAUSE}$ goes low for the remaining duration of the existing command plus any time needed for initiating a data read. In both cases, the host should neither change any information to the Am9511, nor (in the case of data read or status read) attempt to capture data from the Am9511 DB outputs until $\overline{PAUSE}$ has returned high. (See "Pause Operation" section on page 5).

DB0-DB7 (Bidirectional Data Bus, I/O)

These eight bidirectional lines provide for transfer of commands, status and data between the Am9511 and the CPU. The Am9511 will drive the data bus only when $\overline{CS}$ and $\overline{RD}$ are low.

COMMAND STRUCTURE

Each command entered into the Am9511 consists of a single 8-bit byte having the format illustrated below:



Bits 0-4 select the operation to be performed as shown in the table. Bits 5-6 select the data format for the operation. If bit 5 is a 1, a fixed point data format is specified. If bit 5 is a 0, floating point format is specified. Bit 6 selects the precision of the data to be operated on by fixed point commands (if bit 5 = 0, bit 6 must be 0). If bit 6 is a 1, single-precision (16-bit) operands are indicated; if bit 6 is a 0, double-precision (32-bit) operands are indicated. Results are undefined for all illegal combinations of bits in the command byte. Bit 7 indicates whether a service request is to be issued after the command is executed. If bit 7 is a 1, the service request output (SVREQ) will go high at the conclusion of the command and will remain high until reset by a low level on the service acknowledge pin ($\overline{SVACK}$) or until completion of execution of a succeeding command where bit 7 is 0. Each command issued to the Am9511 requests post execution service based upon the state of bit 7 in the command byte. When bit 7 is a 0, SVREQ remains low.

COMMAND SUMMARY

Command Code								Command Mnemonic	Command Description
7	6	5	4	3	2	1	0		
FIXED POINT 16 BIT									
sr	1	1	0	1	1	0	0	SADD	Add TOS to NOS. Result to NOS. Pop Stack.
sr	1	1	0	1	1	0	1	SSUB	Subtract TOS from NOS. Result to NOS. Pop Stack.
sr	1	1	0	1	1	1	0	SMUL	Multiply NOS by TOS. Lower half of result to NOS. Pop Stack.
sr	1	1	1	0	1	1	0	SMUU	Multiply NOS by TOS. Upper half of result to NOS. Pop Stack.
sr	1	1	0	1	1	1	1	SDIV	Divide NOS by TOS. Result to NOS. Pop Stack.
FIXED POINT 32 BIT									
sr	0	1	0	1	1	0	0	DADD	Add TOS to NOS. Result to NOS. Pop Stack.
sr	0	1	0	1	1	0	1	DSUB	Subtract TOS from NOS. Result to NOS. Pop Stack.
sr	0	1	0	1	1	1	0	DMUL	Multiply NOS by TOS. Lower half of result to NOS. Pop Stack.
sr	0	1	1	0	1	1	0	DMUU	Multiply NOS by TOS. Upper half of result to NOS. Pop Stack.
sr	0	1	0	1	1	1	1	DDIV	Divide NOS by TOS. Result to NOS. Pop Stack.
FLOATING POINT 32 BIT									
sr	0	0	1	0	0	0	0	FADD	Add TOS to NOS. Result to NOS. Pop Stack.
sr	0	0	1	0	0	0	1	FSUB	Subtract TOS from NOS. Result to NOS. Pop Stack.
sr	0	0	1	0	0	1	0	FMUL	Multiply NOS by TOS. Result to NOS. Pop Stack.
sr	0	0	1	0	0	1	1	FDIV	Divide NOS by TOS. Result to NOS. Pop Stack.
DERIVED FLOATING POINT FUNCTIONS									
sr	0	0	0	0	0	0	1	SQRT	Square Root of TOS. Result in TOS.
sr	0	0	0	0	0	1	0	SIN	Sine of TOS. Result in TOS.
sr	0	0	0	0	0	1	1	COS	Cosine of TOS. Result in TOS.
sr	0	0	0	0	1	0	0	TAN	Tangent of TOS. Result in TOS.
sr	0	0	0	0	1	0	1	ASIN	Inverse Sine of TOS. Result in TOS.
sr	0	0	0	0	1	1	0	ACOS	Inverse Cosine of TOS. Result in TOS.
sr	0	0	0	0	1	1	1	ATAN	Inverse Tangent of TOS. Result in TOS.
sr	0	0	0	1	0	0	0	LOG	Common Logarithm (base 10) of TOS. Result in TOS.
sr	0	0	0	1	0	0	1	LN	Natural Logarithm (base e) of TOS. Result in TOS.
sr	0	0	0	1	0	1	0	EXP	Exponential (e^X) of TOS. Result in TOS.
sr	0	0	0	1	0	1	1	PWR	NOS raised to the power in TOS. Result in NOS. Pop Stack.
DATA MANIPULATION COMMANDS									
sr	0	0	0	0	0	0	0	NOP	No Operation
sr	0	0	1	1	1	1	1	FIXS	Convert TOS from floating point to 16-bit fixed point format.
sr	0	0	1	1	1	1	0	FIXD	Convert TOS from floating point to 32-bit fixed point format.
sr	0	0	1	1	1	0	1	FLTS	Convert TOS from 16-bit fixed point to floating point format.
sr	0	0	1	1	1	0	0	FLTD	Convert TOS from 32-bit fixed point to floating point format.
sr	1	1	1	0	1	0	0	CHSS	Change sign of 16-bit fixed point operand on TOS.
sr	0	1	1	0	1	0	0	CHSD	Change sign of 32-bit fixed point operand on TOS.
sr	0	0	1	0	1	0	1	CHSF	Change sign of floating point operand on TOS.
sr	1	1	1	0	1	1	1	PTOS	Push 16-bit fixed point operand on TOS to NOS (Copy)
sr	0	1	1	0	1	1	1	PTOD	Push 32-bit fixed point operand on TOS to NOS. (Copy)
sr	0	0	1	0	1	1	1	PTOF	Push floating point operand on TOS to NOS. (Copy)
sr	1	1	1	1	0	0	0	POPS	Pop 16-bit fixed point operand from TOS. NOS becomes TOS.
sr	0	1	1	1	0	0	0	POPD	Pop 32-bit fixed point operand from TOS. NOS becomes TOS.
sr	0	0	1	1	0	0	0	POPF	Pop floating point operand from TOS. NOS becomes TOS.
sr	1	1	1	1	0	0	1	XCHS	Exchange 16-bit fixed point operands TOS and NOS.
sr	0	1	1	1	0	0	1	XCHD	Exchange 32-bit fixed point operands TOS and NOS.
sr	0	0	1	1	0	0	1	XCHF	Exchange floating point operands TOS and NOS.
sr	0	0	1	1	0	1	0	PUPI	Push floating point constant "π" onto TOS. Previous TOS becomes NOS.

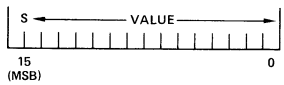
NOTES:

1. TOS means Top of Stack. NOS means Next on Stack.
2. AMD Application Brief "Algorithm Details for the Am9511 APU" provides detailed descriptions of each command function, including data ranges, accuracies, stack configurations, etc.
3. Many commands destroy one stack location (bottom of stack) during development of the result. The derived functions may destroy several stack locations. See Application Brief for details.
4. The trigonometric functions handle angles in radians, not degrees.
5. No remainder is available for the fixed-point divide functions.
6. Results will be undefined for any combination of command coding bits not specified in this table.

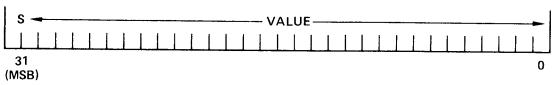
DATA FORMATS

The Am9511 Arithmetic Processing Unit handles operands in both fixed point and floating point formats. Fixed point operands may be represented in either single (16-bit operands) or double precision (32-bit operands), and are always represented as binary, two's complement values.

16-BIT FIXED POINT FORMAT



32-BIT FIXED POINT FORMAT



The sign (positive or negative) of the operand is located in the most significant bit (MSB). Positive values are represented by a sign bit of zero (S = 0). Negative values are represented by the two's complement of the corresponding positive value with a sign bit equal to 1 (S = 1). The range of values that may be accommodated by each of these formats is −32,768 to +32,767 for single precision and −2,147,483,648 to +2,147,483,647 for double precision.

Floating point binary values are represented in a format that permits arithmetic to be performed in a fashion analogous to operations with decimal values expressed in scientific notation.

$$(5.83 \times 10^{2})(8.16 \times 10^{1}) = (4.75728 \times 10^{4})$$

In the decimal system, data may be expressed as values between 0 and 10 times 10 raised to a power that effectively shifts the implied decimal point right or left the number of places necessary to express the result in conventional form (e.g., 47,572.8). The value-portion of the data is called the mantissa. The exponent may be either negative or positive.

The concept of floating point notation has both a gain and a loss associated with it. The gain is the ability to represent the significant digits of data with values spanning a large dynamic range limited only by the capacity of the exponent field. For example, in decimal notation if the exponent field is two digits wide, and the mantissa is five digits, a range of values (positive or negative) from 1.0000×10^{-99} to $9.9999 \times 10^{+99}$ can be accommodated. The loss is that only the significant digits of the value can be represented. Thus there is no distinction in this representation between the values 123451 and 123452, for example, since each would be expressed as: 1.2345×10^{5}. The sixth digit has been discarded. In most applications where the dynamic range of values to be represented is large, the loss of significance, and hence accuracy of results, is a minor consideration. For greater precision a fixed point format could be chosen, although with a loss of potential dynamic range.

The Am9511 is a binary arithmetic processor and requires that floating point data be represented by a fractional mantissa value between .5 and 1 multiplied by 2 raised to an appropriate power. This is expressed as follows:

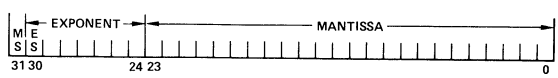
$$\text{value} = \text{mantissa} \times 2^{\text{exponent}}$$

For example, the value 100.5 expressed in this form is 0.11001001×2^{7}. The decimal equivalent of this value may be computed by summing the components (powers of two) of the mantissa and then multiplying by the exponent as shown below:

$$\begin{aligned}\text{value} &= (2^{-1} + 2^{-2} + 2^{-5} + 2^{-8}) \times 2^{7} \\ &= (0.5 + 0.25 + 0.03125 + 0.00290625) \times 128 \\ &= 0.78515625 \times 128 \\ &= 100.5\end{aligned}$$

FLOATING POINT FORMAT

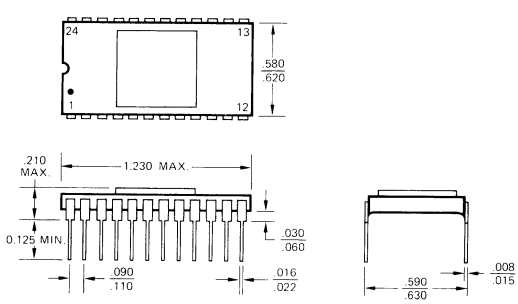
The format for floating point values in the Am9511 is given below. The mantissa is expressed as a 24-bit (fractional) value; the exponent is expressed as an unbiased two's complement 7-bit value having a range of −64 to +63. The most significant bit is the sign of the mantissa (0 = positive, 1 = negative), for a total of 32 bits. The binary point is assumed to be to the left of the most significant mantissa bit (bit 23). All floating point data values must be normalized. Bit 23 must be equal to 1, except for the value zero, which is represented by all zeros.



The range of values that can be represented in this format is $\pm(2.7 \times 10^{-20}$ to $9.2 \times 10^{18})$ and zero.

PHYSICAL DIMENSIONS
Dual-In-Line

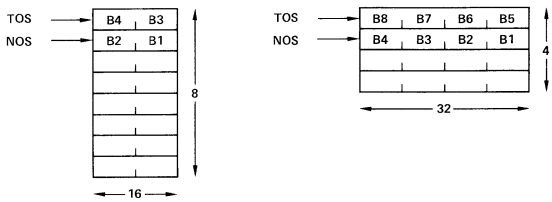
24-Pin Side-Brazed



FUNCTIONAL DESCRIPTION

Stack Control

The user interface to the Am9511 includes access to an 8 level 16-bit wide data stack. Since single precision fixed point operands are 16 bits in length, eight such values may be maintained in the stack. When using double precision fixed point or floating point formats four values may be stored. The stack in these two configurations can be visualized as shown below:



Data are written onto the stack, eight bits at a time, in the order shown (B1, B2, B3, . . .). Data are removed from the stack in reverse byte order (B8, B7, B6, . . .). Data should be transferred into or out of the stack in multiples of the number of bytes appropriate to the chosen data format.

Data Entry

Data entry is accomplished by bringing the chip select ($\overline{CS}$), the command/data line (C/$\overline{D}$), and $\overline{WR}$ low, as shown in the timing diagram. The entry of each new data word "pushes down" the previously entered data and places the new byte on the top of stack (TOS). Data on the bottom of the stack prior to a stack entry are lost.

Data Removal

Data are removed from the stack in the Am9511 by bringing chip select ($\overline{CS}$), command/data (C/$\overline{D}$), and $\overline{RD}$ low as shown in the timing diagram. The removal of each data word redefines TOS so that the next successive byte to be removed becomes TOS. Data removed from the stack rotates to the bottom of the stack.

Command Entry

After the appropriate number of bytes of data have been entered onto the stack, a command may be issued to perform an operation on that data. Commands which require two operands for execution (e.g., add) operate on the TOS and NOS values. Single operand commands operate only on the TOS.

Commands are issued to the Am9511 by bringing the chip select ($\overline{CS}$) line low, command/data (C/$\overline{D}$) line high, and $\overline{WR}$ line low as indicated by the timing diagram. After a command is issued, the CPU can continue execution of its program concurrently with the Am9511 command execution.

Command Completion

The Am9511 signals the completion of each command execution by lowering the End Execution line ($\overline{END}$). Simultaneously, the busy bit in the status register is cleared and the Service Request bit of the command register is checked. If it is a "1" the service request output level (SVREQ) is raised. $\overline{END}$ is cleared on receipt of an active low End Acknowledge ($\overline{EACK}$) pulse. Similarly, the service request line is cleared by recognition of an active low Service Acknowledge ($\overline{SVACK}$) pulse.

Pause Operation

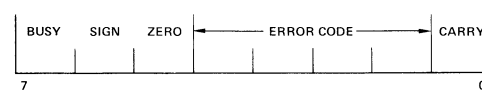
An active low Pause ($\overline{PAUSE}$) is provided. This line is high in its quiescent state and is pulled low by the Am9511 under the following conditions:

1. A previously initiated operation is in progress (device busy) and Command Entry has been attempted. In this case, the $\overline{PAUSE}$ line will be pulled low and remain low until completion of the current command execution. It will then go high, permitting entry of the new command.
2. A previously initiated operation is in progress and stack access has been attempted. In this case, the $\overline{PAUSE}$ line will be pulled low, will remain in that state until execution is complete, and will then be raised to permit completion of the stack access.
3. The Am9511 is not busy, and data removal has been requested. $\overline{PAUSE}$ will be pulled low for the length of time necessary to transfer the byte from the top of stack to the interface latch, and will then go high, indicating availability of the data.
4. The Am9511 is not busy, and a data entry has been requested. $\overline{PAUSE}$ will be pulled low for the length of time required to ascertain if the preceding data byte, if any has been written to the stack. If so $\overline{PAUSE}$ will immediately go high. If not, $\overline{PAUSE}$ will remain low until the interface latch is free and will then go high.
5. When a status read has been requested, $\overline{PAUSE}$ will be pulled low for the length of time necessary to transfer the status to the interface latch, and will then be raised to permit completion of the status read. Status may be read whether or not the Am9511 is busy.

When $\overline{PAUSE}$ goes low, the APU expects the bus and bus control signals present at the time to remain stable until $\overline{PAUSE}$ goes high.

Device Status

Device status is provided by means of an internal status register whose format is shown below:



BUSY: Indicates that Am9511 is currently executing a command (1 = Busy).

SIGN: Indicates that the value on the top of stack is negative (1 = Negative).

ZERO: Indicates that the value on the top of stack is zero (1 = Value is zero).

ERROR CODE: This field contains an indication of the validity of the result of the last operation. The error codes are:

0000 – No error
1000 – Divide by zero
0100 – Square root or log of negative number
1100 – Argument of inverse sine, cosine, or e^x too large
XX10 – Underflow
XX01 – Overflow

CARRY: Previous operation resulted in carry or borrow from most significant bit. (1 = Carry/Borrow, 0 = No Carry/No Borrow)

If the BUSY bit in the status register is a one, the other status bits are not defined; if zero, indicating not busy, the operation is complete and the other status bits are defined as given above.

Read Status

The Am9511 status register can be read by the CPU at any time (whether an operation is in progress or not) by bringing the chip select ($\overline{CS}$) low, the command-data line (C/$\overline{D}$) high, and lowering $\overline{RD}$. The status register is then gated onto the data bus and may be input by the CPU.

EXECUTION TIMES

Timing for execution of the Am9511 command set is shown in the table below. Speeds are given in terms of clock cycles and should be multiplied by the clock period being used to arrive at time values. Where substantial variation of execution times is possible, the minimum and maximum values are shown; otherwise, typical values are given. Variations are data dependent. Some boundary conditions that will cause shorter execution times are not taken into account. The listing is in alphabetical order by mnemonic.

Total execution times may require allowances for operand transfer into the APU, command execution, and result retrieval from the APU. Except for command execution, these times will be heavily influenced by the nature of the data, the control interface used, the speed of memory, the CPU used, the priority allotted to DMA and Interrupt operations, the size and number of operands to be transferred, and the use of chained calculations, etc.

COMMAND EXECUTION TIMES

Command Mnemonic	Clock Cycles	Command Mnemonic	Clock Cycles
ACOS	6304-8284	LOG	4474-7132
ASIN	6230-7938	LN	4298-6956
ATAN	4992-6536	NOP	4
CHSD	26-28	POPD	12
CHSF	16-20	POPF	12
CHSS	22-24	POPS	10
COS	3840-4878	PTOD	20
DADD	20-22	PTOF	20
DDIV	196-210	PTOS	16
DMUL	194-210	PUPI	16
DMUU	182-218	PWR	8290-12032
DSUB	38-40	SADD	16-18
EXP	3794-4878	SDIV	84-94
FADD	54-368	SIN	3796-4808
FDIV	154-184	SMUL	84-94
FIXD	90-336	SMUU	80-98
FIXS	90-214	SQRT	782-870
FLTD	56-342	SSUB	30-32
FLTS	62-156	TAN	4894-5886
FMUL	146-168	XCHD	26
FSUB	70-370	XCHF	26
		XCHS	18

As mentioned, the above clock cycle execution times can be converted to μsec by multiplying by the clock period used. Several examples (minimums) are shown below:

Command Description	Am9511 (2MHz)	Am9511-1 (3MHz)	Am9511-4 (4MHz)
32-Bit Floating-Point Cosine (COS)	1920μsec	1280μsec	960μsec
32-Bit Floating-Point e^x (EXP)	1897μsec	1265μsec	949μsec
32-Bit Floating Point Multiply (FMUL)	73μsec	49μsec	37μsec
16-Bit Fixed-Point Multiply, Lower (SMUL)	42μsec	28μsec	21μsec
32-Bit Floating-Point Add (FADD)	27μsec	18μsec	14μsec
16-Bit Fixed-Point Add (SADD)	8μsec	5μsec	4μsec

MAXIMUM RATINGS beyond which useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
VDD with Respect to VSS	−0.5V to +15.0V
VCC with Respect to VSS	−0.5V to +7.0V
All Signal Voltages with Respect to VSS	−0.5V to +7.0V
Power Dissipation (Package Limitation)	2.0W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	VSS	VCC	VDD
Am9511DC	$0°C \leq T_A \leq +70°C$	0V	+5.0V ±5%	+12V ±5%
Am9511DM	$-55°C \leq T_A \leq +125°C$	0V	+5.0V ±10%	+12V ±10%

ELECTRICAL CHARACTERISTICS Over Operating Range (Note 1)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
VOH	Output HIGH Voltage	IOH = −200μA	3.7			Volts
VOL	Output LOW Voltage	IOL = 3.2mA			0.4	Volts
VIH	Input HIGH Voltage		2.0		VCC	Volts
VIL	Input LOW Voltage		−0.5		0.8	Volts
IIX	Input Load Current	$VSS \leq VI \leq VCC$			±10	μA
IOZ	Data Bus Leakage	VO = 0.4V			10	μA
		VO = VCC			10	
ICC	VCC Supply Current	T_A = +25°C		50	90	mA
		T_A = 0°C			95	
		T_A = −55°C			100	
IDD	VDD Supply Current	T_A = +25°C		50	90	mA
		T_A = 0°C			95	
		T_A = −55°C			100	
CO	Output Capacitance	fc = 1.0MHz, Inputs = 0V		8	10	pF
CI	Input Capacitance			5	8	pF
CIO	I/O Capacitance			10	12	pF

SWITCHING CHARACTERISTICS over operating range (Notes 2, 3)

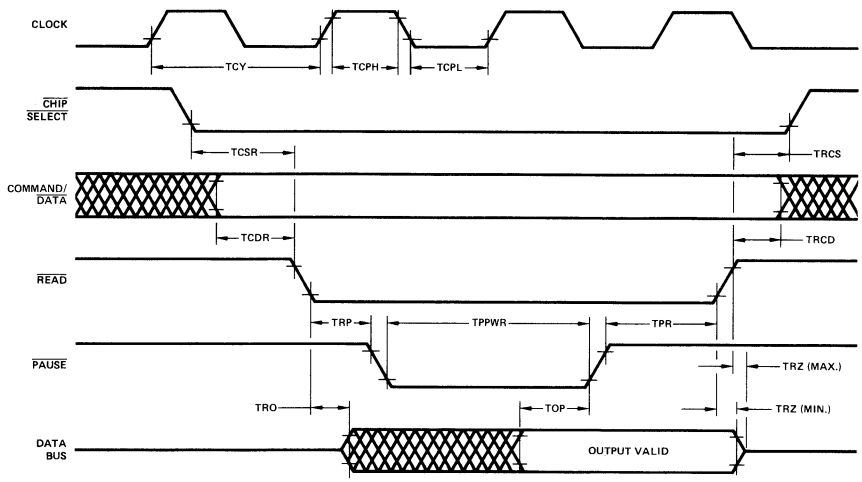
Parameters	Description		Am9511 Min.	Am9511 Max.	Am9511-1 Min.	Am9511-1 Max.	(Preliminary) Am9511-4 Min.	(Preliminary) Am9511-4 Max.	Units
TAPW	$\overline{EACK}$ LOW Pulse Width		100		75		50		ns
TCDR	C/$\overline{D}$ to $\overline{RD}$ LOW Set up Time		0		0		0		ns
TCDW	C/$\overline{D}$ to $\overline{WR}$ LOW Set up Time		0		0		0		ns
TCPH	Clock Pulse HIGH Width		200		140		100		ns
TCPL	Clock Pulse LOW Width		240		160		120		ns
TCSR	$\overline{CS}$ LOW to $\overline{RD}$ LOW Set up Time		50		25		25		ns
TCSW	$\overline{CS}$ LOW to $\overline{WR}$ LOW Set up Time		50		25		25		ns
TCY	Clock Period		480	5000	330	3300	250	2500	ns
TDW	Data Bus Stable to $\overline{WR}$ HIGH Set up Time			150		100		100	ns
TEAE	$\overline{EACK}$ LOW to $\overline{END}$ HIGH Delay			200		175		150	ns
TEPW	$\overline{END}$ LOW Pulse Width (Note 4)		400		300		200		ns
TOP	Data Bus Output Valid to $\overline{PAUSE}$ HIGH Delay		0		0		0		ns
TPPWR	$\overline{PAUSE}$ LOW Pulse Width Read (Note 5)	Data	3.5TCY+50	5.5TCY+300	3.5TCY+50	5.5TCY+200	3.5TCY+50	5.5TCY+200	ns
		Status	1.5TCY+50	3.5TCY+300	1.5TCY+50	3.5TCY+200	1.5TCY+50	3.5TCY+200	
TPPWW	$\overline{PAUSE}$ LOW Pulse Width Write (Note 8)			50		50		50	ns
TPR	$\overline{PAUSE}$ HIGH to $\overline{RD}$ HIGH Hold Time		0		0		0		ns
TPW	$\overline{PAUSE}$ HIGH to $\overline{WR}$ HIGH Hold Time		0		0		0		ns
TRCD	$\overline{RD}$ HIGH to C/$\overline{D}$ Hold Time		0		0		0		ns
TRCS	$\overline{RD}$ HIGH to $\overline{CS}$ HIGH Hold Time		0		0		0		ns
TRO	$\overline{RD}$ LOW to Data Bus ON Delay		50		50		25		ns
TRP	$\overline{RD}$ LOW to $\overline{PAUSE}$ LOW Delay (Note 6)			150		100		100	ns
TRZ	$\overline{RD}$ HIGH to Data Bus OFF Delay		50	200	50	150	25	100	ns
TSAPW	$\overline{SVACK}$ LOW Pulse Width		100		75		50		ns
TSAR	$\overline{SVACK}$ LOW to $\overline{SVREQ}$ LOW Delay			300		200		150	ns
TWCD	$\overline{WR}$ HIGH to C/$\overline{D}$ Hold Time		60		30		30		ns
TWCS	$\overline{WR}$ HIGH to $\overline{CS}$ HIGH Hold Time		60		30		30		ns
TWD	$\overline{WR}$ HIGH to Data Bus Hold Time		20		20		20		ns
TWI	Write Inactive Time (Note 8)	Command	3TCY		3TCY		3TCY		ns
		Data	4TCY		4TCY		4TCY		
TWP	$\overline{WR}$ LOW to $\overline{PAUSE}$ LOW Delay (Note 6)			150		100		100	ns

NOTES

1. Typical values are for $T_A = 25°C$, nominal supply voltages and nominal processing parameters.
2. Switching parameters are listed in alphabetical order.
3. Test conditions assume transition times of 20ns or less, output loading of one TTL gate plus 100pF and timing reference levels of 0.8V and 2.0V.
4. $\overline{END}$ low pulse width is specified for $\overline{EACK}$ tied to VSS. Otherwise TEAE applies.
5. Minimum values shown assume no previously entered command is being executed for the data access. If a previously entered command is being executed, $\overline{PAUSE}$ LOW Pulse Width is the time to complete exeuction plus the time shown. Status may be read at any time without exceeding the time shown.
6. $\overline{PAUSE}$ is pulled low for both command and data operations.
7. TEX is the execution time of the current command (see the Command Execution Times table).
8. $\overline{PAUSE}$ low pulse width is less than 50ns when writing into the data port or the control port as long as the duty cycle requirement (TWI) is observed and no previous command is being executed. TWI may be safely violated as long as the extended TPPWW that results is observed. If a previously entered command is being executed, $\overline{PAUSE}$ LOW Pulse Width is the time to complete execution plus the time shown.

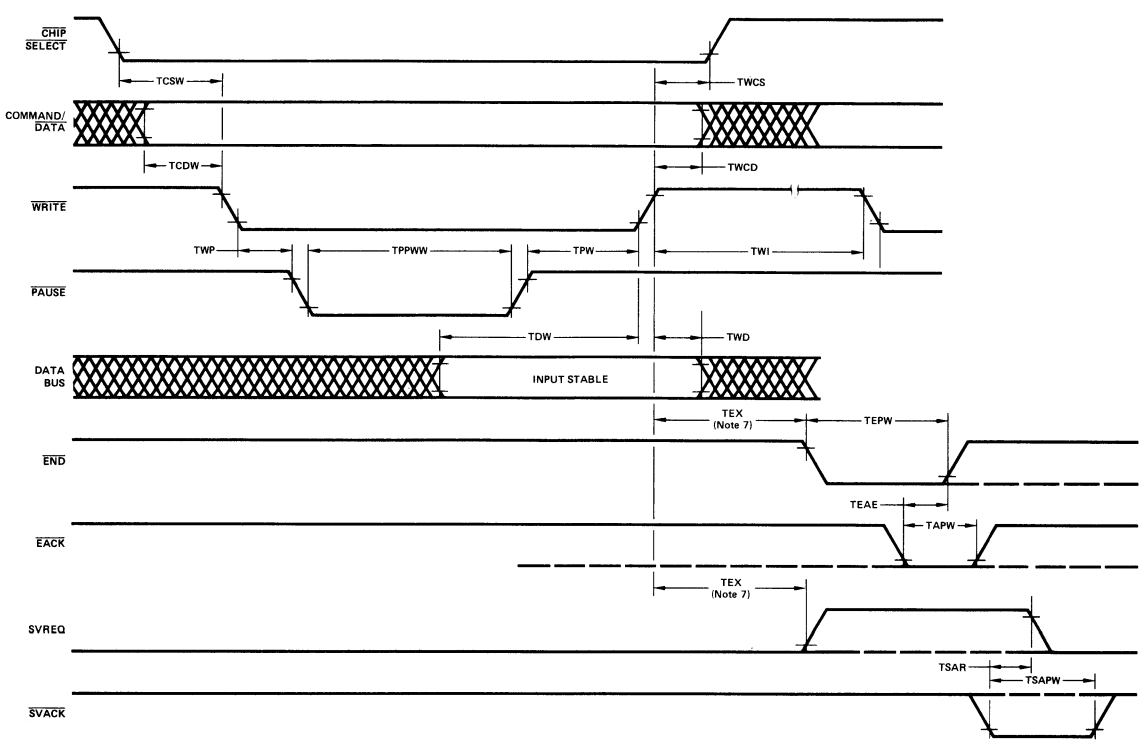
SWITCHING WAVEFORMS

READ OPERATIONS



MOS-048

WRITE OPERATIONS



MOS-049

APPLICATION INFORMATION

The diagram in Figure 2 shows the interface connections for the Am9511 APU with operand transfers handled by an Am9517 DMA controller, and CPU coordination handled by an Am9519 Interrupt Controller. The APU interrupts the CPU to indicate that a command has been completed. When the performance enhancements provided by the DMA and Interrupt operations are not required, the APU interface can be simplified as shown in Figure 1. The Am9511 APU is designed with a general purpose 8-bit data bus and interface control so that it can be conveniently used with any general 8-bit processor.

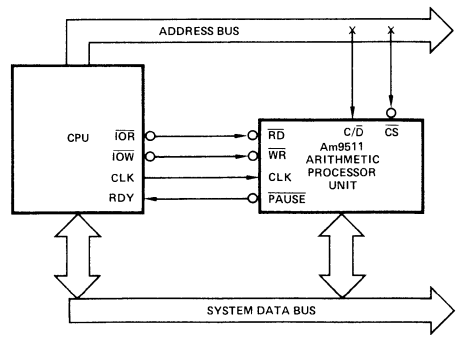


Figure 1. Am9511 Minimum Configuration Example.

MOS-050

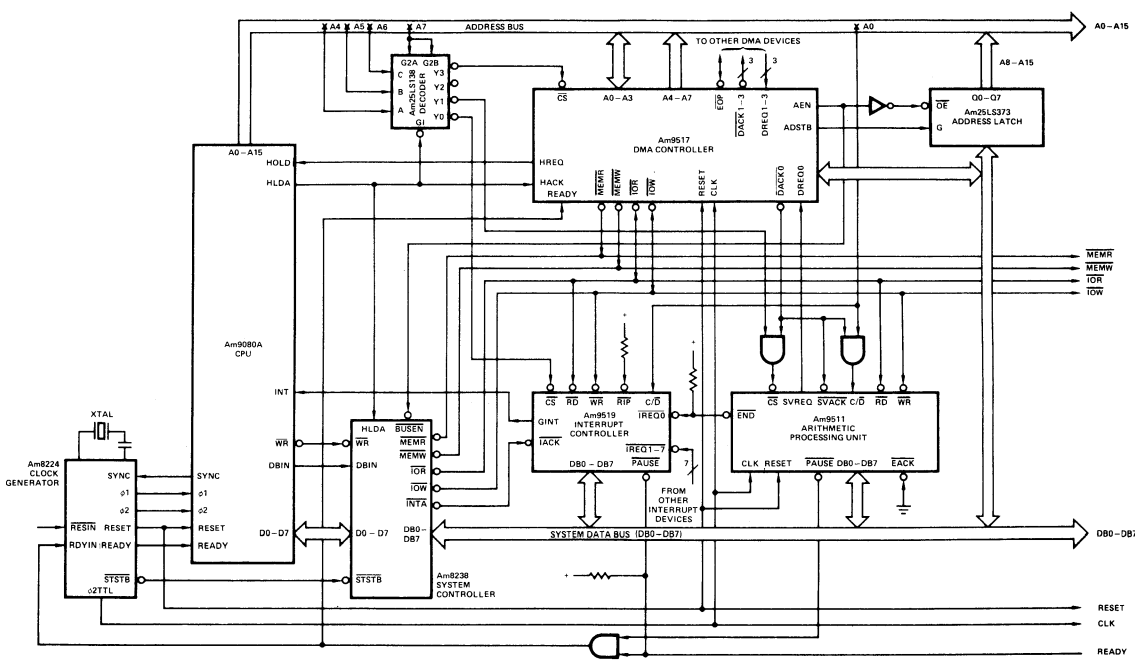


Figure 2. Am9511 High Performance Configuration Example.

MOS-051

Am9517

Multimode DMA Controller

DISTINCTIVE CHARACTERISTICS

- Four independent DMA channels, each with separate registers for Mode Control, Current Address, Base Address, Current Word Count and Base Word Count.
- Transfer modes: Block, Demand, Single Word, Cascade
- Independent autoinitialization of all channels
- Memory-to-memory transfers
- Memory block initialization
- Address increment or decrement
- Master system disable
- Enable/disable control of individual DMA requests
- Directly expandable to any number of channels
- End of Process input for terminating transfers
- Software DMA requests
- Independent polarity control for DREQ and DACK signals
- Compressed timing option speeds transfers – up to 2M words/second
- +5 volt power supply
- Advanced N-channel silicon gate MOS technology
- 40 pin Hermetic DIP package
- 100% MIL-STD-883 reliability assurance testing

GENERAL DESCRIPTION

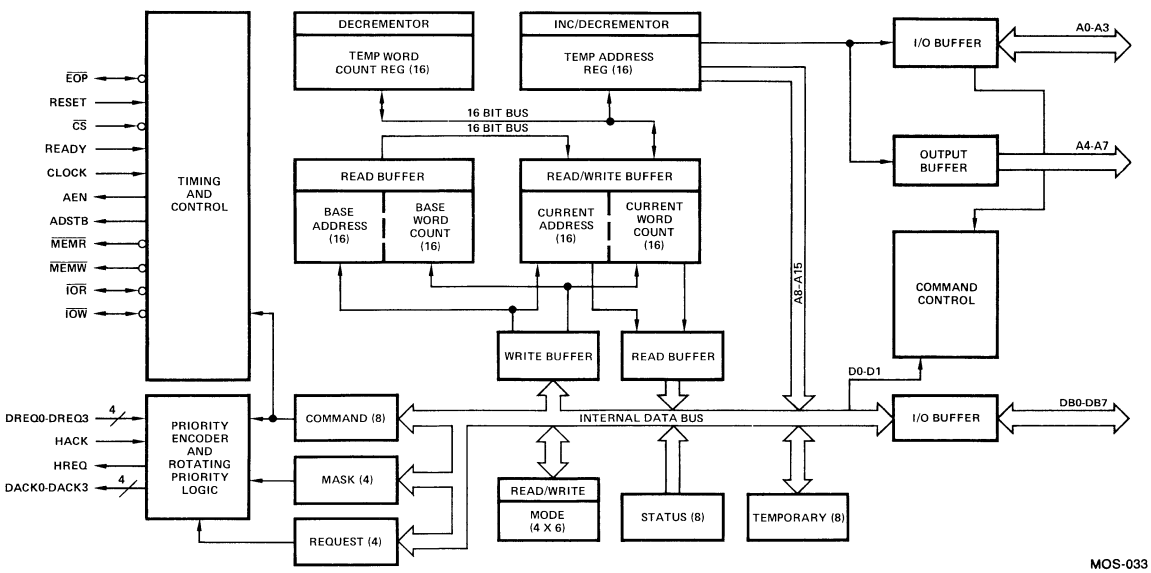
The Am9517 Multimode Direct Memory Access (DMA) Controller is a peripheral interface circuit for microprocessor systems. It is designed to improve system performance by allowing external devices to directly transfer information to or from the system memory. Memory-to-memory transfer capability is also provided. The Am9517 offers a wide variety of programmable control features to enhance data throughput and system optimization and to allow dynamic reconfiguration under program control.

The Am9517 is designed to be used in conjunction with an external 8-bit address register such as the Am74LS373. It contains four independent channels and may be expanded to any number of channels by cascading additional controller chips.

The three basic transfer modes allow programmability of the types of DMA service by the user. Each channel can be individually programmed to Autoinitialize to its original condition following an End of Process ($\overline{EOP}$).

Each channel has a full 64K address and word count capability. An external $\overline{EOP}$ signal can terminate a DMA or memory-to-memory transfer. This is useful for block search or compare operations using external comparators or for intelligent peripherals to abort erroneous services.

BLOCK DIAGRAM



MOS-033

ORDERING INFORMATION

Package Type	Ambient Temperature	Maximum Clock Frequency	
		3MHz	4MHz
Hermetic DIP/ Molded DIP	$0°C \leq T_A \leq +70°C$	Am9517DC/PC Am9517-1DC/PC	Am9517-4DC/PC
Hermetic DIP	$-55°C \leq T_A \leq +125°C$	Am9517DM	

CONNECTION DIAGRAM
Top View

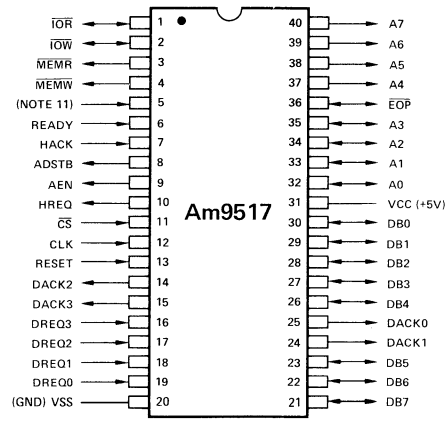


Figure 1.

MOS-034

INTERFACE SIGNAL DESCRIPTION

VCC: +5 Volt Supply
VSS: Ground

CLK (Clock, Input)

This input controls the internal operations of the Am9517 and its rate of data transfers. The input may be driven at up to 3MHz for the standard Am9517 and up to 4MHz for the Am9517-4.

$\overline{CS}$ (Chip Select, Input)

Chip Select is an active low input used to select the Am9517 as an I/O device during the Idle cycle. This allows CPU communication on the data bus.

RESET (Reset, Input)

Reset is an asynchronous active high input which clears the Command, Status, Request and Temporary registers. It also clears the first/last flip/flop and sets the Mask register. Following a Reset the device is in the Idle cycle.

READY (Ready, Input)

Ready is an asynchronous input used to extend the memory read and write pulses from the Am9517 to accommodate slow memories or I/O peripheral devices.

HACK (Hold Acknowledge, Input)

The active high Hold Acknowledge from the CPU indicates that control of the system buses has been relinquished.

DREQ0-DREQ3 (DMA Request, Input)

The DMA Request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In Fixed Priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of the DREQ signal. Polarity of DREQ is programmable. Reset initializes these lines to active high.

DB0-DB7 (Data Bus, Input/Output)

The Data Bus lines are bidirectional three-state signals connected to the system data bus. The outputs are enabled in the Program Condition during the I/O Read to output the contents of an Address register, a Status register, the Temporary register or a Word Count register to the CPU. The outputs are disabled and the inputs are read during an I/O Write cycle when the CPU is programming the Am9517 control registers. During DMA cycles the most significant eight bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In memory-to-memory operations data from the memory comes into the Am9517 on the data bus during the read-from-memory transfer. In the write-to-memory transfer the data bus outputs place the data into the new memory location.

$\overline{IOR}$ (I/O Read, Input/Output)

I/O Read is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to read the control registers. In the Active cycle, it is an output control signal used by the Am9517 to access data from a peripheral during a DMA Write transfer.

$\overline{IOW}$ (I/O Write, Input/Output)

I/O Write is a bidirectional active low three-state line. In the Idle cycle it is an input control signal used by the CPU to load information into the Am9517. In the Active cycle it is an output control signal used by the Am9517 to load data to the peripheral during a DMA Read transfer.

$\overline{EOP}$ (End of Process, Input/Output)

$\overline{EOP}$ is an active low bidirectional signal. Information concerning the completion of DMA services is available at the bidirectional End of Process ($\overline{EOP}$) pin. The Am9517 allows an external signal to terminate an active DMA service. This is accomplished by pulling the $\overline{EOP}$ input low with an external $\overline{EOP}$ signal. The Am9517 also generates a pulse when the terminal count (TC) for any channel is reached. This generates an $\overline{EOP}$ signal which is output through the $\overline{EOP}$ line. The reception of $\overline{EOP}$, either internal or external, will cause the Am9517 to terminate the service, reset the request and if Autoinitialize is enabled, to write the base registers to the current registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel by $\overline{EOP}$ unless the channel is programmed for Autoinitialize. In that case the mask bit remains clear. During memory-to-memory transfers, $\overline{EOP}$ will be output when the TC for channel 1 occurs.

A0-A3 (Address, Input/Output)

The four least significant address lines are bidirectional three-state signals. In the Idle cycle they are inputs and are used by the Am9517 to address the control register to be loaded or read. In the Active cycle they are outputs and provide the lower 4 bits of the output address.

A4-A7 (Address, Output)

The four most significant address lines are three-state outputs and provide four bits of address. These lines are enabled only during the DMA service.

HREQ (Hold Request, Output)

This is the Hold Request to the CPU and is used to request control of the system bus. If the corresponding mask bit is clear, the presence of any valid DREQ causes the Am9517 to issue the HREQ.

DACK0-DACK3 (DMA Acknowledge, Output)

DMA Acknowledge is used to notify the individual peripherals when one has been granted a DMA cycle. The sense of these lines is programmable. Reset initializes them to active low.

AEN (Address Enable, Output)

The Address Enable is an active high level used to enable the output of the external latch which holds the upper byte of address and to disable the system bus during the DMA cycle. Note that during DMA transfers HACK and AEN should be used to deselect all other I/O peripherals which may erroneously be accessed as programmed I/O during the DMA operation. The Am9517 automatically deselects itself during DMA transfer.

ADSTB (Address Strobe, Output)

The active high Address Strobe is used to strobe the upper address byte into an external latch.

$\overline{\text{MEMR}}$ (Memory Read, Output)

The Memory Read signal is an active low three-state output used to access data from the selected memory location during a DMA Read or a memory-to-memory transfer.

$\overline{\text{MEMW}}$ (Memory Write, Output)

The Memory Write signal is an active low three-state output used to write data to the selected memory location during a DMA Write or a memory-to-memory transfer.

FUNCTIONAL DESCRIPTION

The Am9517 block diagram includes the major logic blocks and all of the internal registers. The data interconnection paths are also shown. Not shown are the various control signals between the blocks. The Am9517 contains 344 bits of internal memory in the form of registers. Figure 2 lists these registers by name and shows the size of each. A detailed description of the registers and their functions can be found under Register Description.

Name	Size	Number
Base Address Registers	16 bits	4
Base Word Count Registers	16 bits	4
Current Address Registers	16 bits	4
Current Word Count Registers	16 bits	4
Temporary Address Register	16 bits	1
Temporary Word Count Register	16 bits	1
Status Register	8 bits	1
Command Register	8 bits	1
Temporary Register	8 bits	1
Mode Registers	6 bits	4
Mask Register	4 bits	1
Request Register	4 bits	1

Figure 2. Am9517 Internal Registers.

The Am9517 contains three basic blocks of control logic. The Timing Control block generates internal timing and external control signals for the Am9517. The Program Command Control block decodes the various commands given to the Am9517 by the microprocessor prior to servicing a DMA Request. It also decodes the Mode Control word used to select the type of DMA during the servicing. The Priority Encoder block resolves priority contention between DMA channels requesting service simultaneously.

The Timing Control block derives internal timing from the clock input. In Am9080A systems this input will usually be the $\phi 2$ TTL clock from an Am8224. However, any appropriate system clock will suffice.

DMA OPERATION

The Am9517 is designed to operate in two major cycles. These are called Idle and Active cycles. Each device cycle is made up of a number of states. The Am9517 can assume seven separate states, each composed of one full clock period. State I (SI) is the inactive state. It is entered when the Am9517 has no valid DMA requests pending. While in SI, the DMA controller is inactive but may be in the Program Condition, being programmed by the processor. State 0 (S0) is the first state of a DMA service. The Am9517 has requested a hold but the processor has not yet returned an acknowledge. An acknowledge from the CPU will signal that transfers may begin. S1, S2, S3 and S4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (SW) can be inserted between S2 or S3 and S4 by the use of the Ready line on the Am9517.

Memory-to-memory transfers require a read-from and a write-to-memory to complete each transfer. The states, which resemble the normal working states, use two digit numbers for identification. Eight states are required for a single transfer. The first four states (S11, S12, S13, S14) are used for the read-from-memory half and the last four states (S21, S22, S23 and S24) for the write-to-memory half of the transfer.

IDLE CYCLE

When no channel is requesting service, the Am9517 will enter the Idle cycle and perform "SI" states. In this cycle the Am9517 will sample the DREQ lines every clock cycle to determine if any channel is requesting a DMA service. The device will also sample $\overline{\text{CS}}$, looking for an attempt by the microprocessor to write or read the internal registers of the Am9517. When $\overline{\text{CS}}$ is low and HREQ is low the Am9517 enters the Program Condition. The CPU can now establish, change or inspect the internal definition of the part by reading from or writing to the internal registers. Address lines A0-A3 are inputs to the device and select which registers will be read or written. The $\overline{\text{IOR}}$ and $\overline{\text{IOW}}$ lines are used to select and time reads or writes. Due to the number and size of the internal registers, an internal flip/flop is used to generate an additional bit of address. This bit is used to determine the upper or lower byte of the 16-bit Address and Word Count registers. The flip/flop is reset by Master Clear or Reset. A separate software command can also reset this flip/flop.

Special software commands can be executed by the Am9517 in the Program Condition. These commands are decoded as sets of addresses with $\overline{CS}$ and $\overline{IOW}$. The commands do not make use of the data bus. Instructions include Clear First/Last Flip/Flop and Master Clear.

ACTIVE CYCLE

When the Am9517 is in the Idle cycle and a channel requests a DMA service, the device will output a HREQ to the microprocessor and enter the Active cycle. It is in this cycle that the DMA service will take place, in one of four modes:

Single Transfer Mode: In Single Transfer mode the device is programmed to make one transfer only. The word count will be decremented and the address decremented or incremented following each transfer. When the word count goes to zero a Terminal Count (TC) will cause an Autoinitialize if the channel has been programmed to do so.

DREQ must be held active until DACK becomes active in order to be recognized. If DREQ is held active throughout the single transfer, HREQ will go inactive and release the bus to the system. It will again go active and upon receipt of a new HACK another single transfer will be performed. In 8080A/9080A systems this will ensure one full machine cycle execution between DMA transfers. Details of timing between the Am9517 and other bus control protocols will depend upon the characteristics of the microprocessor involved.

Block Transfer Mode: In Block Transfer mode the device is activated by DREQ to continue making transfers during the service until a TC, caused by the word count going to zero, or an external End of Process ($\overline{EOP}$) is encountered. DREQ need only be held active until DACK becomes active. Again an Autoinitialize will occur at the end of the service if the channel has been programmed for it.

Demand Transfer Mode: In Demand Transfer mode the device is programmed to continue making transfers until a TC or external $\overline{EOP}$ is encountered or until DREQ goes inactive. Thus transfers may continue until the I/O device has exhausted its data capacity. After the I/O device has had a chance to catch up, the DMA service is re-established by means of a DREQ. During the time between services when the microprocessor is allowed to operate, the intermediate values of address and word count are stored in the Am9517 Current Address and Current Word Count registers. Only an $\overline{EOP}$ can cause an Autoinitialize at the end of the service. $\overline{EOP}$ is generated either by TC or by an external signal.

Cascade Mode: This mode is used to cascade more than one Am9517 together for simple system expansion. The HREQ and HACK signals from the additional Am9517 are connected to the DREQ and DACK signals of a channel of the initial Am9517. This allows the DMA requests of the additional device to propagate through the priority network circuitry of the preceding device. The priority chain is preserved and the new device must wait for its turn to acknowledge requests. Since the cascade channel in the initial device is used only for prioritizing the additional device, it does not output any address or control signals of its own. These would conflict with the outputs of the active channel in the added device. The Am9517 will respond to DREQ with DACK but all other outputs except HREQ will be disabled.

Figure 3 shows two additional devices cascaded into an initial device using two of the previous channels. This forms a two level DMA system. More Am9517s could be added at the second level by using the remaining channels of the first level. Additional devices can also be added by cascading into the channels of the second level devices forming a third level.

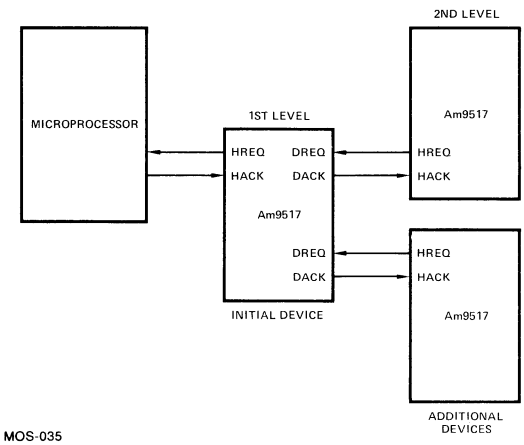


Figure 3. Cascaded Am9517s.

TRANSFER TYPES

Each of the three active transfer modes can perform three different types of transfers. These are Read, Write and Verify. Write transfers move data from an I/O device to the memory by activating $\overline{MEMW}$ and $\overline{IOR}$. Read transfers move data from memory to an I/O device by activating MEMR and IOW. Verify transfers are pseudo transfers. The Am9517 operates as in Read or Write transfers generating addresses, and responding to $\overline{EOP}$, etc. However, the memory and I/O control lines all remain inactive.

Memory-to-Memory: To perform block moves of data from one memory address space to another with a minimum of program effort and time, the Am9517 includes memory-to-memory transfer feature. Programming a bit in the Command register selects channels 0 and 1 to operate as memory-to-memory transfer channels. The transfer is initiated by setting the software DREQ for channel 0. The Am9517 requests a DMA service in the normal manner. After HACK is true, the device, using eight-state transfers in Block Transfer mode, reads data from the memory. The channel 0 Current Address register is the source for the address used and is decremented or incremented in the normal manner. The data byte read from the memory is stored in the Am9517 internal Temporary register. Channel 1 then writes the data from the Temporary register to memory using the address in its Current Address register and incrementing or decrementing it in the normal manner. The channel 1 Current Word Count is decremented. When the word count of channel 1 goes to zero, a TC is generated causing an $\overline{EOP}$ output terminating the service.

Channel 0 may be programmed to retain the same address for all transfers. This allows a single word to be written to a block of memory.

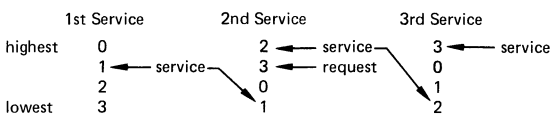
The Am9517 will respond to external $\overline{EOP}$ signals during memory-to-memory transfers. Data comparators in block search schemes may use this input to terminate the service when a match is found. The timing of memory-to-memory transfers is found in Diagram 4.

Autoinitialize: By programming a bit in the Mode register a channel may be set up as an Autoinitialize channel. During Auto-

initialization, the original values of the Current Address and Current Word Count registers are automatically restored from the Base Address and Base Word Count registers of that channel following $\overline{EOP}$. The base registers are loaded simultaneously with the current registers by the microprocessor and remain unchanged throughout the DMA service. The mask bit is not set when the channel is in Autoinitialize. Following Autoinitialize the channel is ready to perform another service without CPU intervention.

Priority: The Am9517 has two types of priority encoding available as software selectable options. The first is Fixed Priority which fixes the channels in priority order based upon the descending value of their number. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel, 0. After the recognition of any one channel for service, the other channels are prevented from interfering with that service until it is complete.

The second scheme is Rotating Priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly.



With Rotating Priority in a single chip DMA system, any device requesting service is guaranteed to be recognized after no more than three higher priority services have occurred. This prevents any one channel from monopolizing the system.

Compressed Timing: In order to achieve even greater throughput where system characteristics permit, the Am9517 can compress the transfer time to two clock cycles. From Timing Diagram 3 it can be seen that state S3 is used to extend the access time of the read pulse. By removing state S3 the read pulse width is made equal to the write pulse width and a transfer consists only of state S2 to change the address and state S4 to perform the read/write. S1 states will still occur when A8-A15 need updating (see Address Generation). Timing for compressed transfers is found in Diagram 6.

Address Generation: In order to reduce pin count, the Am9517 multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch from which they may be placed on the address bus. The falling edge of Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through a three-state enable. The lower order address bits are output by the Am9517 directly. Lines A0-A7 should be connected to the address bus. Timing Diagram 3 shows the time relationships between CLK, AEN, ADSTB, DB0-DB7 and A0-A7.

During Block and Demand Transfer mode services which include multiple transfers, the addresses generated will be sequential. For many transfers the data held in the external address latch will remain the same. This data need only change when a carry or borrow from A7 to A8 takes place in the normal sequence of addresses. To save time and speed transfers, the Am9517 executes S1 states only when updating of A8-A15 in the latch is necessary. This means for long services, S1 states may occur only once every 256 transfers, a savings of 255 clock cycles for each 256 transfers.

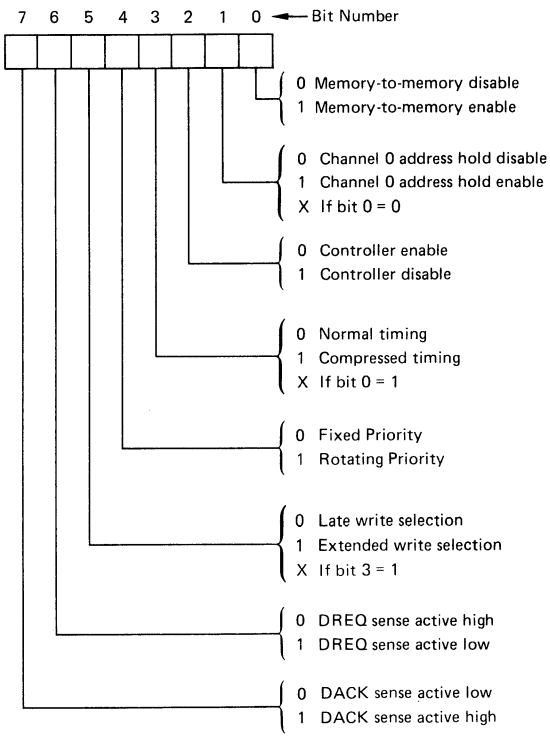
REGISTER DESCRIPTION

Current Address Register: Each channel has a 16-bit Current Address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the Current Address register during the transfer. This register is written or read by the microprocessor in successive 8-bit bytes. It may also be reinitialized by an Autoinitialize back to its original value. Autoinitialization takes place only after an $\overline{EOP}$.

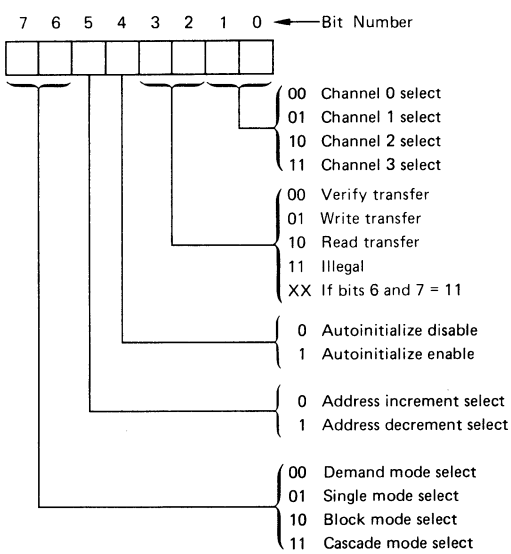
Current Word Count Register: Each channel has a 16-bit Current Word Count register. This register holds the number of transfers to be performed. The word count is decremented after each transfer. The intermediate value of the word count is stored in the register during the transfer. When the value in the register goes to zero, a TC will be generated. This register is loaded or read in successive 8-bit bytes by the microprocessor in the Program Condition. Following the end of a DMA service it may also be reinitialized by an Autoinitialize back to its original value. Autoinitialize can occur only when an $\overline{EOP}$ occurs.

Base Address and Base Word Count Registers: Each channel has a pair of Base Address and Base Word Count registers. These 16-bit registers store the original values of their associated current registers. During Autoinitialize these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register in 8-bit bytes in the Program Condition by the microprocessor. These registers cannot be read by the microprocessor.

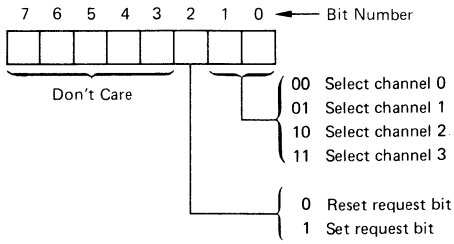
Command Register: This 8-bit register controls the operation of the Am9517. It is programmed by the microprocessor in the Program Condition and is cleared by Reset. The following table lists the function of the command bits. See Figure 6 for address coding.



Mode Register: Each channel has a 6-bit Mode register associated with it. When the register is being written to by the microprocessor in the Program Condition, bits 0 and 1 determine which channel Mode register is to be written.

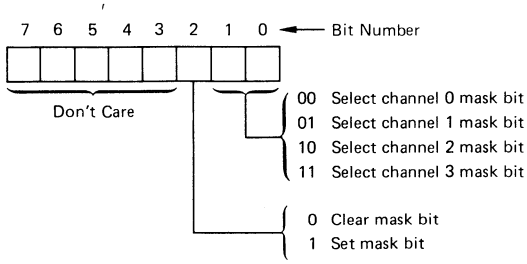


Request Register: The Am9517 can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the four bit Request register. These are nonmaskable and subject to prioritization by the Priority Encoder network. Each register bit is set or reset separately under software control or is cleared upon generation of a TC or external $\overline{EOP}$. The entire register is cleared by a Reset. To set or reset a bit, the software loads the proper form of the data word. See Figure 4 for address coding.

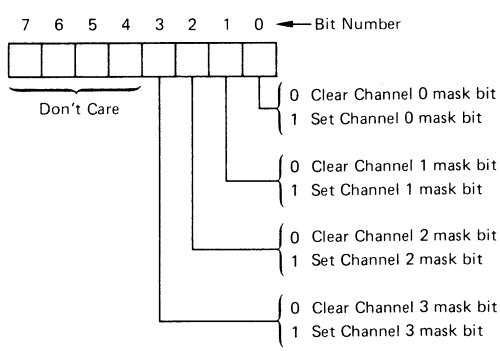


Software requests will be serviced only if the channel is in Block mode. When initiating a memory-to-memory transfer, the software request for channel 0 should be set.

Mask Register: Each channel has associated with it a mask bit which can be set to disable the incoming DREQ. Each mask bit is set when its associated channel produces an $\overline{EOP}$ if the channel is not programmed for Autoinitialize. Each bit of the four bit Mask register may also be set or cleared separately under software control. The entire register is also set by a Reset. This disables all DMA requests until a clear Mask register instruction allows them to occur. The instruction to separately set or clear the mask bits is similar in form to that used with the Request register. See Figure 4 for instruction addressing.



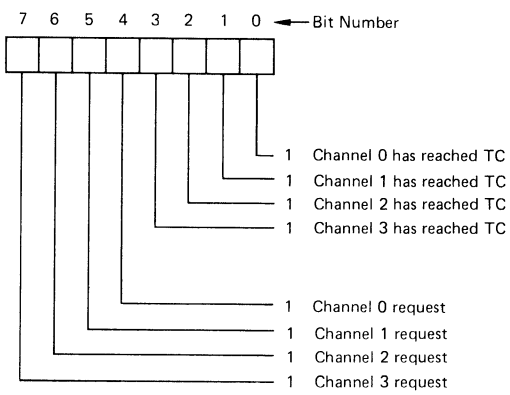
All four bits of the Mask register may also be written with a single command.



Register	Operation	Signals						
		$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0
Command	Write	0	1	0	1	0	0	0
Mode	Write	0	1	0	1	0	1	1
Request	Write	0	1	0	1	0	0	1
Mask	Set/Reset	0	1	0	1	0	1	0
Mask	Write	0	1	0	1	1	1	1
Temporary	Read	0	0	1	1	1	0	1
Status	Read	0	0	1	1	0	0	0

Figure 4. Definition of Register Codes.

Status Register: The Status register is available to be read out of the Am9517 by the microprocessor. It contains information about the status of the device at that point. This information includes which channels have reached a terminal count and which channels have pending DMA requests. Bits 0-3 are set every time a TC is reached by that channel. These bits are cleared upon Reset and on each Status Read. Bits 4-7 are set whenever their corresponding channel is requesting service.



Temporary Register: The Temporary register is used to hold data during memory-to-memory transfers. Following the completion of the transfers, the last word moved can be read by the microprocessor in the Program Condition. The Temporary register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a Reset.

Software Commands: These are additional special software commands which can be executed in the Program Condition. They do not depend on any specific bit pattern on the data bus. The two software commands are:

Clear First/Last Flip/Flop: This command is executed prior to writing or reading new address or word count information to the Am9517. This initializes the flip/flop to a known state so that subsequent accesses to register contents by the microprocessor will address upper and lower bytes in the correct sequence.

Master Clear: This software instruction has the same effect as the hardware Reset. The Command, Status, Request, Temporary, and Internal First/Last Flip/Flop registers are cleared and the Mask register is set. The Am9517 will enter the Idle cycle.

Figure 5 lists the address codes for the software commands.

Operation	Registers Affected	Signals						
		$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0
Clear FF	Internal First/Last Flip/Flop	0	1	0	1	1	0	0
Master Clear	Clear: Command Status Request Temporary Internal First/Last Flip/Flop Set: Mask	0	1	0	1	1	0	1

Figure 5. Software Command Codes.

Channel	Register	Operation	Signals							Internal Flip/Flop	Data Bus DB0–DB7
			$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0		
0	Base & Current Address	Write	0	1	0	0	0	0	0	0	A0-A7
			0	1	0	0	0	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	0	0	0	A0-A7
			0	0	1	0	0	0	0	1	A8-A15
	Base & Current Word Count	Write	0	1	0	0	0	0	1	0	W0-W7
			0	1	0	0	0	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	0	1	0	W0-W7
			0	0	1	0	0	0	1	1	W8-W15
1	Base & Current Address	Write	0	1	0	0	0	1	0	0	A0-A7
			0	1	0	0	0	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	1	0	0	A0-A7
			0	0	1	0	0	1	0	1	A8-A15
	Base & Current Word Count	Write	0	1	0	0	0	1	1	0	W0-W7
			0	1	0	0	0	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	1	1	0	W0-W7
			0	0	1	0	0	1	1	1	W8-W15
2	Base & Current Address	Write	0	1	0	0	1	0	0	0	A0-A7
			0	1	0	0	1	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	0	0	0	A0-A7
			0	0	1	0	1	0	0	1	A8-A15
	Base & Current Word Count	Write	0	1	0	0	1	0	1	0	W0-W7
			0	1	0	0	1	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	0	1	0	W0-W7
			0	0	1	0	1	0	1	1	W8-W15
3	Base & Current Address	Write	0	1	0	0	1	1	0	0	A0-A7
			0	1	0	0	1	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	1	0	0	A0-A7
			0	0	1	0	1	1	0	1	A8-A15
	Base & Current Word Count	Write	0	1	0	0	1	1	1	0	W0-W7
			0	1	0	0	1	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	1	1	0	W0-W7
			0	0	1	0	1	1	1	1	W8-W15

Figure 6. Word Count and Address Register Command Codes.

MAXIMUM RATINGS above which useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
VCC with Respect to VSS	−0.5V to +7.0V
All Signal Voltages with Respect to VSS	−0.5V to +7.0V
Power Dissipation	1.5W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	T_A	VCC
Am9517DC	0°C to +70°C	5.0V ±5%
Am9517-1DC	0°C to +70°C	5.0V ±5%
Am9517-4DC	0°C to +70°C	5.0V ±5%
Am9517DM	−55°C to +125°C	5.0V ±10%

ELECTRICAL CHARACTERISTICS over operating range (Note 1)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
VOH	Output HIGH Voltage	IOH = −200μA	2.4			Volts
		IOH = −100μA, (HREQ Only)	3.3			
VOL	Output LOW Voltage	IOL = 3.2mA			0.4	Volts
VIH	Input HIGH Voltage		2.0		VCC+0.5	Volts
VIL	Input LOW Voltage		−0.5		0.8	Volts
IIX	Input Load Current	VSS ≤ VI ≤ VCC	−10		+10	μA
IOZ	Output Leakage Current	VCC ≤ VO ≤ VSS+.40	−10		+10	μA
ICC	VCC Supply Current	T_A = +25°C		65	130	mA
		T_A = 0°C		75	150	
		T_A = −55°C			175	
CO	Output Capacitance	fc = 1.0MHz, Inputs = 0V		4	8	pF
CI	Input Capacitance			8	15	pF
CIO	I/O Capacitance			10	18	pF

NOTES:

1. Typical values are for T_A = 25°C, nominal supply voltage and nominal processing parameters.
2. Input timing parameters assume transition times of 20ns or less. Waveform measurement points for both input and output signals are 2.0V for High and 0.8V for Low, unless otherwise noted.
3. Output loading is 1 TTL gate plus 50pF capacitance unless noted otherwise.
4. The net $\overline{IOW}$ or $\overline{MEMW}$ pulse width for normal write will be TCY-100ns and for extended write will be 2TCY-100ns. The net $\overline{IOR}$ or $\overline{MEMR}$ pulse width for normal read will be 2TCY-50ns and for compressed read will be TCY-50ns.
5. TDQ is specified for two different output HIGH levels. TDQ1 is measured at 2.0V. TDQ2 is measured at 3.3V. The value for TDQ2 assumes an external 3.3kΩ pull-up resistor connected from HREQ to VCC.
6. DREQ should be held active until DACK is returned.
7. DREQ and DACK signals may be active high or active low. Timing diagrams assume the active high mode.
8. Output loading on the data bus is 1 TTL gate plus 100pF capacitance.
9. Successive read and/or write operations by the external processor to program or examine the controller must be timed to allow at least 600ns for the Am9517 or Am9517-1 and at least 450ns for the Am9517-4 as recovery time between active read or write pulses.
10. Parameters are listed in alphabetical order.
11. Pin 5 is an input that should always be at a logic high level. An internal pull-up resistor will establish a logic high when the pin is left floating. Alternatively, pin 5 may be tied to VCC.

SWITCHING CHARACTERISTICS

ACTIVE CYCLE (Notes 2, 3 and 11)

Parameter	Description	Am9517 Min.	Am9517 Max.	Am9517-1 Min.	Am9517-1 Max.	Am9517-4 Min.	Am9517-4 Max.	Unit
TAEL	AEN HIGH from CLK LOW (S1) Delay Time		300		300		225	ns
TAET	AEN LOW from CLK HIGH (S1) Delay Time		200		200		150	ns
TAFAB	ADR Active to Float Delay from CLK HIGH		150		150		120	ns
TAFC	$\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ Float from CLK HIGH		150		150		120	ns
TAFDB	DB Active to Float Delay from CLK HIGH		250		250		190	ns
TAHR	ADR from $\overline{\text{READ}}$ HIGH Hold Time	TCY-100		TCY-100		TCY-100		ns
TAHS	DB from ADSTB LOW Hold Time	50		50		40		ns
TAHW	ADR from $\overline{\text{WRITE}}$ HIGH Hold Time	TCY-50		TCY-50		TCY-50		ns
TAK	DACK Valid from CLK LOW Delay Time		250		250		190	ns
	$\overline{\text{EOP}}$ HIGH from CLK HIGH Delay Time		250		250		190	ns
	$\overline{\text{EOP}}$ LOW to CLK HIGH Delay Time		250		250		190	ns
TASM	ADR Stable from CLK HIGH		250		250		190	ns
TASS	DB to ADSTB LOW Setup Time	100		100		100		ns
TCH	Clock High Time (Transitions $\leq$ 10ns)	120		120		100		ns
TCL	Clock Low Time (Transitions $\leq$ 10ns)	150		150		110		ns
TCY	CLK Cycle Time	320		320		250		ns
TDCL	CLK HIGH to $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ LOW Delay (Note 4)		270		270		200	ns
TDCTR	$\overline{\text{READ}}$ HIGH from CLK HIGH (S4) Delay Time (Note 4)		270		270		210	ns
TDCTW	$\overline{\text{WRITE}}$ HIGH from CLK HIGH (S4) Delay Time (Note 4)		200		200		150	ns
TDQ1	HREQ Valid from CLK HIGH Delay Time (Note 5)		160		160		120	ns
TDQ2			250		250		190	ns
TEPS	$\overline{\text{EOP}}$ LOW from CLK LOW Setup Time	60		60		45		ns
TEPW	$\overline{\text{EOP}}$ Pulse Width	300		300		225		ns
TFAAB	ADR Float to Active Delay from CLK HIGH		250		250		190	ns
TFAC	$\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ Active from CLK HIGH		200		200		150	ns
TFADB	DB Float to Active Delay from CLK HIGH		300		300		225	ns
THS	HACK valid to CLK HIGH Setup Time	100		100		75		ns
TIDH	Input Data from $\overline{\text{MEMR}}$ HIGH Hold Time	0		0		0		ns
TIDS	Input Data to $\overline{\text{MEMR}}$ HIGH Setup Time	250		250				ns
TODH	Output Data from $\overline{\text{MEMW}}$ HIGH Hold Time	20		20				ns
TODV	Output Data Valid to $\overline{\text{MEMW}}$ HIGH	200		200				ns
TQS	DREQ to CLK LOW (S1, S4) Setup Time	120		120		90		ns
TRH	CLK to READY LOW Hold Time	20		20		20		ns
TRS	READY to CLK LOW Setup Time	100		100		60		ns
TSTL	ADSTB HIGH from CLK HIGH Delay Time		200		200		150	ns
TSTT	ADSTB LOW from CLK HIGH Delay Time		140		140		110	ns

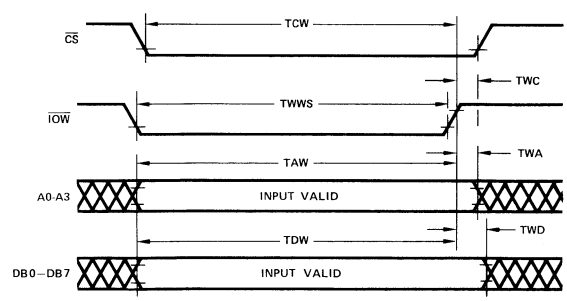
SWITCHING CHARACTERISTICS

PROGRAM CONDITION (IDLE CYCLE)

(Notes 2, 3, 10 and 11)

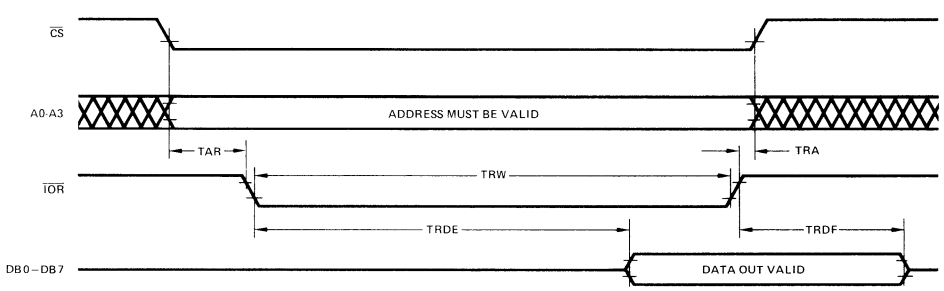
Parameter	Description	Am9517 Min.	Am9517 Max.	Am9517-1 Min.	Am9517-1 Max.	Am9517-4 Min.	Am9517-4 Max.	Unit
TAR	ADR Valid or $\overline{CS}$ LOW to $\overline{READ}$ LOW	50		50		50		ns
TAW	ADR Valid to $\overline{WRITE}$ HIGH Setup Time	200		200		150		ns
TCW	$\overline{CS}$ LOW to $\overline{WRITE}$ HIGH Setup Time	200		200		150		ns
TDW	Data Valid to $\overline{WRITE}$ HIGH Setup Time	200		200		150		ns
TRA	ADR or $\overline{CS}$ Hold from $\overline{READ}$ HIGH	0		0		0		ns
TRDE	Data Access from $\overline{READ}$ LOW (Note 8)		300		200		150	ns
TDRF	DB Float Delay from $\overline{READ}$ HIGH	20	150	20	100	20	100	μs
TRSTD	Power Supply HIGH to RESET LOW Setup Time	500		500		500		ns
TRSTS	RESET to First $\overline{IOWR}$	2		2		2		TCY
TRSTW	RESET Pulse Width	300		300		300		ns
TRW	$\overline{READ}$ Width	300		300		250		ns
TWA	ADR from $\overline{WRITE}$ HIGH Hold Time	20		20		20		ns
TWC	$\overline{CS}$ HIGH from $\overline{WRITE}$ HIGH Hold Time	20		20		20		ns
TWD	Data from $\overline{WRITE}$ HIGH Hold Time	30		30		30		ns
TWWS	Write Width	200		200		200		ns

SWITCHING WAVEFORMS



Timing Diagram 1. Program Condition Write Timing.

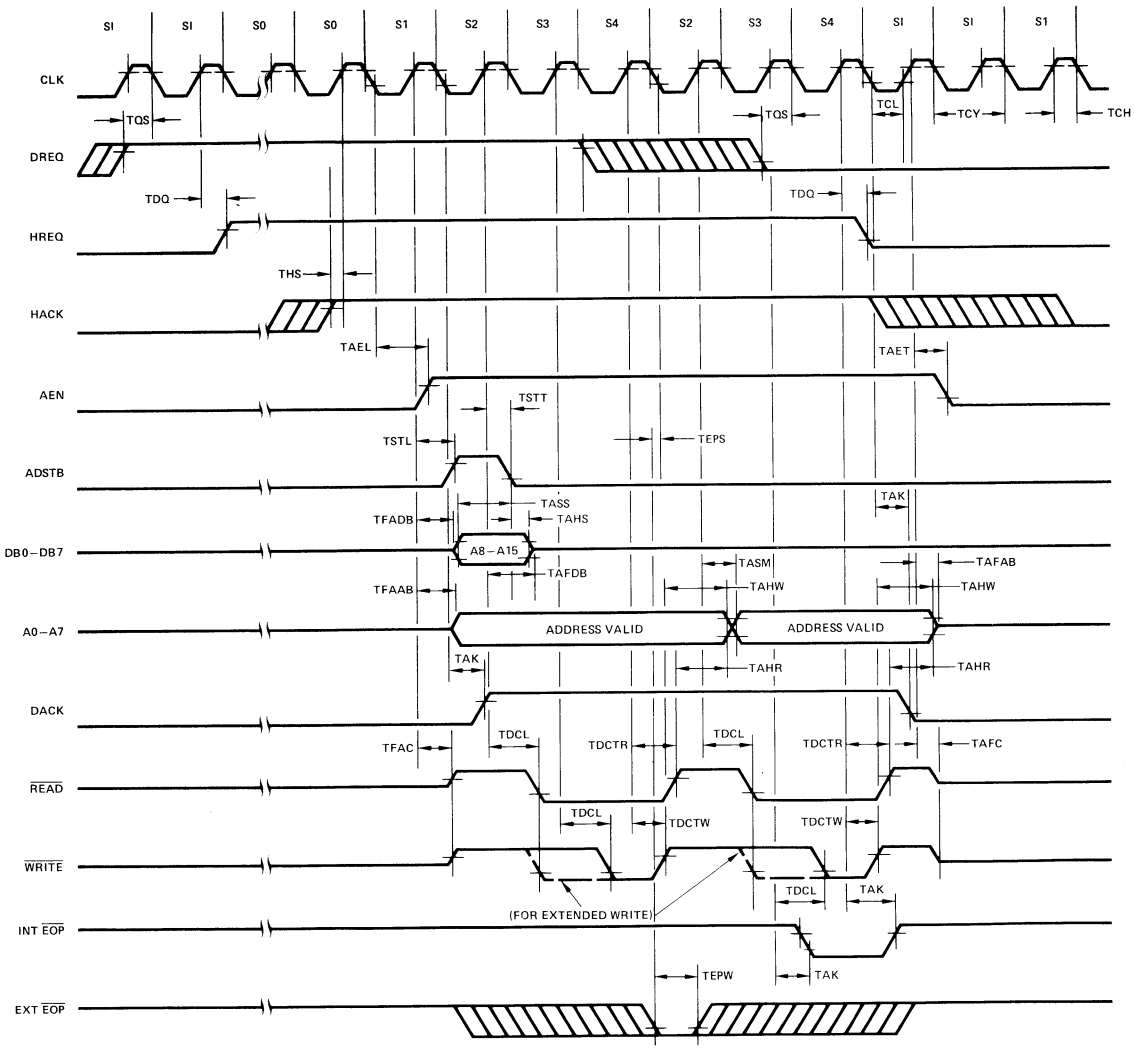
MOS-036



Timing Diagram 2. Program Condition Read Cycle.

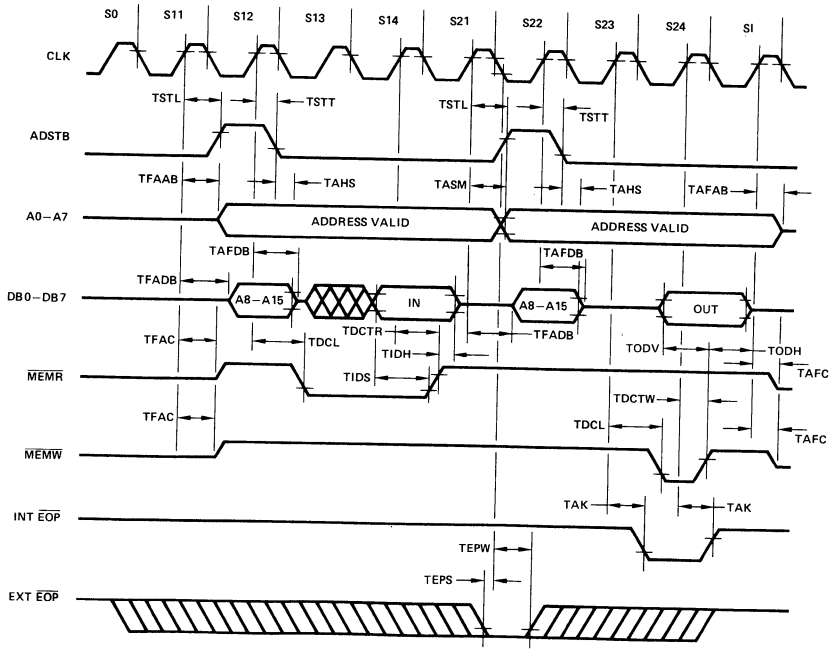
MOS-037

SWITCHING WAVEFORMS (Cont.)



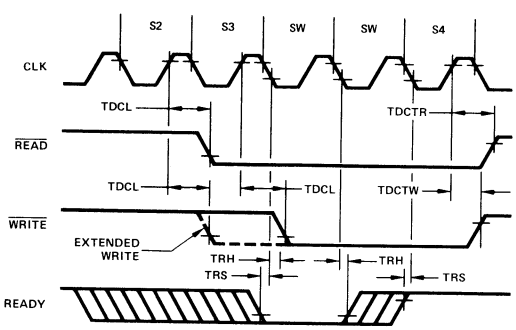
Timing Diagram 3. Active Cycle Timing Diagram.

MOS-038



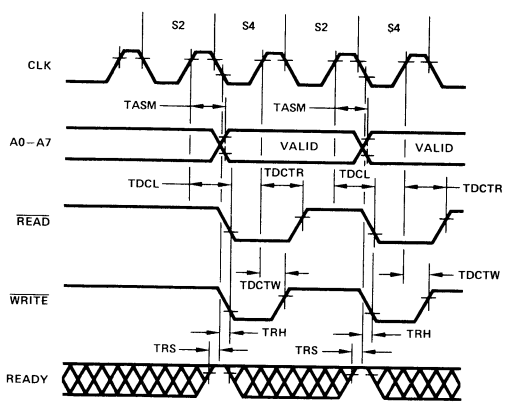
Timing Diagram 4. Memory-to-Memory.

MOS-039



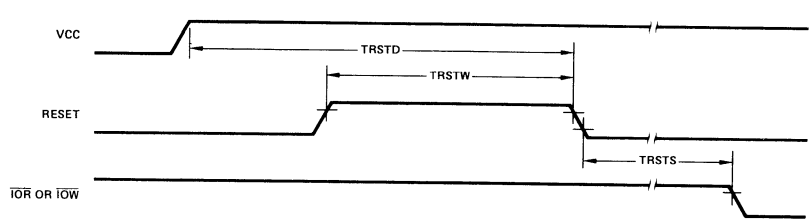
Timing Diagram 5. Ready Timing.

MOS-040



Timing Diagram 6. Compressed Timing.

MOS-041



Timing Diagram 7. Reset Timing.

MOS-042

APPLICATION INFORMATION

Figure 7 shows a convenient method for configuring a DMA system with the Am9517 Controller and an 8080A/9080A microprocessor system. The Multimode DMA Controller issues a Hold Request to the processor whenever there is at least one valid DMA Request from a peripheral device. When the processor replies with a Hold Acknowledge signal, the Am9517 takes control of the Address Bus, the Data Bus and the Control Bus. The address for the first transfer operation comes out in two bytes – the least significant eight bits on the eight Address outputs and the most significant eight bits on the Data Bus. The contents of the Data Bus are then latched into the Am74LS373 register to complete the full 16 bits of the Address Bus. The Am74LS373 is a high speed, low power, 8-bit, three-state register in a 20 pin package. After the initial transfer takes place, the register is updated only after a carry or borrow is generated in the least significant address byte. Four DMA channels are provided when one Am9517 is used.

In the example system configuration shown in Figure 8 the Am9517 is used to handle data transfers between the Am9511 arithmetic processing unit and the system memory. These transfers may be operands, commands, or results. Although the CPU must initialize the DMA operations, it is still much more efficient than performing the same transfers under programmed I/O. The Am9519 interrupt controller shown in Figure 8 also enhances the system throughput by allowing concurrent CPU and APU operations, and simplifying coordination between the two units.

Figure 9 shows one method to expand the number of DMA channels available. A second Am9517 chip is attached to one of the initial DMA channels providing a net capacity of 7 channels. Both DMA chips share the same external 8-bit latch. Any channel on any Am9517 may be used for such expansions.

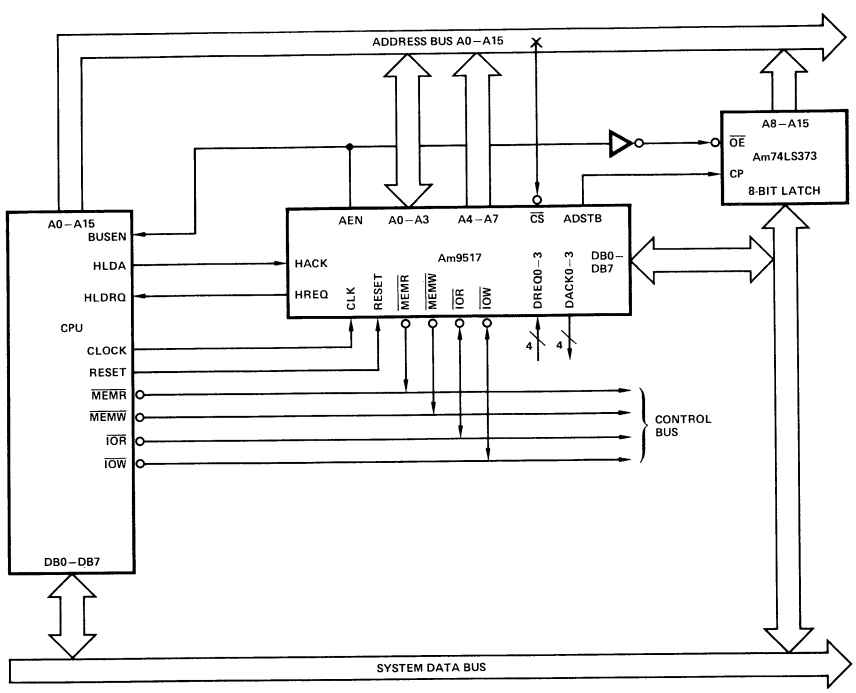


Figure 7. Basic DMA Configuration.

MOS-043

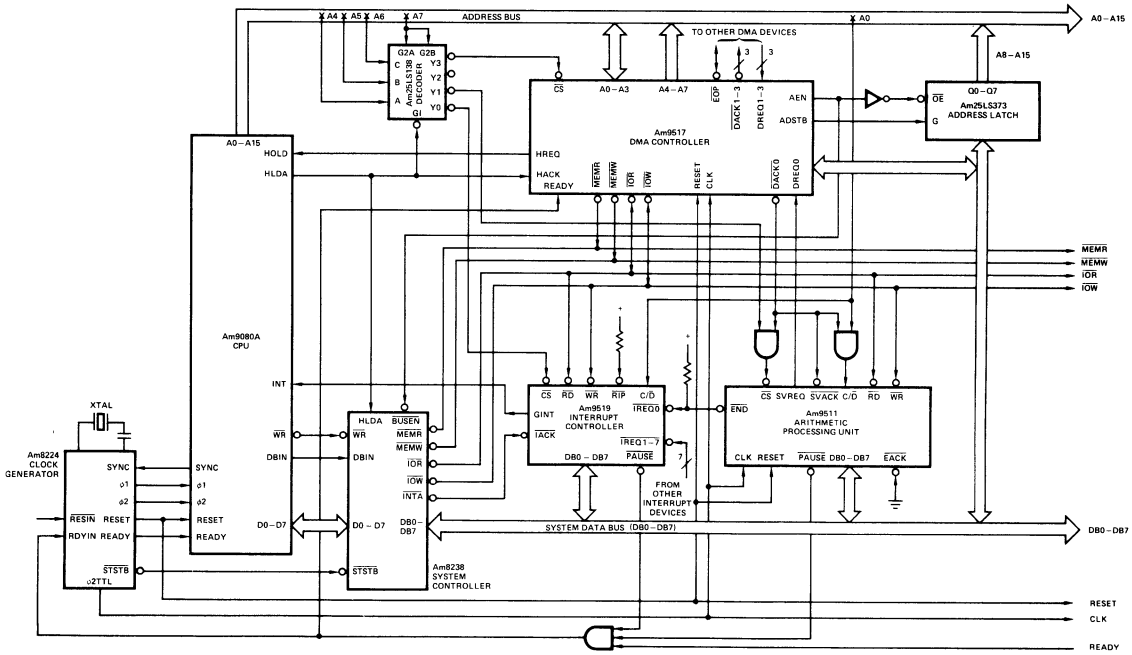


Figure 8. Am9517 Typical Application Example.

MOS-044

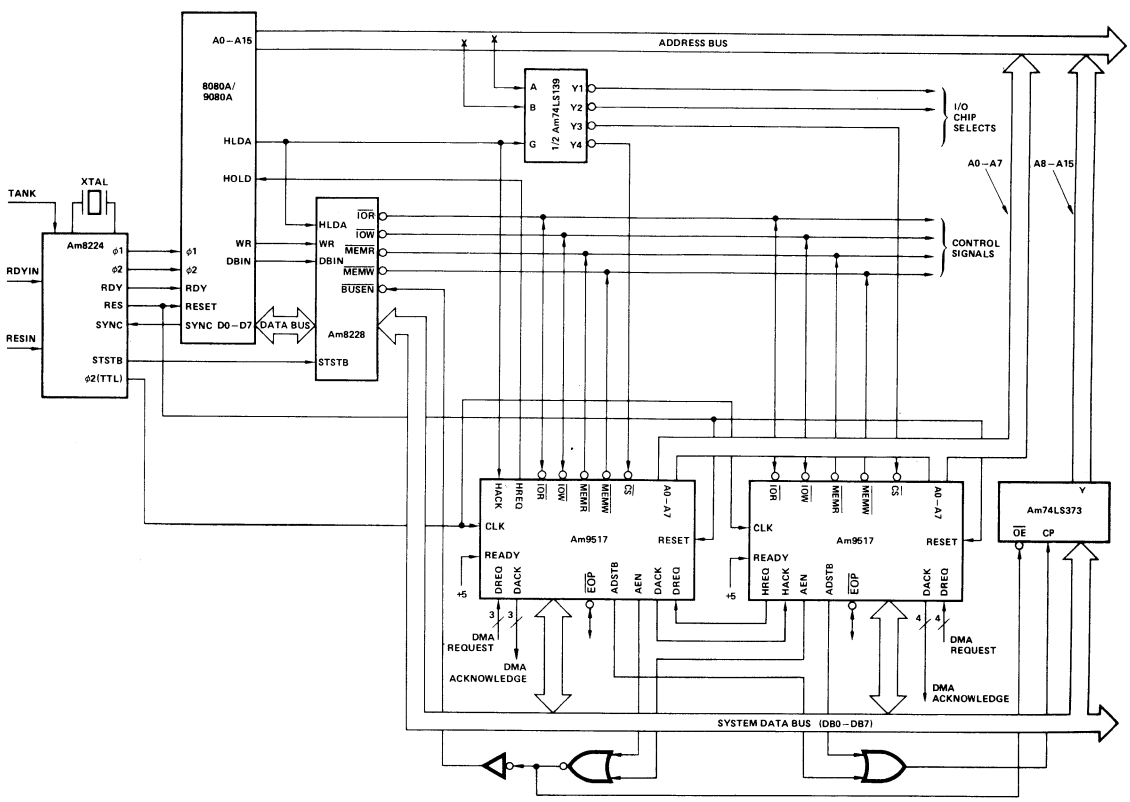
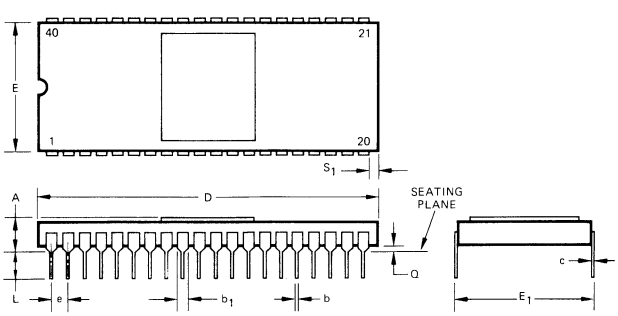


Figure 9. Expanded Am9517 Configuration.

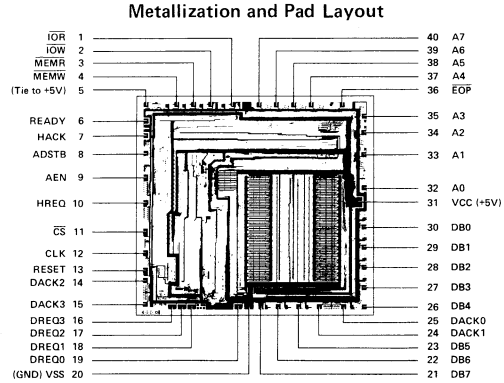
MOS-045

PHYSICAL DIMENSIONS
40-Pin Hermetic DIP



Reference Symbol	Inches	
	Min.	Max.
A	.100	.200
b	.015	.022
b_1	.030	.060
c	.008	.013
D	1.960	2.040
E	.550	.610
E_1	.590	.620
e	.090	.110
L	.120	.160
Q	.020	.060
S_1	.005	

Metallization and Pad Layout



DIE SIZE
0.198" X 0.210"

Am9519
Universal Interrupt Controller

DISTINCTIVE CHARACTERISTICS

- Eight individually maskable interrupt inputs
- Software interrupt request capability
- Fully programmable 1, 2, 3 or 4 byte responses
- Unlimited daisy-chain expansion capability
- Fixed or rotating priority resolution
- Common vector option
- Polled mode option
- Optional automatic clearing of acknowledged interrupts
- Bit set/reset capability for Mask register
- Master Mask bit disables all interrupts
- Pulse-catching interrupt input circuitry
- Polarity control of interrupt inputs and output
- Various timing options including 8085A compatible Am9519-1
- Single +5V supply
- 100% MIL-STD-883 reliability assurance testing

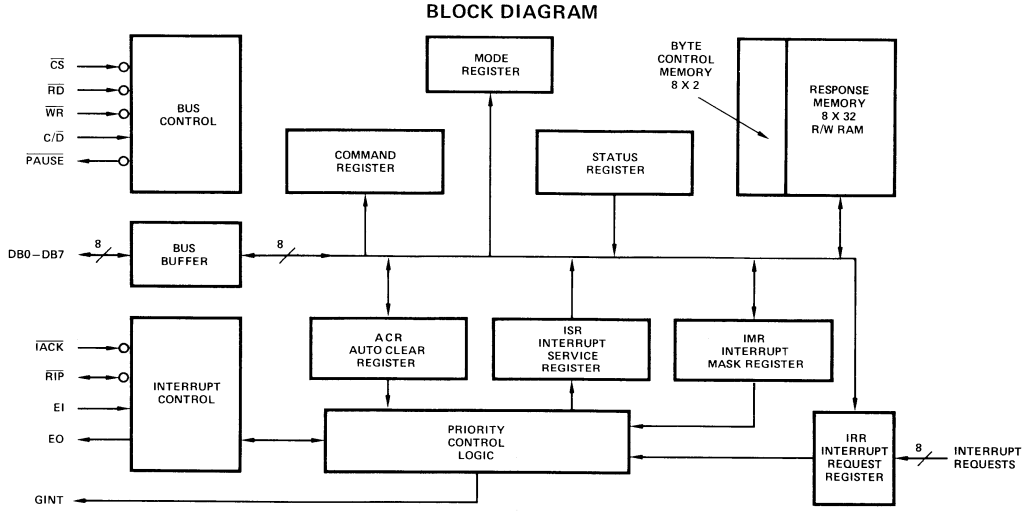
GENERAL DESCRIPTION

The Am9519 Universal Interrupt Controller is a processor support circuit that provides a powerful interrupt structure to increase the efficiency and versatility of microcomputer-based systems. A single Am9519 manages up to eight maskable interrupt request inputs, resolves priorities and supplies up to four bytes of fully programmable response for each interrupt. It uses a simple expansion structure that allows many units to be cascaded for control of large numbers of interrupts. Several programmable control features are provided to enhance system flexibility and optimization.

The Universal Interrupt Controller is designed with a general purpose interface to facilitate its use with a wide range of digital systems, including most popular 8-bit microprocessors. Since the response bytes are fully programmable, any instruction or vectoring protocol appropriate for the host processor may be used.

When the Am9519 controller receives an unmasked Interrupt Request, it issues a Group Interrupt output to the CPU. When the interrupt is acknowledged, the controller outputs the one-to-four byte response associated with the highest priority unmasked interrupt request. The ability of the CPU to set interrupt requests under software control permits hardware prioritization of software tasks and aids system diagnostic and maintenance procedures.

BLOCK DIAGRAM



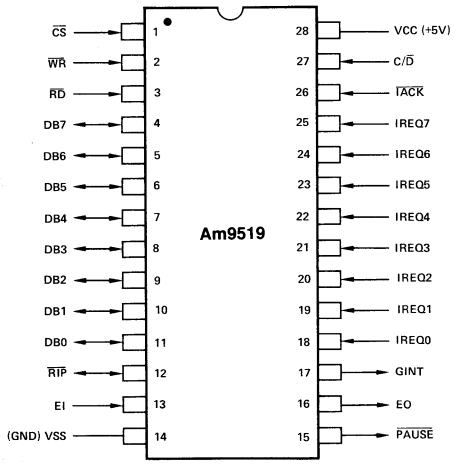
MOS-143

ORDERING INFORMATION

Package Type	Ambient Temperature	Timing Options		
		Am9519	Am9519-1	Am9519-4
Hermetic DIP*	$0°C \leq T_A \leq +70°C$	AM9519DC/CC	AM9519-1DC/CC	AM9519-4DC/CC
	$-55°C \leq T_A \leq +125°C$	AM9519DM	AM9519-1DM	
Molded DIP	$0°C \leq T_A \leq +70°C$	AM9519PC	AM9519-1PC	AM9519-4PC

*DC = Side-Brazed Ceramic CC = Cerdip

CONNECTION DIAGRAM



Top View

Pin 1 is marked for orientation.

MOS-019

INTERFACE SIGNAL DESCRIPTION

VCC: +5 Volt Power Supply
VSS: Ground

DB0 – DB7 (Data Bus, Input/Output)

The eight bidirectional data bus signals are used to transfer information between the Am9519 and the system data bus. The direction of transfer is controlled by the IACK, WR and RD input signals. Programming and control information are written into the device; status and response data are output by it.

CS (Chip Select, Input)

The active low Chip Select input enables read and write operations on the data bus. Interrupt acknowledge responses are not conditioned by CS.

RD (Read, Input)

The active low Read signal is conditioned by CS and indicates that information is to be transferred from the Am9519 to the data bus.

WR (Write, Input)

The active low Write signal is conditioned by CS and indicates that data bus information is to be transferred from the data bus to a location within the Am9519.

C/D (Control/Data, Input)

The C/D control signal selects source and destination locations for data bus read and write operations. Data read or write transfers are made to or from preselected internal registers or memory locations. Control write operations load the command register and control read operations output the status register.

IREQ0 – IREQ7 (Interrupt Request, Input)

The Interrupt Request signals are used by external devices to indicate that service by the host CPU is desired. IREQ inputs are accepted asynchronously and they may be programmed for either a high-to-low or low-to-high edge transition. Active inputs are latched internally in the Interrupt Request Register. After the IRR bit is cleared, an IREQ transition of the programmed polarity must occur to initiate another request.

RIP (Response In Process, Input/Output)

Response In Process is a bidirectional signal used when two or more Am9519 circuits are cascaded. It permits multibyte response transfers to be completed without interference from higher priority interrupts. An Am9519 that is responding to an acknowledged interrupt will treat RIP as an output and hold it low until the acknowledge response is finished. An Am9519 without an acknowledged interrupt will treat RIP as an input and will ignore IACK pulses as long as RIP is low. The RIP output is open drain and requires an external pullup resistor to VCC.

IACK (Interrupt Acknowledge, Input)

The active low Interrupt Acknowledge line indicates that the external system is asking for interrupt response information. Depending on the programmed state of the Am9519, it will accept 1, 2, 3 or 4 IACK pulses; one response byte is transferred per pulse. The first IACK pulse causes selection of the highest priority unmasked pending interrupt request and generates a RIP output signal.

PAUSE (Pause, Output)

The active-low Pause signal is used to coordinate interrupt responses with data bus and control timing. Pause goes low when the first IACK is received and remains low until RIP goes low. The external system can use Pause to stretch the acknowledge cycle and allow the control timing to automatically adjust to the actual priority resolution delays in the interrupt system. Second, third and fourth response bytes do not cause Pause to go low. Pause is an open drain output and requires an external pullup resistor to VCC.

EO (Enable Out, Output)

The active high EO signal is used to implement daisy-chained cascading of several Am9519 circuits. EO is connected to the EI input of the next lower priority chip. On receipt of an interrupt acknowledge, each EO will go inactive until it has been determined that no valid interrupt request is pending on that chip. If an active request is present, EO remains low. EO is also held low when the master mask bit is active, thus disabling all lower priority chips.

EI (Enable In, Input)

The active high EI signal is used to implement daisy-chained cascading of several Am9519 circuits. EI is connected to EO of the next higher priority chip. It may also be used as a hardware disable input for the interrupt system. When EI is low IACK inputs are ignored. EI is internally pulled up to VCC so that no external pullup is needed when EI is not used.

GINT (Group Interrupt, Output)

The Group Interrupt output signal indicates that at least one unmasked interrupt request is pending. It may be programmed for active high or active low polarity. When active low, the output is open drain and requires an external pull up resistor to VCC.

REGISTER DESCRIPTION

Interrupt Request Register (IRR): The 8-bit IRR is used to store pending interrupt requests. A bit in the IRR is set whenever the corresponding IREQ input goes active. Bits may also be set under program control from the CPU, thus permitting software generated interrupts. IRR bits may be cleared under program control. An IRR bit is automatically cleared when its interrupt is acknowledged. All IRR bits are cleared by a reset function.

Interrupt Service Register (ISR): The 8-bit ISR contains one bit for each IREQ input. It is used to indicate that a pending interrupt has been acknowledged and to mask all lower priority interrupts. When a bit is set by the acknowledge logic in the ISR, the corresponding IRR bit is cleared. If an acknowledged interrupt is not programmed to be automatically cleared, its ISR bit must be cleared by the CPU under program control when it is desired to permit interrupts from lower priority devices. When the interrupt is programmed for automatic clearing, the ISR bit is automatically reset during the acknowledge sequence. All ISR bits are cleared by a reset function.

Interrupt Mask Register (IMR): The 8-bit IMR is used to enable or disable the individual interrupt inputs. The IMR bits correspond to the IREQ inputs and all eight may be loaded, set or cleared in parallel under program control. In addition, individual IMR bits may be set or cleared by the CPU. A reset function will set all eight mask bits, disabling all requests. A mask bit that is set does not disable the IRR, and an IREQ that arrives while a corresponding mask bit is set will cause an interrupt later when the mask bit is cleared. Only unmasked interrupt inputs can generate a Group Interrupt output.

Response Memory: An 8 x 32 read/write response memory is included in the Am9519. It is used to store up to four bytes of response information for each of the eight interrupt request inputs. All bits in the memory are programmable, allowing any desired vector, opcode, instruction or other data to be entered. The Am9519 transfers the interrupt response information for the highest priority unmasked interrupt from the memory to the data bus when the $\overline{IACK}$ input is active.

Auto Clear Register: The 8-bit Auto Clear register contains one bit for each IREQ input and specifies the operating mode for each of the ISR bits. When an auto clear bit is off, the corresponding ISR bit is set when that interrupt is acknowledged and is cleared by software command. When an auto clear bit is on, the corresponding ISR bit is cleared by the hardware before the end of the acknowledge sequence. A reset function clears all auto clear bits.

Status Register: The 8-bit Status register contains information concerning the internal state of the chip. It is especially useful when operating in the polled mode in order to identify interrupting devices. Figure 1 shows the status register bit assignments. The polarity of the GINT bit 7 is not affected by the GINT polarity control (Mode bit 3). The Status register is read by executing a read operation ($\overline{CS} = 0$, $\overline{RD} = 0$) with the control location selected ($C/\overline{D} = 1$).

Mode Register: The 8-bit Mode register controls the operating options of the Am9519. Figure 2 shows the bit assignments for the Mode register. The five low order mode bits (0 through 4) are loaded in parallel by command. Bits 5, 6 and 7 are controlled by separate commands. (See Figure 4.) The Mode register cannot be read out directly to the data bus, but Mode bits 0, 2 and 7 are available as part of the Status register.

Command Register: The 8-bit Command register stores the last command entered. Depending upon the command opcode, it may initiate internal actions or precondition the part for subsequent data bus transfers. The Command register is loaded by executing a write operation ($\overline{WR} = 0$) with the control location selected ($C/\overline{D} = 1$), as shown in Figure 3.

Byte Count Register: The length in bytes of the response associated with each interrupt is independently programmed so that different interrupts may have different length responses. The byte count for each response is stored in eight 2-bit Byte Count registers. For a given interrupt the Am9519 will expect to receive a number of $\overline{IACK}$ pulses that equals the corresponding byte count, and will hold $\overline{RIP}$ low until the count is satisfied. The byte count does not control the number of bytes loaded into the response memory during initialization.

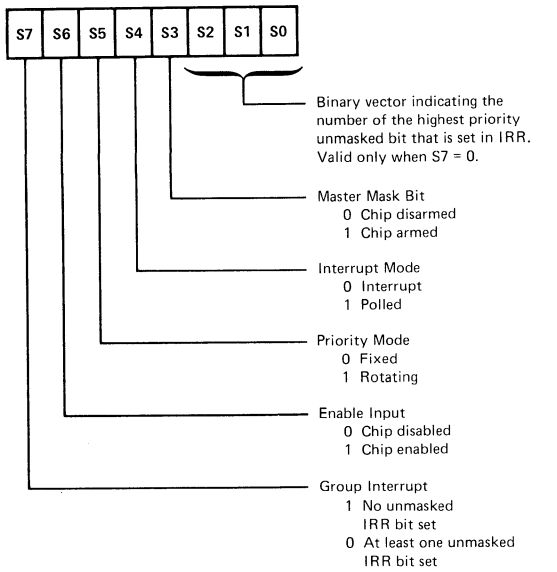


Figure 1. Status Register Bit Assignments. MOS-025

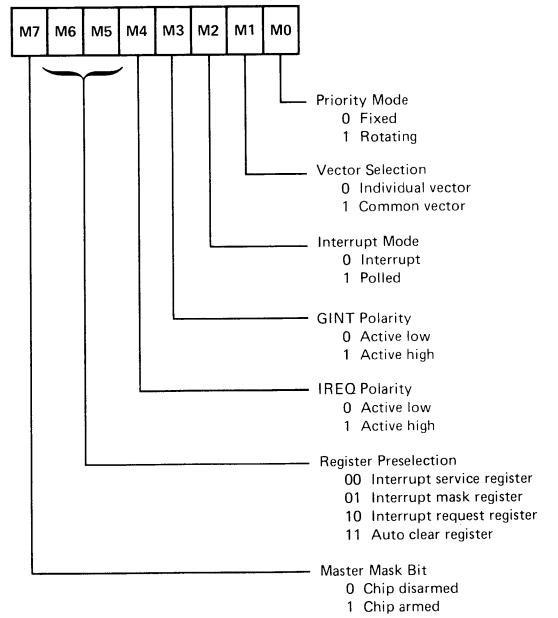


Figure 2. Mode Register Bit Assignments. MOS-026

FUNCTIONAL DESCRIPTION

Interrupts are used to improve system throughput and response time by eliminating heavy dependence on software polling procedures. Interrupts allow external devices to asynchronously modify the instruction sequence of a program being executed. In systems with multiple interrupts, vectoring can further improve performance by allowing direct identification of the interrupting device and its associated service routine. The Am9519 Universal Interrupt Controller contains, on one chip, all of the circuitry necessary to detect, prioritize and manage eight vectored interrupts. It includes many options and operating modes that permit the design of sophisticated interrupt systems.

Reset

The reset function is accomplished by software command or automatically during power-up. The reset command may be issued by the CPU at any time. Internal power up circuitry is triggered when VCC reaches a predetermined threshold, causing a brief internal reset pulse. In both cases, the resulting internal state of the machine is that all registers are cleared except the Mask register which is set. Thus no Group Interrupt will be generated and no interrupt requests will be recognized. The response memory and Byte Count registers are not affected by reset. Their contents after power-up are unpredictable and must be established by the host CPU during initialization.

Operating Sequence

A brief description of a typical sequence of events in an operating interrupt system will illustrate the general interactions among the host CPU, the interrupt controller and the interrupting peripheral.

1. The Am9519 controller is initialized by the CPU in order to customize its configuration and operation for the application at hand. Both the controller and the CPU are then enabled to accept interrupts.
2. One (or more) of the interrupt request inputs to the controller becomes active indicating that peripheral equipment is asking for service. The controller asynchronously accepts and latches the request(s).
3. If the request is masked, no further action takes place. If the request is not masked, a Group Interrupt output is generated by the controller.
4. The GINT signal is recognized by the CPU which normally will complete the execution of the current instruction, insert an interrupt acknowledge sequence into its instruction execution stream, and disable its internal interrupt structure. The controller expects to receive one or more $\overline{IACK}$ signals from the CPU during the acknowledge sequence.
5. When the controller receives the $\overline{IACK}$ signal, it brings $\overline{PAUSE}$ low and selects the highest priority unmasked pending request. When selection is complete, the $\overline{RIP}$ output is brought low and the first byte in the response memory associated with the selected request is output on the data bus. $\overline{PAUSE}$ stays low until RIP goes low. $\overline{RIP}$ stays low until the last byte of the response has been transferred.
6. During the acknowledge sequence, the IRR bit corresponding to the selected request is automatically cleared, and the corresponding ISR bit is set. When the ISR bit is set, the Group Interrupt output is disabled until a higher priority request arrives or the ISR bit is cleared. The ISR bit will be cleared by either hardware or software.
7. If a higher priority request arrives while the current request is being serviced, GINT will be output by the controller, but will be recognized and acknowledged only if the CPU has its interrupt input enabled. If acknowledged, the corresponding higher priority ISR bit will be set and the requests nested.

Information Transfers

Figure 3 shows the control signal configurations for all information transfer operations between the Am9519 and the data bus. The following conventions are assumed: $\overline{RD}$ and $\overline{WR}$ active are mutually exclusive; $\overline{RD}$, $\overline{WR}$ and C/$\overline{D}$ have no meaning unless $\overline{CS}$ is low; active $\overline{IACK}$ pulses occur only when $\overline{CS}$ is high.

For reading, the Status register is selected directly by the C/$\overline{D}$ control input. Other internal registers are read by preselecting the desired register with mode bits 5 and 6, and then executing a data read. The response memory can be read only with $\overline{IACK}$ pulses. For writing, the Command register is selected directly by the C/$\overline{D}$ control input. The Mask and Auto Clear registers are loaded following specific commands to that effect. To load each level of the response memory, the response preselect command is issued to select the desired level. An appropriate number of data write operations are then executed to load that level.

CONTROL INPUT					DATA BUS OPERATION
$\overline{CS}$	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{IACK}$	
0	0	0	1	1	Transfer contents of preselected data register to data bus
0	0	1	0	1	Transfer contents of data bus to preselected data register
0	1	0	1	1	Transfer contents of status register to data bus
0	1	1	0	1	Transfer contents of data bus to command register
1	X	X	X	0	Transfer contents of selected response memory location to data bus
1	X	X	X	1	No information transferred

Figure 3. Summary of Data Bus Transfers.

The Pause output may be used by the host CPU to ensure that proper timing relationships are maintained with the Am9519 when $\overline{IACK}$ is active. The $\overline{IACK}$ pulse width required depends on several variables, including: operating temperature, internal logic delays, number of interrupt controllers chained together, and the priority level of the interrupt being acknowledged. When delays in these variables combine to delay selection of a request following the falling edge of the first $\overline{IACK}$, the Pause output may be used to extend the $\overline{IACK}$ pulse, if necessary. Pause will remain low until a request has been selected, as indicated by the falling edge of $\overline{RIP}$. Typically, the internal interrupt selection process is quite fast, especially for systems with a single Am9519, and Pause will consequently remain low for only a very brief interval and will not cause extension of the $\overline{IACK}$ timing.

Operating Options

The Mode register specifies the various combinations of operating options that may be selected by the CPU. It is cleared by power-up or by a reset command.

Mode bit 0 specifies the rotating/fixed priority mode (see Figure 2). In the fixed mode, priority is assigned to the request inputs based upon their physical location at the chip interface, with IREQ0 the highest and IREQ7 the lowest. In the rotating mode, relative priority is the same as for the fixed mode and the most recently serviced request is assigned the lowest priority. In the fixed mode, a lower priority request might never receive service if enough higher priority requests are active. In the rotating mode, any request will receive service within a maximum of seven other service cycles no matter what pattern the request inputs follow.

Mode bit 1 selects the individual/common vector option. Individual vectoring provides a unique location in the response memory for each interrupt request. The common vector option always supplies the response associated with IREQ0 no matter which request is being acknowledged.

Mode bit 2 specifies interrupt or polled operation. In the polled mode the Group Interrupt output is disabled. The CPU may read the Status register to determine if a request is pending. Since $\overline{IACK}$ pulses are not normally supplied in polled mode, the IRR bit is not automatically cleared, but may be cleared by command. With no $\overline{IACK}$ input the ISR and the response memory are not used. An Am9519 in the polled mode has EI connected to EO so that in multichip interrupt systems the polled chip is functionally removed from the priority hierarchy.

Mode bit 3 specifies the sense of the GINT output. When active high polarity is selected the output is a two-state configuration. For active low polarity, the output is open drain and requires an external pull-up resistor to provide the high logic level. The open drain output allows wired-or configurations with other similar output signals.

Mode bit 4 specifies the sense of the IREQ inputs. When active low polarity is selected, the IRR responds to falling edges on the request inputs. When active high is selected, the IRR responds to rising edges.

Mode bits 5 and 6 specify the register that will be read on subsequent data read operations (C/$\overline{D}$ = 0, $\overline{RD}$ = 0). This preselection remains valid until changed by a reset or a command.

Mode bit 7 is the master mask bit that disables all request inputs. It is used to disable all interrupts without modifying the IMR so that the previous IMR contents are valid when interrupts are re-enabled. When the master mask bit is low, it causes the EO line to remain disabled (low). Thus, for multiple-chip interrupt systems, one master mask bit can disable the whole interrupt structure. Alternatively, portions of the structure may be disabled. The state of the master mask bit is available as bit S3 of the Status register.

Programming

After reset, the Am9519 must be initialized by the CPU in order to perform useful work. At a minimum, the master mask bit and at least one of the IMR bits should be enabled. If vectoring is to be used, the response memory must be loaded; if not, the mode must be changed to a non-vectored configuration. Normally, the first step will be to modify the Mode register and the Auto clear register in order to establish the configuraton desired for the application. Then the response memory and byte count will be loaded for those request levels that will be in use. Finally, the master mask bit and at least portions of the IMR will be enabled to allow interrupt processing to proceed.

Commands

The host CPU configures, changes and inspects the internal condition of the Am9519 using the set of commands shown in Figure 4. An "X" entry in the table indicates a "don't care" state. All commands are entered by directly loading the Command register as shown in Figure 3 ($C/\overline{D}$ = 1, $\overline{WR}$ = 0). Figure 5 shows the coding assignments for the Byte Count registers. A detailed description of each command is contained in the Am9519 Application Note AMPUB071.

BY1	BY0	COUNT
0	0	1
0	1	2
1	0	3
1	1	4

Figure 5. Byte Count Coding.

COMMAND CODE								COMMAND DESCRIPTION
7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
0	0	0	1	0	X	X	X	Clear all IRR and all IMR bits
0	0	0	1	1	B2	B1	B0	Clear IRR and IMR bit specified by B2, B1, B0
0	0	1	0	0	X	X	X	Clear all IMR bits
0	0	1	0	1	B2	B1	B0	Clear IMR bit specified by B2, B1, B0
0	0	1	1	0	X	X	X	Set all IMR bits
0	0	1	1	1	B2	B1	B0	Set IMR bit specified by B2, B1, B0
0	1	0	0	0	X	X	X	Clear all IRR bits
0	1	0	0	1	B2	B1	B0	Clear IRR bit specified by B2, B1, B0
0	1	0	1	0	X	X	X	Set all IRR bits
0	1	0	1	1	B2	B1	B0	Set IRR bit specified by B2, B1, B0
0	1	1	0	X	X	X	X	Clear highest priority ISR bit
0	1	1	1	0	X	X	X	Clear all ISR bits
0	1	1	1	1	B2	B1	B0	Clear ISR bit specified by B2, B1, B0
1	0	0	M4	M3	M2	M1	M0	Load Mode register bits 0–4 with specified pattern
1	0	1	0	M6	M5	0	0	Load Mode register bits 5, 6 with specified pattern
1	0	1	0	M6	M5	0	1	Load Mode register bits 5, 6 and set mode bit 7
1	0	1	0	M6	M5	1	0	Load Mode register bits 5, 6 and clear mode bit 7
1	0	1	1	X	X	X	X	Preselect IMR for subsequent loading from data bus
1	1	0	0	X	X	X	X	Preselect Auto Clear register for subsequent loading from data bus
1	1	1	BY1	BY0	L2	L1	L0	Load BY1, BY0 into byte count register and preselect response memory level specified by L2, L1, L0 for subsequent loading from data bus

Figure 4. Am9519 Command Summary.

MAXIMUM RATINGS above which useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
VCC with Respect to VSS	−0.5V to +7.0V
All Signal Voltages with Respect to VSS	−0.5V to +7.0V
Power Dissipation (Package Limitation)	1.5W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	VCC	VSS
Am9519DC Am9519-4DC	$0°C \leq T_A \leq +70°C$	+5.0V ± 5%	0V
Am9519DM	$-55°C \leq T_A \leq +125°C$	+5.0V ± 10%	0V

ELECTRICAL CHARACTERISTICS Over Operating Range (Note 1)

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Unit
VOH	Output High Voltage (Note 12)	IOH = −200μA		2.4			Volts
		IOH = −100μA (EO only)		2.4			
VOL	Output Low Voltage	IOL = 3.2mA				0.4	Volts
		IOL = 1.0mA (EO only)				0.4	
VIH	Input High Voltage			2.0		VCC	Volts
VIL	Input Low Voltage			−0.5		0.8	Volts
IIX	Input Load Current	VSS ≤ VIN ≤ VCC	EI Input	−60		10	μA
			Other Inputs	−10		10	
IOZ	Output Leakage Current	VSS ≤ VOUT ≤ VCC, Output off		−10		10	μA
ICC	VCC Supply Current	T_A = +25°C			80	125	mA
		T_A = 0°C			100	145	
CO	Output Capacitance	fc = 1.0MHz				15	pF
CI	Input Capacitance	T_A = 25°C				10	
CIO	I/O Capacitance	All pins at 0V				20	

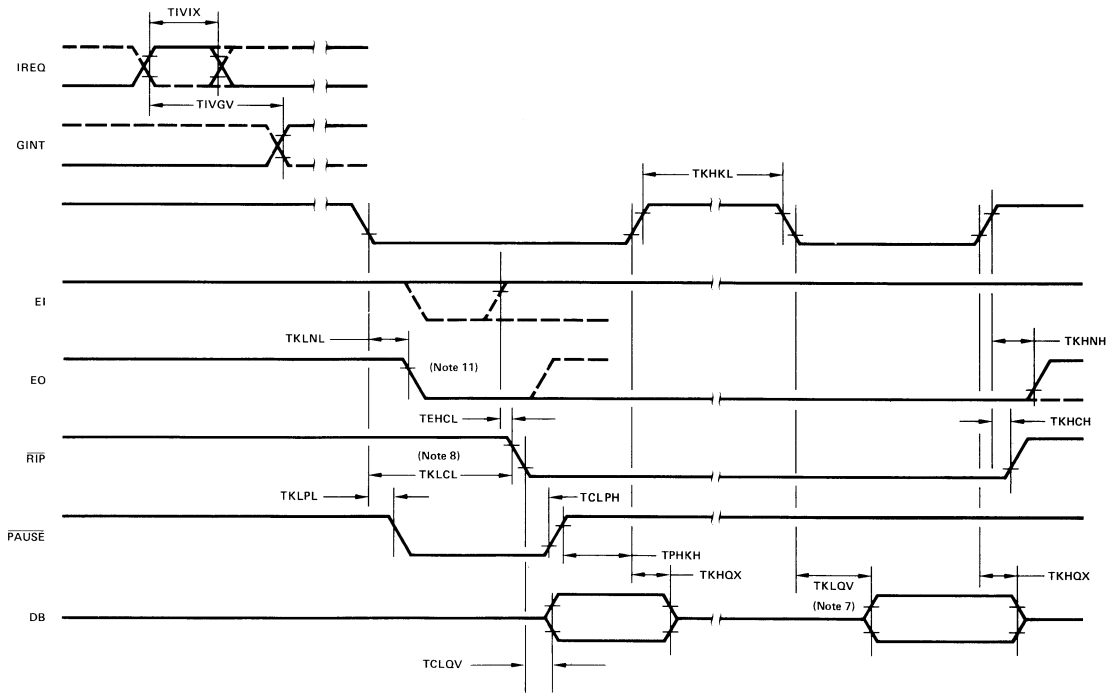
SWITCHING CHARACTERISTICS Over Operating Range (Notes 2, 3, 4, 5)

Parameters	Description	Am9519 Min.	Am9519 Max.	Am9519-1 Min.	Am9519-1 Max.	Am9519-4 Min.	Am9519-4 Max.	Units
TAVRL	C/$\overline{D}$ Valid and $\overline{CS}$ LOW to Read LOW	0		0		0		ns
TAVWL	C/$\overline{D}$ Valid and $\overline{CS}$ LOW to Write LOW	0		0		0		ns
TCLPH	$\overline{RIP}$ LOW to $\overline{PAUSE}$ HIGH (Note 6)	75	300	75	300	75	200	ns
TCLQV	$\overline{RIP}$ LOW to Data Out Valid (Note 7)		50		40		25	ns
TDVWH	Data In Valid to Write HIGH	250		200		125		ns
TEHCL	Enable in HIGH to $\overline{RIP}$ LOW (Notes 8, 9)	30	300	30	300	30	150	ns
TIVGV	Interrupt Request Valid to Group Interrupt Valid		800		650		475	ns
TIVIX	Interrupt Request Valid to Interrupt Request Don't Care (IREQ Pulse Duration)	250		250		150		ns
TKHCH	$\overline{IACK}$ HIGH to $\overline{RIP}$ HIGH (Note 8)		400		350		250	ns
TKHKL	$\overline{IACK}$ HIGH to $\overline{IACK}$ LOW ($\overline{IACK}$ Recovery)		500		500		200	ns
TKHNH	$\overline{IACK}$ HIGH to EO HIGH (Notes 10, 11)		800		700		600	ns
TKHQX	$\overline{IACK}$ HIGH to Data Out Invalid	20	200	20	100	20	60	ns
TKLCL	$\overline{IACK}$ LOW to $\overline{RIP}$ LOW (Note 8)	75	600	75	450	75	350	ns
TKLNL	$\overline{IACK}$ LOW to EO LOW (Notes 10, 11)		125		100		75	ns
TKLPL	$\overline{IACK}$ LOW to $\overline{PAUSE}$ LOW	25	175	25	125	25	75	ns
TKLQV	$\overline{IACK}$ LOW to Data Out Valid (Note 7)	25	300	25	200	25	175	ns
TPHKH	$\overline{PAUSE}$ HIGH to $\overline{IACK}$ HIGH	0		0		0		ns
TRHAX	Read HIGH to C/$\overline{D}$ and $\overline{CS}$ Don't Care	0		0		0		ns
TRHQX	Read HIGH to Data Out Invalid	20	200	20	100	20	60	ns
TRLQV	Read LOW to Data Out Valid		300		200		175	ns
TRLQX	Read LOW to Data Out Unknown	50		50		50		ns
TRLRH	Read LOW to Read HIGH ($\overline{RD}$ Pulse Duration)	300		250		200		ns
TWHAX	Write HIGH to C/$\overline{D}$ and $\overline{CS}$ Don't Care	0		0		0		ns
TWHDX	Write HIGH to Data In Don't Care	0		0		0		ns
TWHRW	Write HIGH to Read or Write LOW (Write Recovery)	600		400		250		ns
TWLWH	Write LOW to Write HIGH ($\overline{WR}$ Pulse Duration)	300		250		200		ns

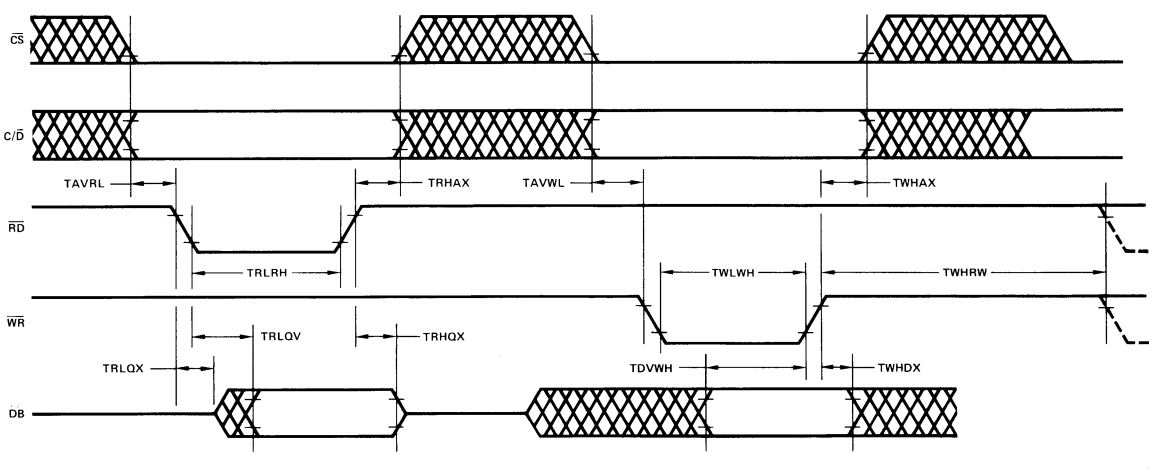
NOTES:

1. Typical values are for T_A = 25°C, nominal supply voltage and nominal processing parameters.
2. Test conditions assume transition times of 20ns or less, timing reference levels of 0.8V and 2.0V and output loading of one TTL gate plus 100pF, unless otherwise noted.
3. Transition abbreviations used for the switching parameter symbols include: H = High, L = Low, V = Valid, X = unknown or don't care, Z = high impedance.
4. Signal abbreviations used for the switching parameter symbols include: R = Read, W = Write, Q = Data Out, D = Data In, A = Address ($\overline{CS}$ and C/$\overline{D}$), K = Interrupt Acknowledge, N = Enable Out, E = Enable In, P = Pause, C = $\overline{RIP}$.
5. Switching parameters are listed in alphabetical order.
6. During the first $\overline{IACK}$ pulse, $\overline{PAUSE}$ will be low long enough to allow for priority resolution and will not go high until after $\overline{RIP}$ goes low (TCLPH).
7. TKLQV applies only to second, third and fourth $\overline{IACK}$ pulses while $\overline{RIP}$ is low. During the first $\overline{IACK}$ pulse, Data Out will be valid following the falling edge of $\overline{RIP}$ (TCLQV).
8. $\overline{RIP}$ is pulled low to indicate that an interrupt request has been selected. $\overline{RIP}$ cannot be pulled low until EI is high following an internal delay. TKLCL will govern the falling edge of $\overline{RIP}$ when EI is always high or is high early in the acknowledge cycle. TEHCL will govern when EI goes high later in the cycle. The rising edge of EI will be determined by the length of the preceding priority resolution chain. $\overline{RIP}$ remains low until after the rising edge of the $\overline{IACK}$ pulse that transfers the last response byte for the selected IREQ.
9. Test conditions for the EI line assume timing reference levels of 0.8V and 2.0V with transition times of 10ns or less.
10. Test conditions for the EO line assume output loading of two LS TTL gates plus 30pF and timing reference levels of 0.8V and 2.0V. Since EO normally only drives EI of another Am9519, higher speed operation can be specified with this more realistic test condition.
11. The arrival of $\overline{IACK}$ will cause EO to go low, disabling additional circuits that may be connected to EO. If no valid interrupt is pending, EO will return high when EI is high. If a pending request is selected, EO will stay low until after the last $\overline{IACK}$ pulse for that interrupt is complete and $\overline{RIP}$ goes high.
12. VOH specifications do not apply to $\overline{RIP}$ or to $\overline{GINT}$ when active-low. These outputs are open-drain and VOH levels will be determined by external circuitry.

SWITCHING WAVEFORMS



Interrupt Operations



Data Bus Transfers

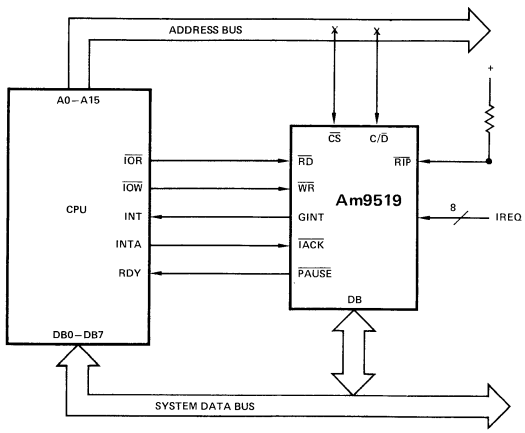


Figure 6. Base Interrupt System Configuration.

MOS-146

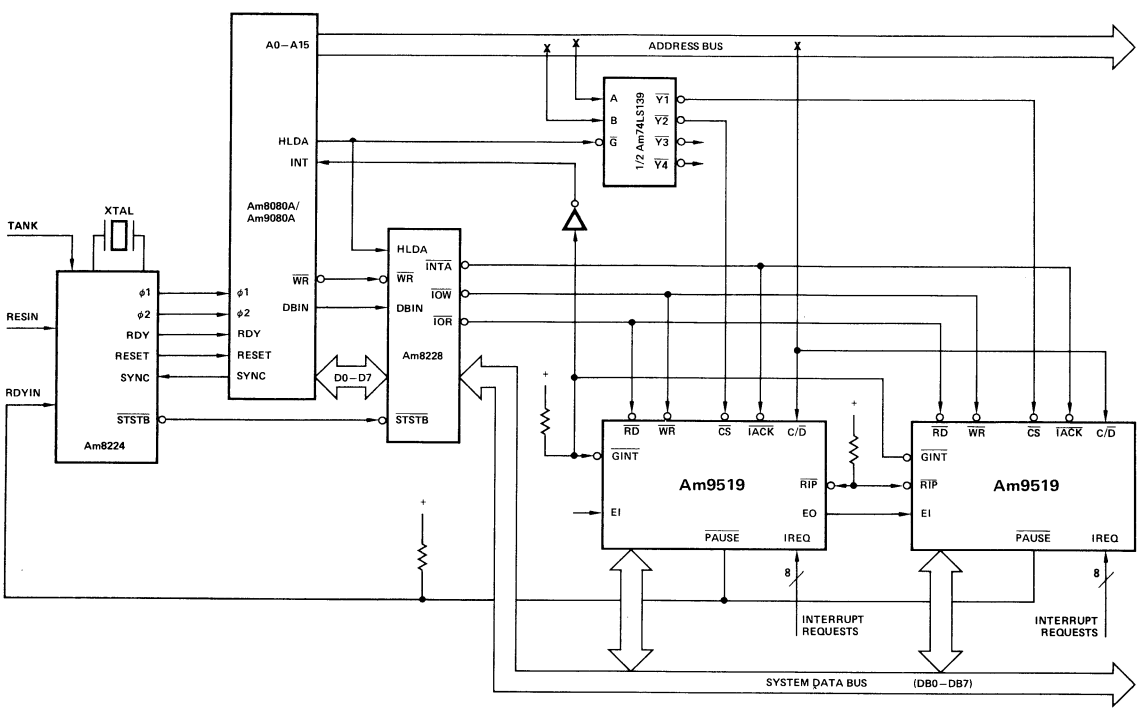
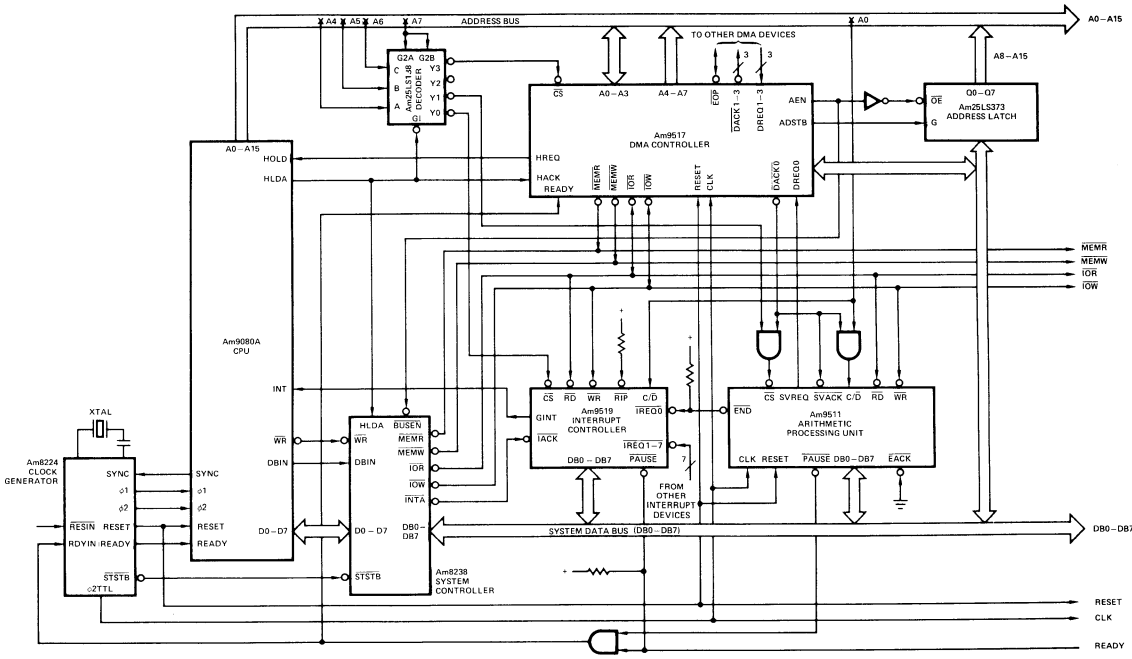


Figure 7. Expanded Interrupt System Configuration.

MOS-147

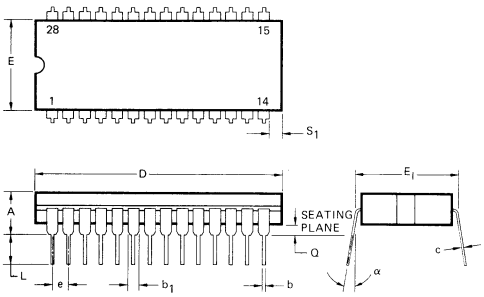


MOS-148

Figure 8. Am9519 Typical Application Example.

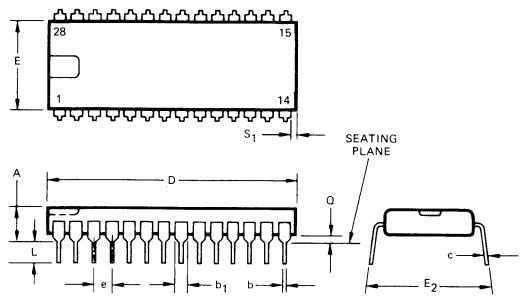
PHYSICAL DIMENSIONS

28-Pin Cerdip



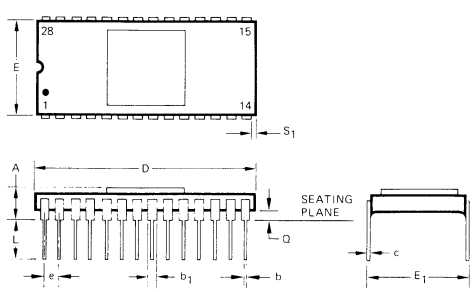
Reference Symbol	Inches	
	Min.	Max.
A	.150	.225
b	.016	.020
b_1	.045	.065
c	.009	.012
D	1.440	1.490
E	.510	.545
E_1	.600	.620
e	.090	.110
L	.125	.150
Q	.015	.060
S_1	.010	

28-Pin Molded DIP



Reference Symbol	Inches	
	Min.	Max.
A	.150	.200
b	.015	.020
b_1	.055	.065
c	.009	.011
D	1.450	1.440
E	.530	.550
E_2	.585	.700
e	.090	.110
L	.125	.160
Q	.015	.060
S_1	.040	.070

28-Pin Side-Brazed Ceramic



Reference Symbol	Inches	
	Min.	Max.
A	.100	.200
b	.015	.022
b_1	.030	.060
c	.008	.013
D	1.380	1.420
E	.560	.600
E_1	.580	.620
e	.090	.110
L	.120	.160
Q	.020	.060
S_1*	.005	
α	0	0

Applications

Algorithm Details for The Am9511 Arithmetic Processing Unit

TABLE OF CONTENTS

INTRODUCTION

The Am9511 APU is a complete, high performance, complex arithmetic processor contained within a single chip. It is designed to enhance the number manipulation capability of a wide variety of processor systems. It includes not only floating-point operations but fixed-point as well; not only basic add, subtract, multiply and divide operations, but a group of transcendental derived functions plus control and conversion commands as well. This Application Brief provides detailed descriptions of all the commands that can be executed by the Am9511 and indicates the error performance of the derived functions.

The Am9511 is packaged in a standard, 24 pin, dual in-line package with .6 inch between rows. Figure 1 shows the package pin assignments. Details on the operation of each interface pin will be found in the data sheet.

The block diagram in Figure 2 shows the internal structure of the APU. The part is addressed as two ports selected by the C/$\overline{D}$ control line. When C/$\overline{D}$ is high (Control Port), a read op-

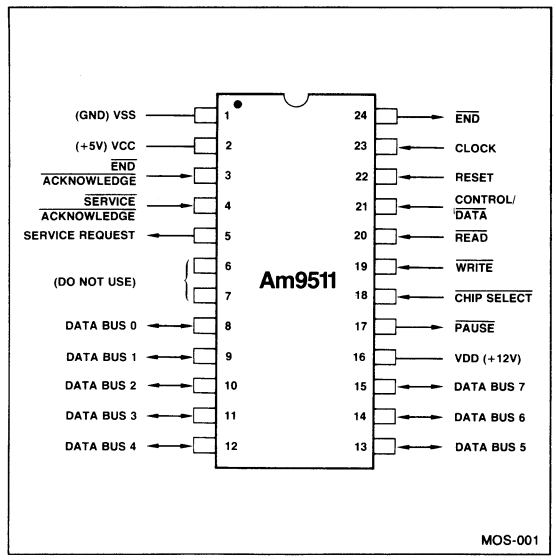


Figure 1. Connection Diagram.

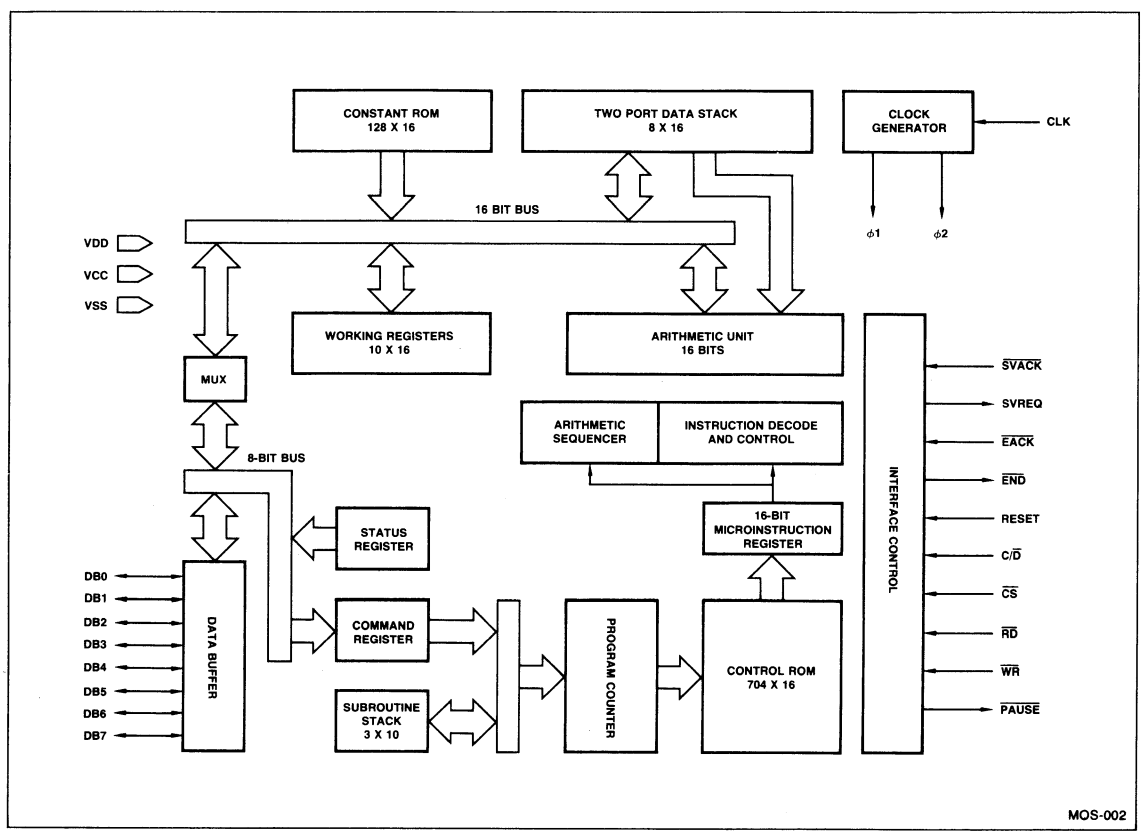


Figure 2. Arithmetic Processing Unit Block Diagram.

eration accesses the status register and a write operation enters a command. When C/$\overline{D}$ is low (Data Port), a read operation accesses data from the top of the data stack and a write operation enters data into the top of the data stack.

Data Formats

The APU executes both 16- and 32-bit fixed-point operations. All fixed-point operands and results are represented as binary two's complement integer values. The 16-bit format can express numbers with a range of −32,768 to +32,767. The 32-bit format can express numbers with a range of −2,147,483,648 to +2,147,483,647.

The floating-point format uses a 32-bit word with fields as shown in Figure 3. The most significant bit (bit 31) indicates the sign of the mantissa. The next seven bits form the exponent and the remaining 24 bits form the mantissa value.

The exponent of the base 2 is an unbiased two's complement number with a range of −64 to +63. The mantissa is a sign-magnitude number with an assumed binary point just to the left of the most significant mantissa bit (bit 23). All floating-point values must be normalized, which makes bit 23 always equal to 1 except when representing a value of zero. The number Zero is represented with binary zeros in all 32 bit positions.

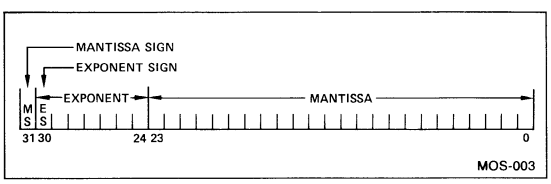


Figure 3. Floating Point Format.

Status Register

The Am9511 Status register format is shown in Figure 4. When the Busy bit (bit 7) is high, the APU is processing a previously entered command and the balance of the Status register should not be considered valid. When the Busy bit is low, the operation is complete and the other status bits are valid.

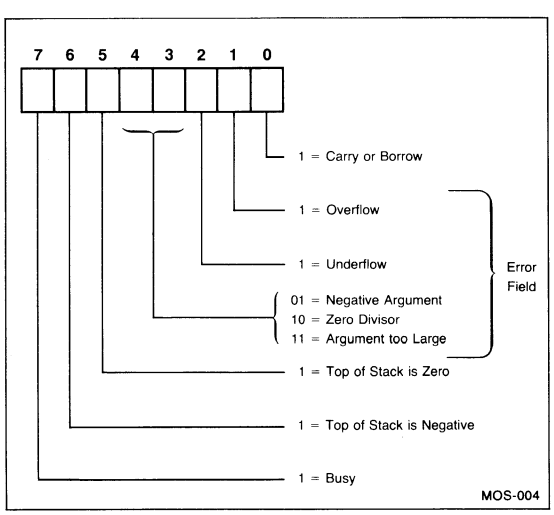


Figure 4. Status Register.

Data Stack

Figure 5 shows the two logical organizations of the internal data stack. It operates as a true push-down stack or FILO stack. That is, the data first written in will be the data last read out. Within each stack entry, the least significant byte is entered first and retrieved last.

Figure 6 shows a typical sequence for 32 bit operations. 6a represents the stack prior to entry of data. 6b shows the stack following entry of the LS Byte of operand C. 6c illustrates the stack contents following the entry of four bytes of operand C. When operands C, B and A are all fully entered the stack appears as in 6e. If a command is then issued, to add B to A for example, the stack contents look like 6f where R is the result of B + A. When the first (MSB) byte of R is removed the stack appears as in 6g. 6h shows the stack following the complete retrieval or R. An even number of bytes should always be transferred for any data operation.

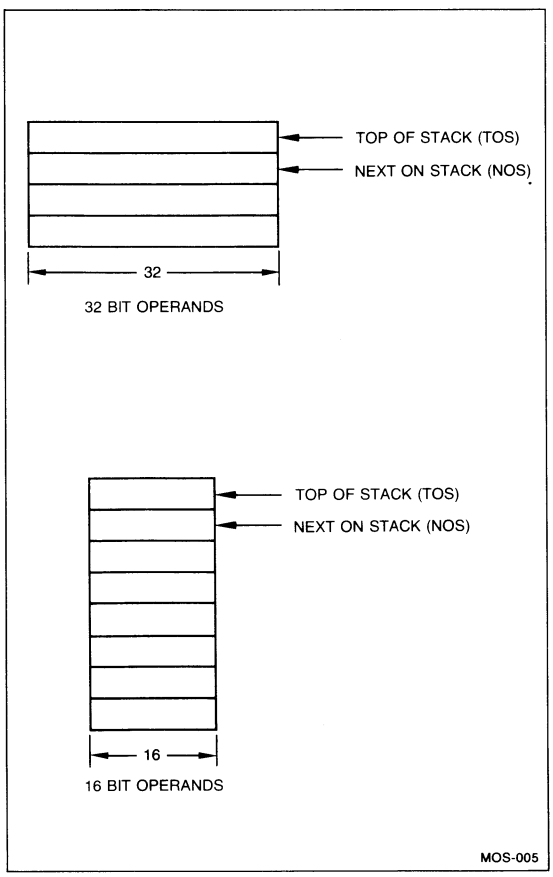


Figure 5. Stack Configurations.

Command Format

Each command executed by the APU is specified by a single byte with the format shown in Figure 7. Bits 0 through 4 indicate the operation to be performed. Bits 5 and 6 specify the data format. Bit 7 is used to control the Service Request interface line. When bit 7 is a one, the SVREQ output will go true when the execution of the command is complete.

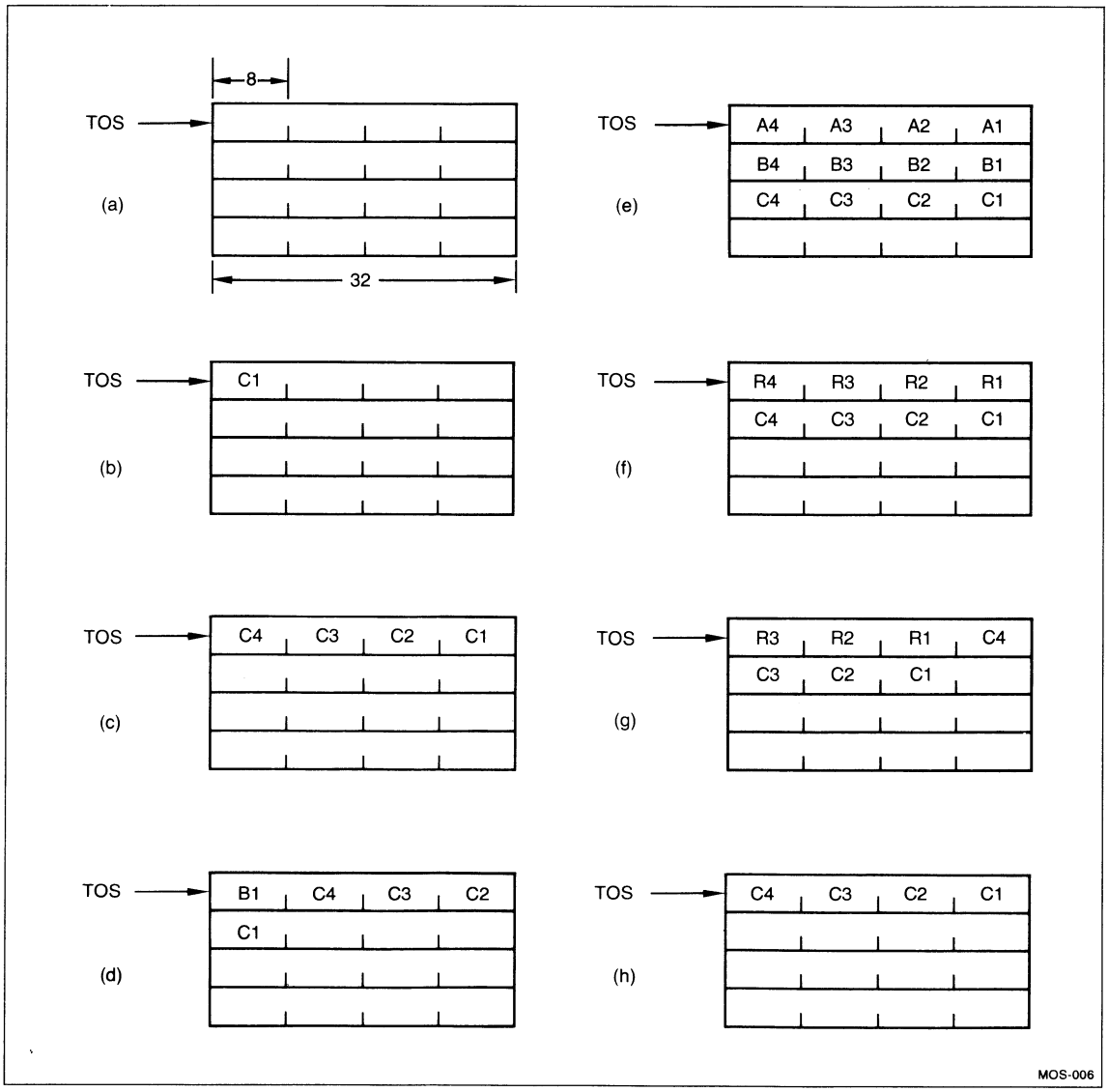


Figure 6. Stack Data Sequence Example.

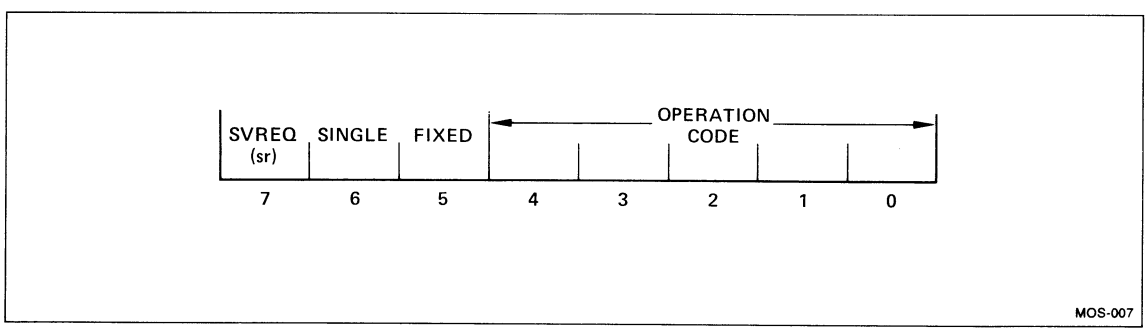


Figure 7. Command Format.

Command Mnemonic	Hex Code (sr = 1)	Hex Code (sr = 0)	Execution Cycles	Summary Description
16-BIT FIXED-POINT OPERATIONS				
SADD	EC	6C	16-18	Add TOS to NOS. Result to NOS. Pop Stack.
SSUB	ED	6D	30-32	Subtract TOS from NOS. Result to NOS. Pop Stack.
SMUL	EE	6E	84-94	Multiply NOS by TOS. Lower result to NOS. Pop Stack.
SMUU	F6	76	80-98	Multiply NOS by TOS. Upper result to NOS. Pop Stack.
SDIV	EF	6F	84-94	Divide NOS by TOS. Result to NOS. Pop Stack.
32-BIT FIXED-POINT OPERATIONS				
DADD	AC	2C	20-22	Add TOS to NOS. Result to NOS. Pop Stack.
DSUB	AD	2D	38-40	Subtract TOS from NOS. Result to NOS. Pop Stack.
DMUL	AE	2E	194-210	Multiply NOS by TOS. Lower result to NOS. Pop Stack.
DMUU	B6	36	182-218	Multiply NOS by TOS. Upper result to NOS. Pop Stack.
DDIV	AF	2F	196-210	Divide NOS by TOS. Result to NOS. Pop Stack.
32-BIT FLOATING-POINT PRIMARY OPERATIONS				
FADD	90	10	54-368	Add TOS to NOS. Result to NOS. Pop Stack.
FSUB	91	11	70-370	Subtract TOS from NOS. Result to NOS. Pop Stack.
FMUL	92	12	146-168	Multiply NOS by TOS. Result to NOS. Pop Stack.
FDIV	93	13	154-184	Divide NOS by TOS. Result to NOS. Pop Stack.
32-BIT FLOATING-POINT DERIVED OPERATIONS				
SQRT	81	01	782-870	Square Root of TOS. Result to TOS.
SIN	82	02	3796-4808	Sine of TOS. Result to TOS.
COS	83	03	3840-4878	Cosine of TOS. Result to TOS.
TAN	84	04	4894-5886	Tangent of TOS. Result to TOS.
ASIN	85	05	6230-7938	Inverse Sine of TOS. Result to TOS.
ACOS	86	06	6304-8284	Inverse Cosine of TOS. Result to TOS.
ATAN	87	07	4992-6536	Inverse Tangent of TOS. Result to TOS.
LOG	88	08	4474-7132	Common Logarithm of TOS. Result to TOS.
LN	89	09	4298-6956	Natural Logarithm of TOS. Result to TOS.
EXP	8A	0A	3794-4878	e raised to power in TOS. Result to TOS.
PWR	8B	0B	8290-12032	NOS raised to power in TOS. Result to NOS. Pop Stack.
DATA AND STACK MANIPULATION OPERATIONS				
NOP	80	00	4	No Operation. Clear or set SVREQ.
FIXS	9F	1F	90-214	Convert TOS from floating point format to fixed point format.
FIXD	9E	1E	90-336	
FLTS	9D	1D	62-156	Convert TOS from fixed point format to floating point format.
FLTD	9C	1C	56-342	
CHSS	F4	74	22-24	Change sign of fixed point operand on TOS.
CHSD	B4	34	26-28	
CHSF	95	15	16-20	Change sign of floating point operand on TOS.
PTOS	F7	77	16	Push stack. Duplicate NOS in TOS.
PTOD	B7	37	20	
PTOF	97	17	20	
POPS	F8	78	10	Pop stack. Old NOS becomes new TOS. Old TOS rotates to bottom.
POPD	B8	38	12	
POPF	98	18	12	
XCHS	F9	79	18	Exchange TOS and NOS.
XCHD	B9	39	26	
XCHF	99	19	26	
PUPI	9A	1A	16	Push floating point constant π onto TOS. Previous TOS becomes NOS.

Figure 8.

ALGORITHM DISCUSSION

Computer approximations of transcendental functions are often based on some form of polynomial equation, such as:

$$F(X) = A_0 + A_1X + A_2X^2 + A_3X^3 + A_4X^4 \ldots . \quad (1\text{-}1)$$

The primary shortcoming of an approximation in this form is that it typically exhibits very large errors when the magnitude of $|X|$ is large, although the errors are small when $|X|$ is small. With polynomials in this form, the error distribution is markedly uneven over any arbitrary interval.

Fortunately, a set of approximating functions exists that not only minimizes the maximum error but also provides an even distribution of errors within the selected data representation interval. These are known as Chebyshev Polynomials and are based upon cosine functions.[1,2] These functions are defined as follows:

$$T_n(X) = \text{Cos } n\theta; \text{ where } n = 0,1,2 \ldots \quad (1\text{-}2)$$
$$\theta = \text{Cos}^{-1}X$$

The various terms of the Chebyshev series can be computed as shown below:

$$T_0(X) = \text{Cos } (0 \cdot \theta) = \text{Cos } (0) = 1 \quad (1\text{-}4)$$
$$T_1(X) = \text{Cos } (\text{Cos}^{-1}X) = X \quad (1\text{-}5)$$
$$T_2(X) = \text{Cos } 2\theta = 2\text{Cos}^2\,\theta - 1 = 2\text{Cos}^2\,(\text{Cos}^{-1}X) - 1 = 2X^2 - 1 \quad (1\text{-}6)$$

In general, the next term in the Chebyshev series can be recursively derived from the previous term as follows:

$$T_n(X) = 2X\,[T_n{-}1(X)] - T_n{-}2\,(X); \; n \geq 2 \quad (1\text{-}7)$$

The terms T_3, T_4, T_5 and T_6 are given below for reference:

$$T_3 = 4X^3 - 3X \quad (1\text{-}8)$$
$$T_4 = 8X^4 - 8X^2 + 1 \quad (1\text{-}9)$$
$$T_5 = 16X^5 - 20X^3 + 5X \quad (1\text{-}10)$$
$$T_6 = 32X^6 - 48X^4 + 18X^2 - 1 \quad (1\text{-}11)$$

Chebyshev polynomials can be directly substituted for corresponding terms of a power series expansion by simple algebraic manipulation:

$$1 = T_0 \quad (1\text{-}12)$$
$$X = T_1 \quad (1\text{-}13)$$
$$X^2 = 1/2\,(T_0 + T_2) \quad (1\text{-}14)$$
$$X^3 = 1/4\,(3T_1 + T_3) \quad (1\text{-}15)$$
$$X^4 = 1/8\,(3T_0 + 4T_2 + T_4) \quad (1\text{-}16)$$
$$X^5 = 1/16\,(10T_1 + 5T_3 + T_5) \quad (1\text{-}17)$$
$$X^6 = 1/32\,(10T_0 + 15T_2 + 6T_4 + T_6) \quad (1\text{-}18)$$

Each of the derived functions except square root implemented in the Am9511 APU has been reduced to Chebyshev polynomial form. A sufficient number of terms has been used to provide a mean relative error of about one part in 10^7.

Each of the functions is implemented as a three-step process. The first step involves range reduction. That is, the input argument to the function is transformed to fall within a range of values for which the function can compute a valid result. For example, since functions like sine and cosine are periodic for multiples of $\pi/2$ radians, input arguments for these functions are converted to lie within the range of $-\pi/2$ to $+\pi/2$. Processing of the range-reduced input argument according to the appropriate Chebyshev expansion is done in the second step. The third step includes any necessary post processing of the result, such as sign correction in sine or cosine for a particular quadrant. Range reduction and post processing are unique to each of the functions, while processing the Chebyshev expansion is performed by an algorithm that is common to all functions.

DERIVED FUNCTION ERROR PERFORMANCE

Since each of the derived functions is an approximation of the true function, results computed by the Am9511 are not always exact. In order to more comprehensively quantify the error performance of the component, the following graphs have been prepared. Each function has been executed with a statistically significant number of diverse data values, spanning the allowable input data range, and resulting errors have been tabulated. Absolute errors (that is, the number of bits in error) have been converted to relative errors according to the following equation:

$$\text{Relative Error} = \frac{\text{Absolute Error}}{\text{True Result}}$$

This conversion permits the error to be viewed with respect to the magnitude of the true result. This provides a more objective measurement of error performance since it directly translates to a measure of significant digits of algorithm accuracy.

For example, if a given absolute error is 0.001 and the true result is also 0.001, it is clear that the relative error is equal to 1.0 (which implies that even the first significant digit of the result is wrong). However, if the same absolute error is computed for a true result of 10000.0, then the first six significant digits of the result are correct (0.001/10000 = 0.0000001).

Each of the following graphs was prepared to illustrate relative algorithm error as a function of input data range. Natural Logarithm is the only exception; since logarithms are typically additive, absolute error is plotted for this function.

Two graphs have not been included in the following figures: common logarithms and the power function (X^Y). Common logarithms are computed by multiplication of the natural logarithm by the conversion factor 0.43429448 and the error function is therefore the same as that for natural logarithm. The power function is realized by combination of natural log and exponential functions according to the equation:

$$X^Y = e^{Y\text{Ln}x}$$

The error for the power function is a combination of that for the logarithm and exponential functions. Specifically, the relative error for PWR is expressed as follows:

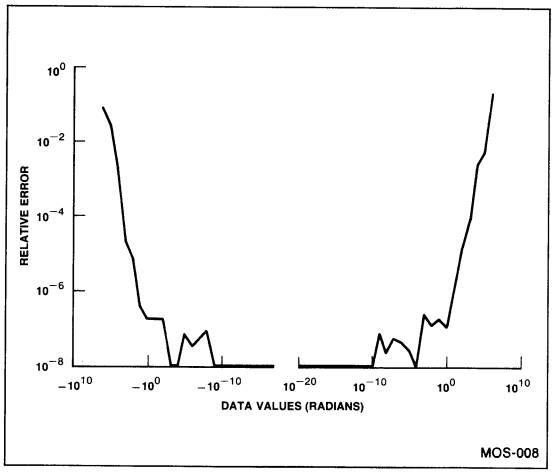
$$|RE_{PWR}| = |RE_{EXP}| + |X\,(AE_{LN})|$$

where:

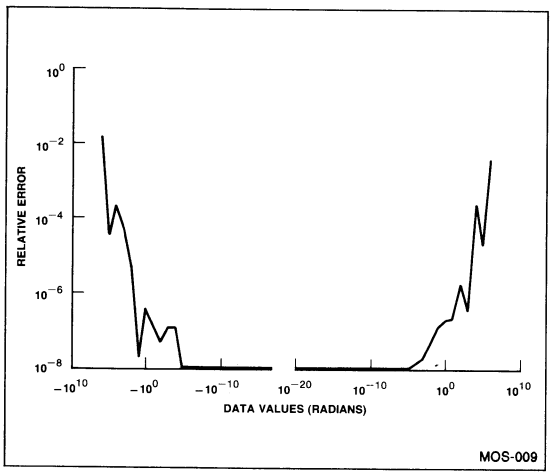
RE_{PWR} = relative error for power function
RE_{EXP} = relative error for exponential function
AE_{LN} = absolute error for natural logarithm
X = value of independent variable in X^Y

Notes:

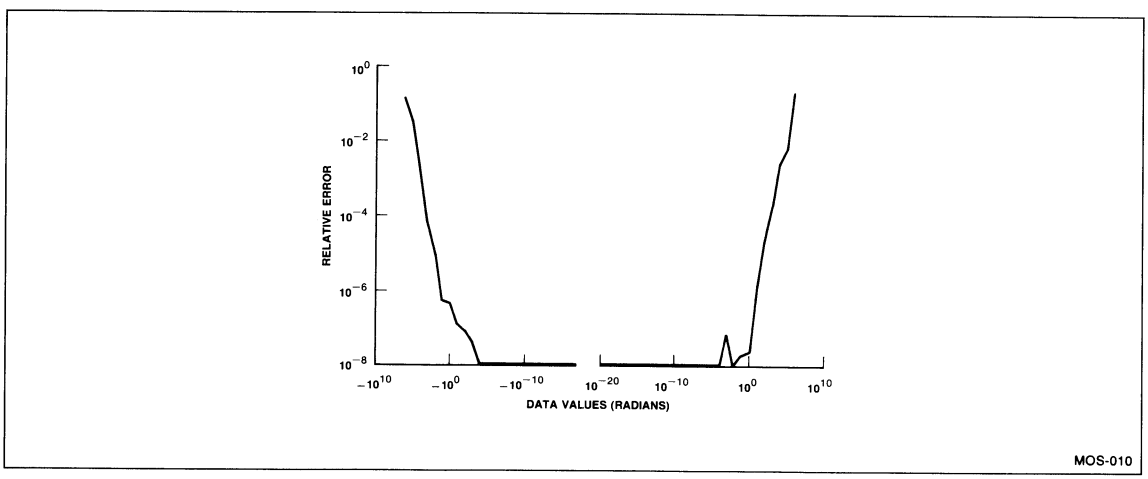
1. Properties of Chebyshev polynomials taken from: Applied Numerical Methods; Carnahan, Luther, Wikes; John Wiley & Sons, Inc.; 1969.
2. Derived function algorithms adapted from: Algorithms for Special Functions (I and II); Numerische Mathematic (1963); Clenshaw, Miller, Woodger.



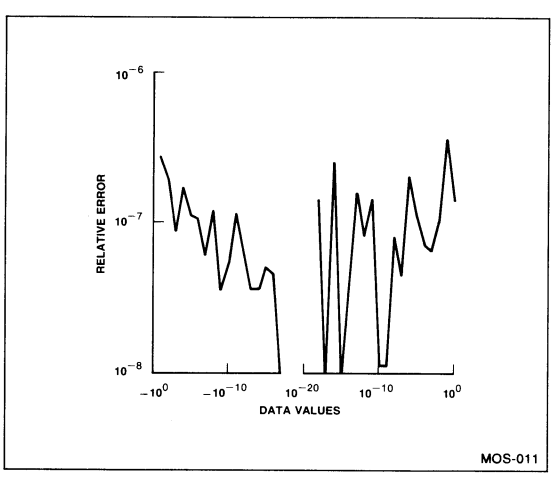
SINE



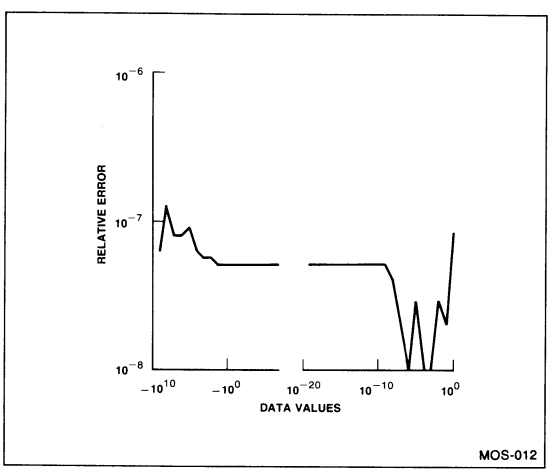
COSINE



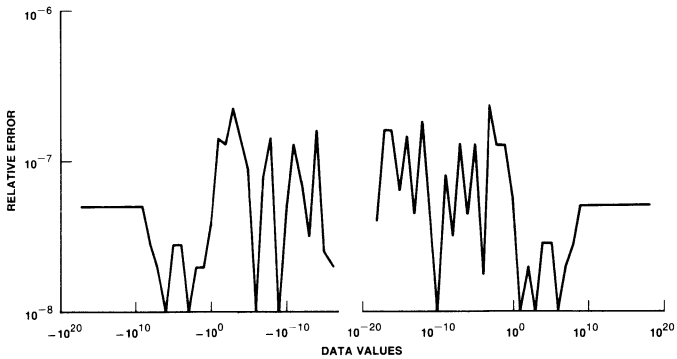
TANGENT



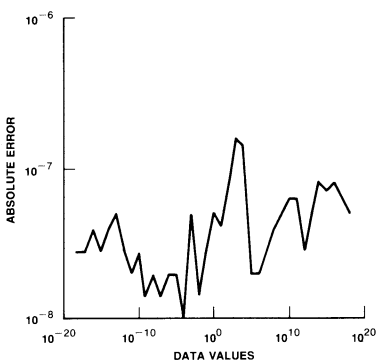
INVERSE SINE



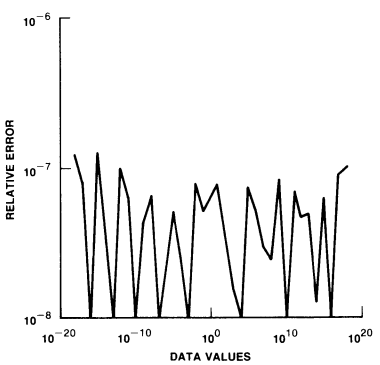
INVERSE COSINE



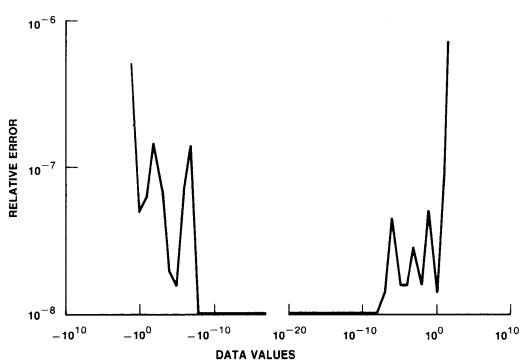
INVERSE TANGENT



NATURAL LOG



SQUARE ROOT



e^x

COMMAND DESCRIPTIONS

This section contains detailed descriptions of the APU commands. They are arranged in alphabetical order by command mnemonic. In the descriptions, TOS means Top Of Stack and NOS means Next On Stack.

All derived functions except Square Root use Chebyshev polynomial approximating algorithms. This approach is used to help minimize the internal microprogram, to minimize the maximum error values and to provide a relatively even distribution of errors over the data range. The basic arithmetic operations are used by the derived functions to compute the various Chebyshev terms. The basic operations may produce error codes in the status register as a result.

Execution times are listed in terms of clock cycles and may be converted into time values by multiplying by the clock period used. For example, an execution time of 44 clock cycles when running at a 4MHz rate translates to 11 microseconds (44 x .25μs = 11μs). Variations in execution cycles reflect the data dependency of the algorithms.

In some operations exponent overflow or underflow may be possible. When this occurs, the exponent returned in the result will be 128 greater or smaller than its true value.

Many of the functions use portions of the data stack as scratch storage during development of the results. Thus previous values in those stack locations will be lost. Scratch locations destroyed are listed in the command descriptions and shown with the crossed-out locations in the Stack Contents After diagram.

Figure 8 is a summary of all the Am9511 commands. It shows the hex codes for each command, the mnemonic abbreviation, a brief description and the execution time in clock cycles. The commands are grouped by functional classes.

Figure 9 lists the command mnemonics in alphabetical order.

ACOS	ARCCOSINE	LOG	COMMON LOGARITHM
ASIN	ARCSINE	LN	NATURAL LOGARITHM
ATAN	ARCTANGENT	NOP	NO OPERATION
CHSD	CHANGE SIGN DOUBLE	POPD	POP STACK DOUBLE
CHSF	CHANGE SIGN FLOATING	POPF	POP STACK FLOATING
CHSS	CHANGE SIGN SINGLE	POPS	POP STACK SINGLE
COS	COSINE	PTOD	PUSH STACK DOUBLE
DADD	DOUBLE ADD	PTOF	PUSH STACK FLOATING
DDIV	DOUBLE DIVIDE	PTOS	PUSH STACK SINGLE
DMUL	DOUBLE MULTIPLY LOWER	PUPI	PUSH π
DMUU	DOUBLE MULTIPLY UPPER	PWR	POWER (X^Y)
DSUB	DOUBLE SUBTRACT	SADD	SINGLE ADD
EXP	EXPONENTIATION (e^x)	SDIV	SINGLE DIVIDE
FADD	FLOATING ADD	SIN	SINE
FDIV	FLOATING DIVIDE	SMUL	SINGLE MULTIPLY LOWER
FIXD	FIX DOUBLE	SMUU	SINGLE MULTIPLY UPPER
FIXS	FIX SINGLE	SQRT	SQUARE ROOT
FLTD	FLOAT DOUBLE	SSUB	SINGLE SUBTRACT
FLTS	FLOAT SINGLE	TAN	TANGENT
FMUL	FLOATING MULTIPLY	XCHD	EXCHANGE OPERANDS DOUBLE
FSUB	FLOATING SUBTRACT	XCHF	EXCHANGE OPERANDS FLOATING
		XCHS	EXCHANGE OPERANDS SINGLE

Figure 9. Command Mnemonics in Alphabetical Order.

ACOS

32-BIT FLOATING-POINT INVERSE COSINE

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	0	0	0	1	1	0

Hex Coding: 86 with sr = 1
06 with sr = 0

Execution Time: 6304 to 8284 clock cycles

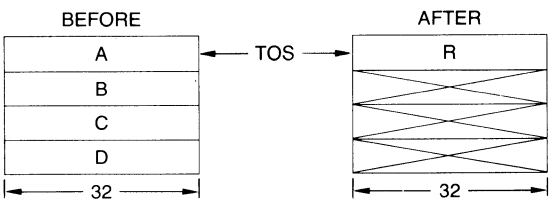
Description:

The 32-bit floating-point operand A at the TOS is replaced by the 32-bit floating-point inverse cosine of A. The result R is a value in radians between 0 and π. Initial operands A, B, C and D are lost. ACOS will accept all input data values within the range of -1.0 to $+1.0$. Values outside this range will return an error code of 1100 in the status register.

Accuracy: ACOS exhibits a maximum relative error of 2.0 x 10^{-7} over the valid input data range.

Status Affected: Sign, Zero, Error Field

STACK CONTENTS



ATAN

32-BIT FLOATING-POINT INVERSE TANGENT

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	0	0	0	1	1	1

Hex Coding: 87 with sr = 1
07 with sr = 0

Execution Time: 4992 to 6536 clock cycles

Description:

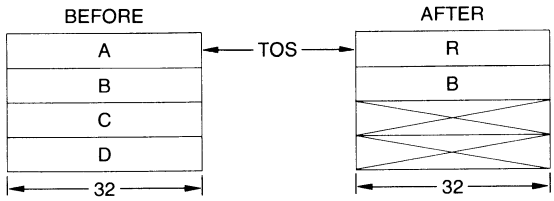
The 32-bit floating-point operand A at the TOS is replaced by the 32-bit floating-point inverse tangent of A. The result R is a value in radians between $-\pi/2$ and $+\pi/2$. Initial operands A, C and D are lost. Operand B is unchanged.

ATAN will accept all input data values that can be represented in the floating point format.

Accuracy: ATAN exhibits a maximum relative error of 3.0 x 10^{-7} over the input data range.

Status Affected: Sign, Zero

STACK CONTENTS



ASIN

32-BIT FLOATING-POINT INVERSE SINE

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	0	0	0	1	0	1

Hex Coding: 85 with sr = 1
05 with sr = 0

Execution Time: 6230 to 7938 clock cycles

Description:

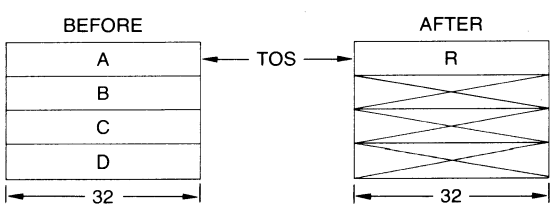
The 32-bit floating-point operand A at the TOS is replaced by the 32-bit floating-point inverse sine of A. The result R is a value in radians between $-\pi/2$ and $+\pi/2$. Initial operands A, B, C and D are lost.

ASIN will accept all input data values within the range of -1.0 to $+1.0$. Values outside this range will return an error code of 1100 in the status register.

Accuracy: ASIN exhibits a maximum relative error of 4.0 x 10^{-7} over the valid input data range.

Status Affected: Sign, Zero, Error Field

STACK CONTENTS



CHSD

32-BIT FIXED-POINT SIGN CHANGE

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	1	1	0	1	0	0

Hex Coding: B4 with sr = 1
34 with sr = 0

Execution Time: 26 to 28 clock cycles

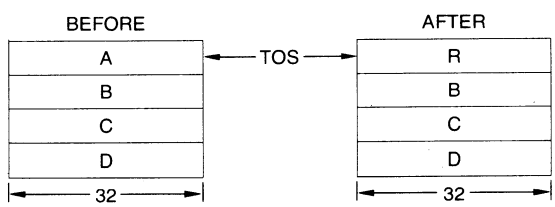
Description:

The 32-bit fixed-point two's complement integer operand A at the TOS is subtracted from zero. The result R replaces A at the TOS. Other entries in the stack are not disturbed.

Overflow status will be set and the TOS will be returned unchanged when A is input as the most negative value possible in the format since no positive equivalent exists.

Status Affected: Sign, Zero, Error Field (overflow)

STACK CONTENTS



CHSF

32-BIT FLOATING-POINT SIGN CHANGE

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	0	1	0	1	0	1

Hex Coding: 95 with sr = 1
15 with sr = 0

Execution Time: 16 to 20 clock cycles

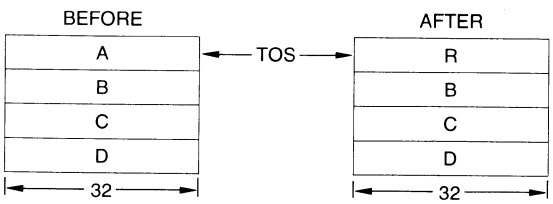
Description:

The sign of the mantissa of the 32-bit floating-point operand A at the TOS is inverted. The result R replaces A at the TOS. Other stack entries are unchanged.

If A is input as zero (mantissa MSB = 0), no change is made.

Status Affected: Sign, Zero

STACK CONTENTS



CHSS

16-BIT FIXED-POINT SIGN CHANGE

	7	6	5	4	3	2	1	0
Binary Coding:	sr	1	1	1	0	1	0	0

Hex Coding: F4 with sr = 1
74 with sr = 0

Execution Time: 22 to 24 clock cycles

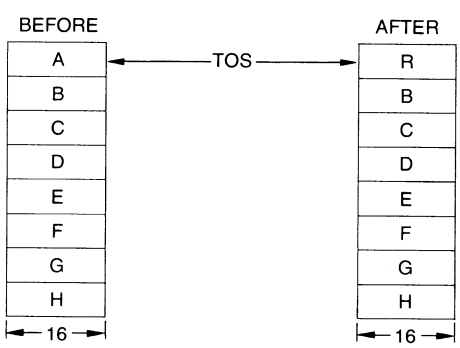
Description:

16-bit fixed-point two's complement integer operand A at the TOS is subtracted from zero. The result R replaces A at the TOS. All other operands are unchanged.

Overflow status will be set and the TOS will be returned unchanged when A is input as the most negative value possible in the format since no positive equivalent exists.

Status Affected: Sign, Zero, Overflow

STACK CONTENTS



COS

32-BIT FLOATING-POINT COSINE

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	0	0	0	0	1	1

Hex Coding: 83 with sr = 1
03 with sr = 0

Execution Time: 3840 to 4878 clock cycles

Description:

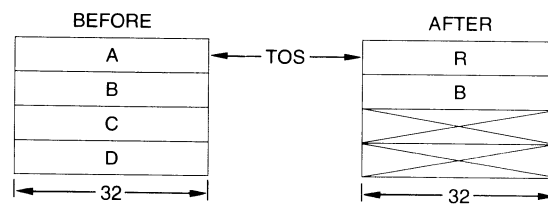
The 32-bit floating-point operand A at the TOS is replaced by R, the 32-bit floating-point cosine of A. A is assumed to be in radians. Operands A, C and D are lost. B is unchanged.

The COS function can accept any input data value that can be represented in the data format. All input values are range reduced to fall within an interval of $-\pi/2$ to $+\pi/2$ radians.

Accuracy: COS exhibits a maximum relative error of 5.0 x 10^{-7} for all input data values in the range of -2π to $+2\pi$ radians.

Status Affected: Sign, Zero

STACK CONTENTS



DADD

32-BIT FIXED-POINT ADD

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	1	0	1	1	0	0

Hex Coding: AC with sr = 1
2C with sr = 0

Execution Time: 20 to 22 clock cycles

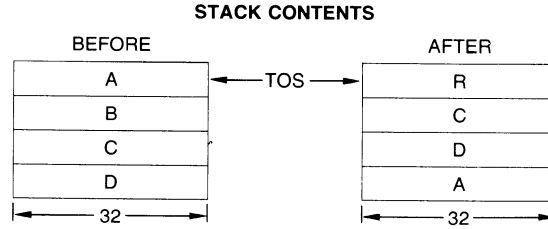
Description:

The 32-bit fixed-point two's complement integer operand A at the TOS is added to the 32-bit fixed-point two's complement integer operand B at the NOS. The result R replaces operand B and the Stack is moved up so that R occupies the TOS. Operand B is lost. Operands A, C and D are unchanged. If the addition generates a carry it is reported in the status register.

If the result is too large to be represented by the data format, the least significant 32 bits of the result are returned and overflow status is reported.

Status Affected: Sign, Zero, Carry, Error Field

STACK CONTENTS



DDIV

32-BIT FIXED-POINT DIVIDE

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	1	0	1	1	1	1

Hex Coding: AF with sr = 1
2F with sr = 0

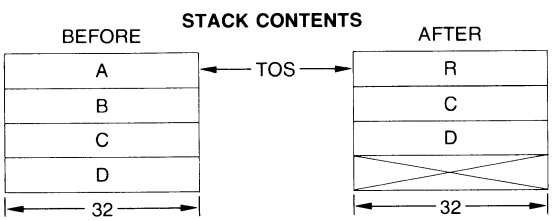
Execution Time: 196 to 210 clock cycles when A ≠ 0
18 clock cycles when A = 0.

Description:

The 32-bit fixed-point two's complement integer operand B at NOS is divided by the 32-bit fixed-point two's complement integer operand A at the TOS. The 32-bit integer quotient R replaces B and the stack is moved up so that R occupies the TOS. No remainder is generated. Operands A and B are lost. Operands C and D are unchanged.

If A is zero, R is set equal to B and the divide-by-zero error status will be reported. If either A or B is the most negative value possible in the format, R will be meaningless and the overflow error status will be reported.

Status Affected: Sign, Zero, Error Field



DMUL

32-BIT FIXED-POINT MULTIPLY, LOWER

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	1	0	1	1	1	0

Hex Coding: AE with sr = 1
2E with sr = 0

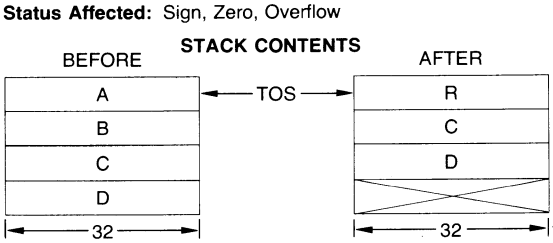
Execution Time: 194 to 210 clock cycles

Description:

The 32-bit fixed-point two's complement integer operand A at the TOS is multiplied by the 32-bit fixed-point two's complement integer operand B at the NOS. The 32-bit least significant half of the product R replaces B and the stack is moved up so that R occupies the TOS. The most significant half of the product is lost. Operands A and B are lost. Operands C and D are unchanged.

The overflow status bit is set if the discarded upper half was non-zero. If either A or B is the most negative value that can be represented in the format, that value is returned as R and the overflow status is set.

Status Affected: Sign, Zero, Overflow



DMUU

32-BIT FIXED-POINT MULTIPLY, UPPER

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	1	1	0	1	1	0

Hex Coding: B6 with sr = 1
36 with sr = 0

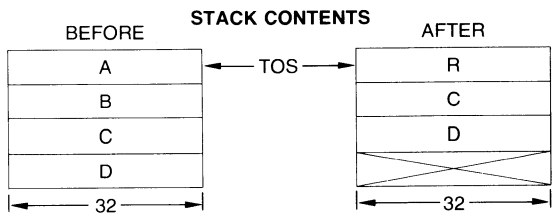
Execution Time: 182 to 218 clock cycles

Description:

The 32-bit fixed-point two's complement integer operand A at the TOS is multiplied by the 32-bit fixed-point two's complement integer operand B at the NOS. The 32-bit most significant half of the product R replaces B and the stack is moved up so that R occupies the TOS. The least significant half of the product is lost. Operands A and B are lost. Operands C and D are unchanged.

If A or B was the most negative value possible in the format, overflow status is set and R is meaningless.

Status Affected: Sign, Zero, Overflow



DSUB

32-BIT FIXED-POINT SUBTRACT

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	1	0	1	1	0	1

Hex Coding: AD with sr = 1
2D with sr = 0

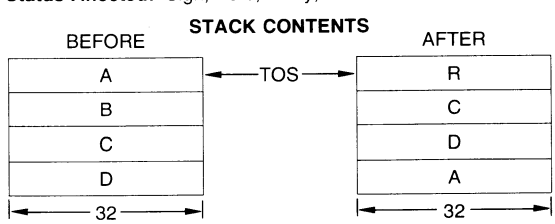
Execution Time: 38 to 40 clock cycles

Description:

The 32-bit fixed-point two's complement operand A at the TOS is subtracted from the 32-bit fixed-point two's complement operand B at the NOS. The difference R replaces operand B and the stack is moved up so that R occupies the TOS. Operand B is lost. Operands A, C and D are unchanged.

If the subtraction generates a borrow it is reported in the carry status bit. If A is the most negative value that can be represented in the format the overflow status is set. If the result cannot be represented in the data format range, the overflow bit is set and the 32 least significant bits of the result are returned as R.

Status Affected: Sign, Zero, Carry, Overflow



EXP

32-BIT FLOATING-POINT e^X

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	0	0	1	0	1	0

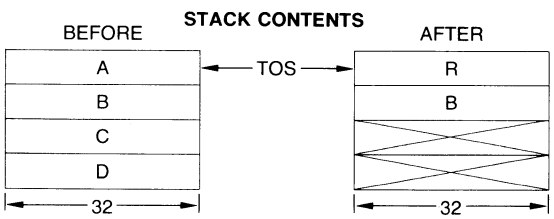
Hex Coding: 8A with sr = 1
0A with sr = 0

Execution Time: 3794 to 4878 clock cycles for $|A| \leq 1.0 \times 2^5$
34 clock cycles for $|A| > 1.0 \times 2^5$

Description:
The base of natural logarithms, e, is raised to an exponent value specified by the 32-bit floating-point operand A at the TOS. The result R of e^A replaces A. Operands A, C and D are lost. Operand B is unchanged.
EXP accepts all input data values within the range of $-1.0 \times 2^{+5}$ to $+1.0 \times 2^{+5}$. Input values outside this range will return a code of 1100 in the error field of the status register.

Accuracy: EXP exhibits a maximum relative error of 5.0×10^{-7} over the valid input data range.

Status Affected: Sign, Zero, Error Field



FADD

32-BIT FLOATING-POINT ADD

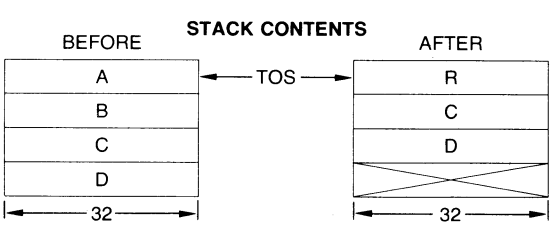
	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	0	1	0	0	0	0

Hex Coding: 90 with sr = 1
10 with sr = 0

Execution Time: 54 to 368 clock cycles for A ≠ 0
24 clock cycles for A = 0

Description:
32-bit floating-point operand A at the TOS is added to 32-bit floating-point operand B at the NOS. The result R replaces B and the stack is moved up so that R occupies the TOS. Operands A and B are lost. Operands C and D are unchanged.
Exponent alignment before the addition and normalization of the result accounts for the variation in execution time. Exponent overflow and underflow are reported in the status register, in which case the mantissa is correct and the exponent is offset by 128.

Status Affected: Sign, Zero, Error Field



FDIV

32-BIT FLOATING-POINT DIVIDE

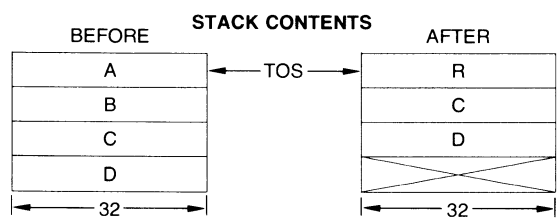
	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	0	1	0	0	1	1

Hex Coding: 93 with sr = 1
13 with sr = 0

Execution Time: 154 to 184 clock cycles for A ≠ 0
22 clock cycles for A = 0

Description:
32-bit floating-point operand B at NOS is divided by 32-bit floating-point operand A at the TOS. The result R replaces B and the stack is moved up so that R occupies the TOS. Operands A and B are lost. Operands C and D are unchanged.
If operand A is zero, R is set equal to B and the divide-by-zero error is reported in the status register. Exponent overflow or underflow is reported in the status register, in which case the mantissa portion of the result is correct and the exponent portion is offset by 128.

Status Affected: Sign, Zero, Error Field



FIXD

32-BIT FLOATING-POINT TO 32-BIT FIXED-POINT CONVERSION

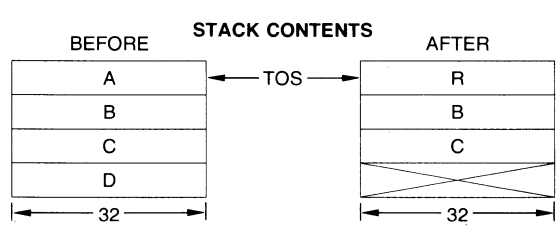
	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	0	1	1	1	1	0

Hex Coding: 9E with sr = 1
1E with sr = 0

Execution Time: 90 to 336 clock cycles

Description:
32-bit floating-point operand A at the TOS is converted to a 32-bit fixed-point two's complement integer. The result R replaces A. Operands A and D are lost. Operands B and C are unchanged.
If the integer portion of A is larger than 31 bits when converted, the overflow status will be set and A will not be changed. Operand D, however, will still be lost.

Status Affected: Sign, Zero Overflow



FIXS

32-BIT FLOATING-POINT TO 16-BIT FIXED-POINT CONVERSION

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	0	1	1	1	1	1

Hex Coding: 9F with sr = 1
1F with sr = 0

Execution Time: 90 to 214 clock cycles

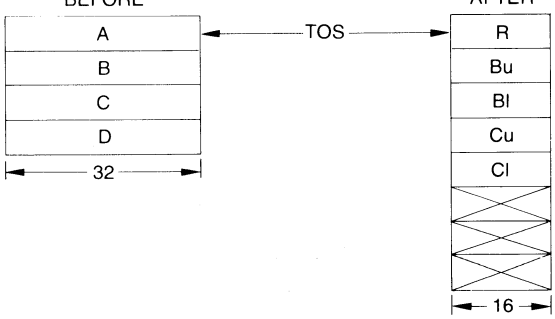
Description:

32-bit floating-point operand A at the TOS is converted to a 16-bit fixed-point two's complement integer. The result R replaces the lower half of A and the stack is moved up by two bytes so that R occupies the TOS. Operands A and D are lost. Operands B and C are unchanged, but appear as upper (u) and lower (l) halves on the 16-bit wide stack if they are 32-bit operands.

If the integer portion of A is larger than 15 bits when converted, the overflow status will be set and A will not be changed. Operand D, however, will still be lost.

Status Affected: Sign, Zero, Overflow

STACK CONTENTS



FLTD

32-BIT FIXED-POINT TO 32-BIT FLOATING-POINT CONVERSION

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	0	1	1	1	0	0

Hex Coding: 9C with sr = 1
1C with sr = 0

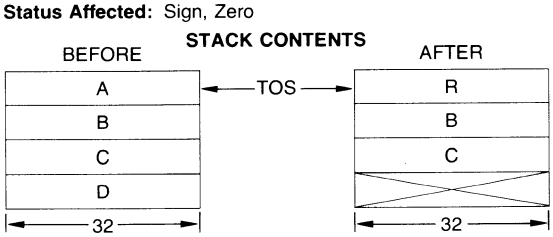
Execution Time: 56 to 342 clock cycles

Description:

32-bit fixed-point two's complement integer operand A at the TOS is converted to a 32-bit floating-point number. The result R replaces A at the TOS. Operands A and D are lost. Operands B and C are unchanged.

Status Affected: Sign, Zero

STACK CONTENTS



FLTS

16-BIT FIXED-POINT TO 32-BIT FLOATING-POINT CONVERSION

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	0	1	1	1	0	1

Hex Coding: 9D with sr = 1
1D with sr = 0

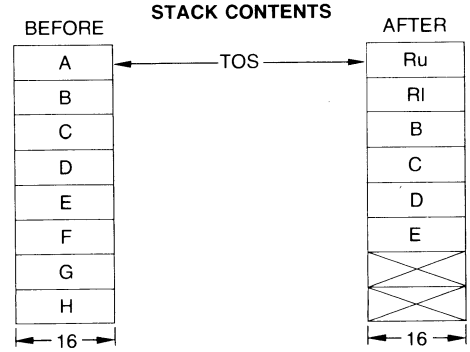
Execution Time: 62 to 156 clock cycles

Description:

16-bit fixed-point two's complement integer A at the TOS is converted to a 32-bit floating-point number. The lower half of the result R (Rl) replaces A, the upper half (Ru) replaces H and the stack is moved down so that Ru occupies the TOS. Operands A, F, G and H are lost. Operands B, C, D and E are unchanged.

Status Affected: Sign, Zero

STACK CONTENTS



FMUL

32-BIT FLOATING-POINT MULTIPLY

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	0	1	0	0	1	0

Hex Coding: 92 with sr = 1
12 with sr = 0

Execution Time: 146 to 168 clock cycles

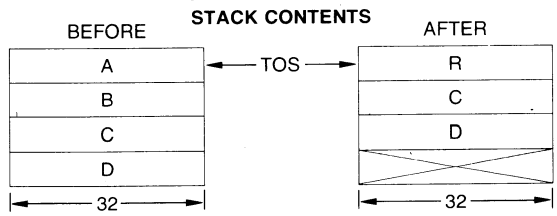
Description:

32-bit floating-point operand A at the TOS is multiplied by the 32-bit floating-point operand B at the NOS. The normalized result R replaces B and the stack is moved up so that R occupies the TOS. Operands A and B are lost. Operands C and D are unchanged.

Exponent overflow or underflow is reported in the status register, in which case the mantissa portion of the result is correct and the exponent portion is offset by 128.

Status Affected: Sign, Zero, Error Field

STACK CONTENTS



FSUB

32-BIT FLOATING-POINT SUBTRACTION

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	0	1	0	0	0	1

Hex Coding: 91 with sr = 1
11 with sr = 0

Execution Time: 70 to 370 clock cycles for A ≠ 0
26 clock cycles for A = 0

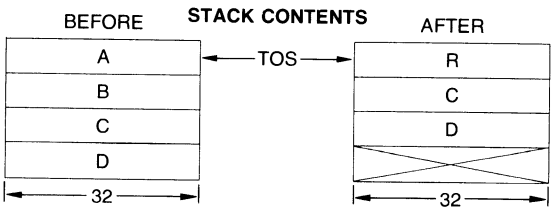
Description:

32-bit floating-point operand A at the TOS is subtracted from 32-bit floating-point operand B at the NOS. The normalized difference R replaces B and the stack is moved up so that R occupies the TOS. Operands A and B are lost. Operands C and D are unchanged.

Exponent alignment before the subtraction and normalization of the result account for the variation in execution time.

Exponent overflow or underflow is reported in the status register in which case the mantissa portion of the result is correct and the exponent portion is offset by 128.

Status Affected: Sign, Zero, Error Field (overflow)



LOG

32-BIT FLOATING-POINT COMMON LOGARITHM

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	0	0	1	0	0	0

Hex Coding: 88 with sr = 1
08 with sr = 0

Execution Time: 4474 to 7132 clock cycles for A > 0
20 clock cycles for A ≤ 0

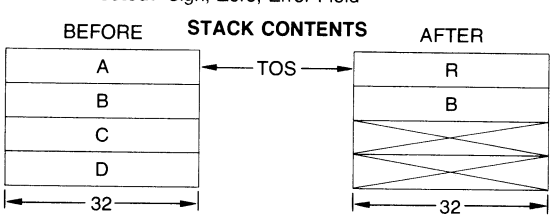
Description:

The 32-bit floating-point operand A at the TOS is replaced by R, the 32-bit floating-point common logarithm (base 10) of A. Operands A, C and D are lost. Operand B is unchanged.

The LOG function accepts any positive input data value that can be represented by the data format. If LOG of a non-positive value is attempted an error status of 0100 is returned.

Accuracy: LOG exhibits a maximum absolute error of 2.0×10^{-7} for the input range from 0.1 to 10, and a maximum relative error of 2.0×10^{-7} for positive values less than 0.1 or greater than 10.

Status Affected: Sign, Zero, Error Field



LN

32-BIT FLOATING-POINT NATURAL LOGARITHM

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	0	0	1	0	0	1

Hex Coding: 89 with sr = 1
09 with sr = 0

Execution Time: 4298 to 6956 clock cycles for A > 0
20 clock cycles for A≤ 0

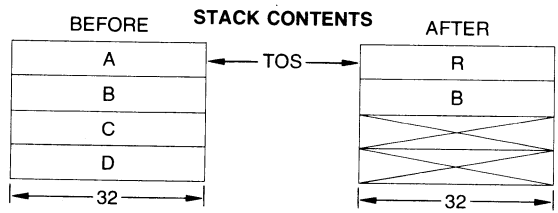
Description:

The 32-bit floating-point operand A at the TOS is replaced by R, the 32-bit floating-point natural logarithm (base e) of A. Operands A, C and D are lost. Operand B is unchanged.

The LN function accepts all positive input data values that can be represented by the data format. If LN of a non-positive number is attempted an error status of 0100 is returned.

Accuracy: LN exhibits a maximum absolute error of 2×10^{-7} for the input range from e^{-1} to e, and a maximum relative error of 2.0×10^{-7} for positive values less than e^{-1} or greater than e.

Status Affected: Sign, Zero, Error Field



NOP

NO OPERATION

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	0	0	0	0	0	0

Hex Coding: 80 with sr = 1
00 with sr = 0

Execution Time: 4 clock cycles

Description:

The NOP command performs no internal data manipulations. It may be used to set or clear the service request interface line without changing the contents of the stack.

Status Affected: The status byte is cleared to all zeroes.

POPD

32-BIT STACK POP

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	1	1	1	0	0	0

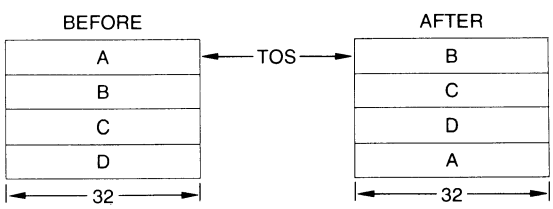
Hex Coding: B8 with sr = 1
38 with sr = 0

Execution Time: 12 clock cycles

Description:
The 32-bit stack is moved up so that the old NOS becomes the new TOS. The previous TOS rotates to the bottom of the stack. All operand values are unchanged. POPD and POPF execute the same operation.

Status Affected: Sign, Zero

STACK CONTENTS



POPS

16-BIT STACK POP

	7	6	5	4	3	2	1	0
Binary Coding:	sr	1	1	1	1	0	0	0

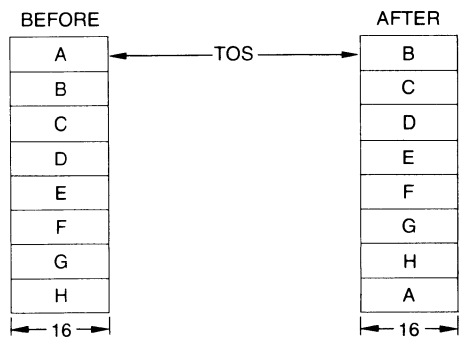
Hex Coding: F8 with sr = 1
78 with sr = 0

Execution Time: 10 clock cycles

Description:
The 16-bit stack is moved up so that the old NOS becomes the new TOS. The previous TOS rotates to the bottom of the stack. All operand values are unchanged.

Status Affected: Sign, Zero

STACK CONTENTS



POPF

32-BIT STACK POP

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	0	1	1	0	0	0

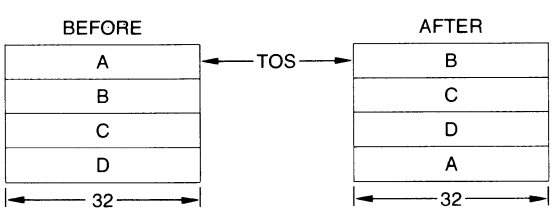
Hex Coding: 98 with sr = 1
18 with sr = 0

Execution Time: 12 clock cycles

Description:
The 32-bit stack is moved up so that the old NOS becomes the new TOS. The old TOS rotates to the bottom of the stack. All operand values are unchanged. POPF and POPD execute the same operation.

Status Affected: Sign, Zero

STACK CONTENTS



PTOD

PUSH 32-BIT TOS ONTO STACK

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	1	1	0	1	1	1

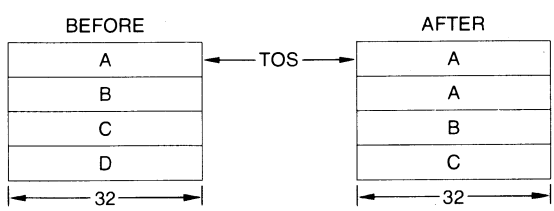
Hex Coding: B7 with sr = 1
37 with sr = 0

Execution Time: 20 clock cycles

Description:
The 32-bit stack is moved down and the previous TOS is copied into the new TOS location. Operand D is lost. All other operand values are unchanged. PTOD and PTOF execute the same operation.

Status Affected: Sign, Zero

STACK CONTENTS



PTOF

PUSH 32-BIT TOS ONTO STACK

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	0	1	0	1	1	1

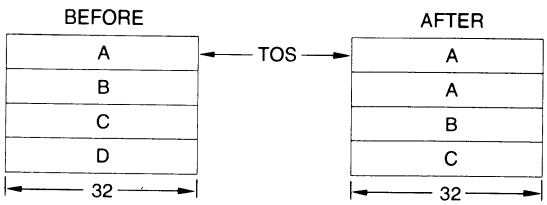
Hex Coding: 97 with sr = 1
17 with sr = 0

Execution Time: 20 clock cycles

Description:
The 32-bit stack is moved down and the previous TOS is copied into the new TOS location. Operand D is lost. All other operand values are unchanged. PTOF and PTOD execute the same operation.

Status Affected: Sign, Zero

STACK CONTENTS



PTOS

PUSH 16-BIT TOS ONTO STACK

	7	6	5	4	3	2	1	0
Binary Coding:	sr	1	1	1	0	1	1	1

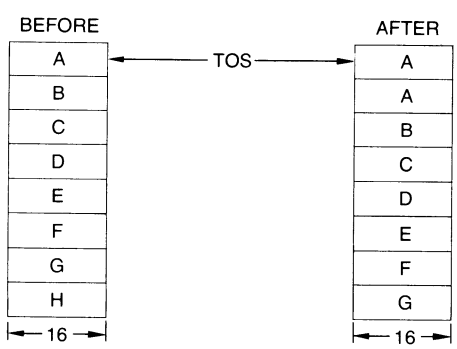
Hex Coding: F7 with sr = 1
77 with sr = 0

Execution Time: 16 clock cycles

Description:
The 16-bit stack is moved down and the previous TOS is copied into the new TOS location. Operand H is lost and all other operand values are unchanged.

Status Affected: Sign, Zero

STACK CONTENTS



PUPI

PUSH 32-BIT FLOATING-POINT π

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	0	1	1	0	1	0

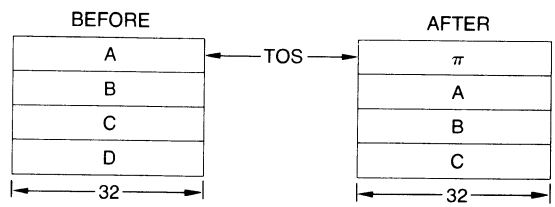
Hex Coding: 9A with sr = 1
1A with sr = 0

Execution Time: 16 clock cycles

Description:
The 32-bit stack is moved down so that the previous TOS occupies the new NOS location. 32-bit floating-point constant π is entered into the new TOS location. Operand D is lost. Operands A, B and C are unchanged.

Status Affected: Sign, Zero

STACK CONTENTS



PWR

32-BIT FLOATING-POINT X^Y

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	0	0	1	0	1	1

Hex Coding: 8B with sr = 1
0B with sr = 0

Execution Time: 8290 to 12032 clock cycles

Description:

32-bit floating-point operand B at the NOS is raised to the power specified by the 32-bit floating-point operand A at the TOS. The result R of B^A replaces B and the stack is moved up so that R occupies the TOS. Operands A, B, and D are lost. Operand C is unchanged.

The PWR function accepts all input data values that can be represented in the data format for operand A and all positive values for operand B. If operand B is non-positive an error status of 0100 will be returned. The EXP and LN functions are used to implement PWR using the relationship $B^A = EXP\,[A(LN\ B)]$. Thus if the term $[A(LN\ B)]$ is outside the range of $-1.0 \times 2^{+5}$ to $+1.0 \times 2^{+5}$ an error status of 1100 will be returned. Underflow and overflow conditions can occur.

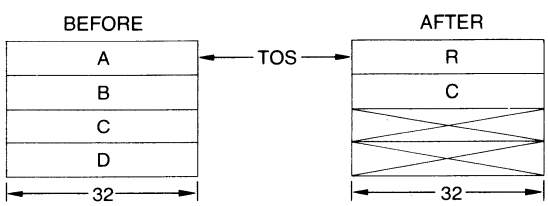
Accuracy: The error performance for PWR is a function of the LN and EXP performance as expressed by:

$|(\text{Relative Error})_{PWR}| = |(\text{Relative Error})_{EXP} + |A(\text{Absolute Error})_{LN}|$

The maximum relative error for PWR occurs when A is at its maximum value while $[A(LN\ B)]$ is near 1.0×2^5 and the EXP error is also at its maximum. For most practical applications the relative error for PWR will be less than 7.0×10^{-7}

Status Affected: Sign, Zero, Error Field

STACK CONTENTS



SADD

16-BIT FIXED-POINT ADD

	7	6	5	4	3	2	1	0
Binary Coding:	sr	1	1	0	1	1	0	0

Hex Coding: EC with sr = 1
6C with sr = 0

Execution Time: 16 to 18 clock cycles

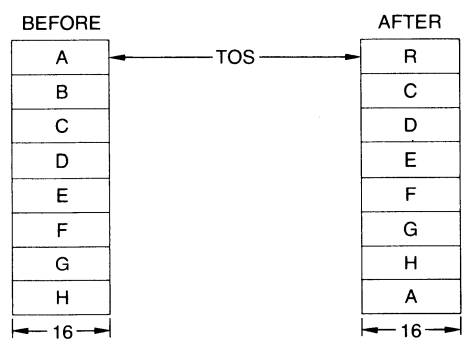
Description:

16-bit fixed-point two's complement integer operand A at the TOS is added to 16-bit fixed-point two's complement integer operand B at the NOS. The result R replaces B and the stack is moved up so that R occupies the TOS. Operand B is lost. All other operands are unchanged.

If the addition generates a carry bit it is reported in the status register. If an overflow occurs it is reported in the status register and the 16 least significant bits of the result are returned.

Status Affected: Sign, Zero, Carry, Error Field

STACK CONTENTS



SDIV

16-BIT FIXED-POINT DIVIDE

	7	6	5	4	3	2	1	0
Binary Coding:	sr	1	1	0	1	1	1	1

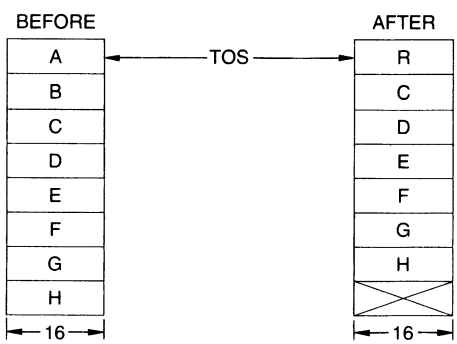
Hex Coding: EF with sr = 1
6F with sr = 0

Execution Time: 84 to 94 clock cycles for A ≠ 0
14 clock cycles for A = 0

Description:
16-bit fixed-point two's complement integer operand B at the NOS is divided by 16-bit fixed-point two's complement integer operand A at the TOS. The 16-bit integer quotient R replaces B and the stack is moved up so that R occupies the TOS. No remainder is generated. Operands A and B are lost. All other operands are unchanged.
If A is zero, R will be set equal to B and the divide-by-zero error status will be reported.

Status Affected: Sign, Zero, Error Field

STACK CONTENTS



SIN

32-BIT FLOATING-POINT SINE

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	0	0	0	0	1	0

Hex Coding: 82 with sr = 1
02 with sr = 0

Execution Time: 3796 to 4808 clock cycles for $|A| > 2^{-12}$ radians
30 clock cycles for $|A| \leq 2^{-12}$ radians

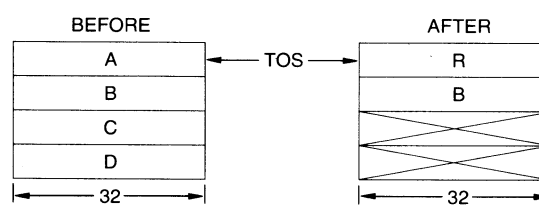
Description:
The 32-bit floating-point operand A at the TOS is replaced by R, the 32-bit floating-point sine of A. A is assumed to be in radians. Operands A, C and D are lost. Operand B is unchanged.

The SIN function will accept any input data value that can be represented by the data format. All input values are range reduced to fall within the interval $-\pi/2$ to $+\pi/2$ radians.

Accuracy: SIN exhibits a maximum relative error of 5.0×10^{-7} for input values in the range of -2π to $+2\pi$ radians.

Status Affected: Sign, Zero

STACK CONTENTS



SMUL

16-BIT FIXED-POINT MULTIPLY, LOWER

	7	6	5	4	3	2	1	0
Binary Coding:	sr	1	1	0	1	1	1	0

Hex Coding: EE with sr = 1
6E with sr = 0

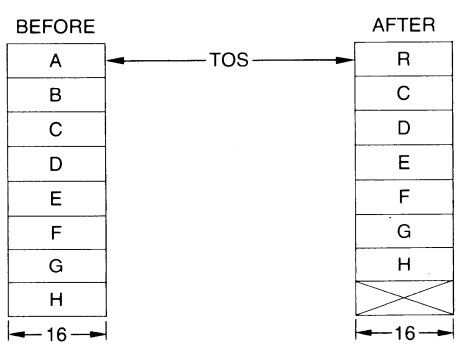
Execution Time: 84 to 94 clock cycles

Description:

16-bit fixed-point two's complement integer operand A at the TOS is multiplied by the 16-bit fixed-point two's complement integer operand B at the NOS. The 16-bit least significant half of the product R replaces B and the stack is moved up so that R occupies the TOS. The most significant half of the product is lost. Operands A and B are lost. All other operands are unchanged. The overflow status bit is set if the discarded upper half was non-zero. If either A or B is the most negative value that can be represented in the format, that value is returned as R and the overflow status is set.

Status Affected: Sign, Zero, Error Field

STACK CONTENTS



SMUU

16-BIT FIXED-POINT MULTIPLY, UPPER

	7	6	5	4	3	2	1	0
Binary Coding:	sr	1	1	1	0	1	1	0

Hex Coding: F6 with sr = 1
76 with sr = 0

Execution Time: 80 to 98 clock cycles

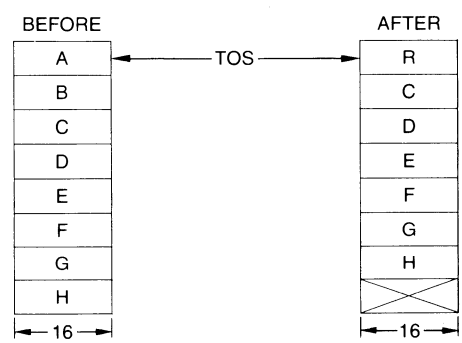
Description:

16-bit fixed-point two's complement integer operand A at the TOS is multiplied by the 16-bit fixed-point two's complement integer operand B at the NOS. The 16-bit most significant half of the product R replaces B and the stack is moved up so that R occupies the TOS. The least significant half of the product is lost. Operands A and B are lost. All other operands are unchanged.

If either A or B is the most negative value that can be represented in the format, that value is returned as R and the overflow status is set.

Status Affected: Sign, Zero, Error Field

STACK CONTENTS



SQRT

32-BIT FLOATING-POINT SQUARE ROOT

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	0	0	0	0	0	1

Hex Coding: 81 with sr = 1
01 with sr = 0

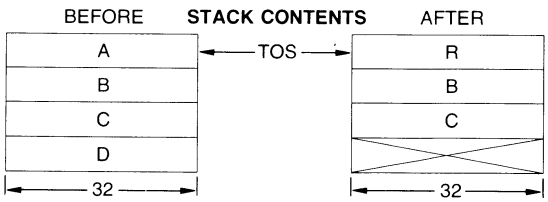
Execution Time: 782 to 870 clock cycles

Description:

32-bit floating-point operand A at the TOS is replaced by R, the 32-bit floating-point square root of A. Operands A and D are lost. Operands B and C are not changed.

SQRT will accept any non-negative input data value that can be represented by the data format. If A is negative an error code of 0100 will be returned in the status register.

Status Affected: Sign, Zero, Error Field



SSUB

16-BIT FIXED-POINT SUBTRACT

	7	6	5	4	3	2	1	0
Binary Coding:	sr	1	1	0	1	1	0	1

Hex Coding: ED with sr = 1
6D with sr = 0

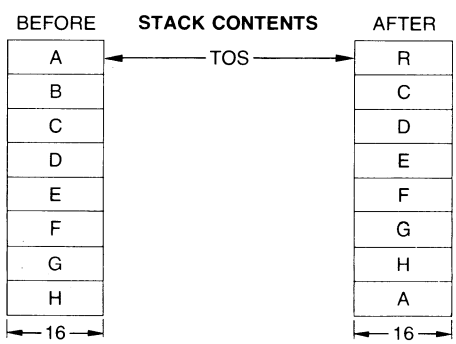
Execution Time: 30 to 32 clock cycles

Description:

16-bit fixed-point two's complement integer operand A at the TOS is subtracted from 16-bit fixed-point two's complement integer operand B at the NOS. The result R replaces B and the stack is moved up so that R occupies the TOS. Operand B is lost. All other operands are unchanged.

If the subtraction generates a borrow it is reported in the carry status bit. If A is the most negative value that can be represented in the format the overflow status is set. If the result cannot be represented in the format range, the overflow status is set and the 16 least significant bits of the result are returned as R.

Status Affected: Sign, Zero, Carry, Error Field



TAN

32-BIT FLOATING-POINT TANGENT

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	0	0	0	1	0	0

Hex Coding: 84 with sr = 1
04 with sr = 0

Execution Time: 4894 to 5886 clock cycles for $|A| > 2^{-12}$ radians
30 clock cycles for $|A| \leq 2^{-12}$ radians

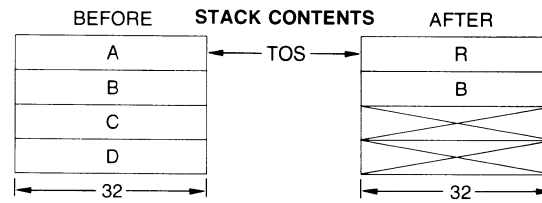
Description:

The 32-bit floating-point operand A at the TOS is replaced by the 32-bit floating-point tangent of A. Operand A is assumed to be in radians. A, C and D are lost. B is unchanged.

The TAN function will accept any input data value that can be represented in the data format. All input data values are range-reduced to fall within $-\pi/4$ to $+\pi/4$ radians. TAN is unbounded for input values near odd multiples of $\pi/2$ and in such cases the overflow bit is set in the status register. For angles smaller than 2^{-12} radians, TAN returns A as the tangent of A.

Accuracy: TAN exhibits a maximum relative error of 5.0×10^{-7} for input data values in the range of -2π to $+2\pi$ radians except for data values near odd multiples of $\pi/2$.

Status Affected: Sign, Zero, Error Field (overflow)



XCHD

EXCHANGE 32-BIT STACK OPERANDS

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	1	1	1	0	0	1

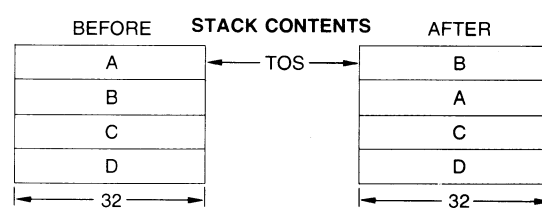
Hex Coding: B9 with sr = 1
39 with sr = 0

Execution Time: 26 clock cycles

Description:

32-bit operand A at the TOS and 32-bit operand B at the NOS are exchanged. After execution, B is at the TOS and A is at the NOS. All operands are unchanged. XCHD and XCHF execute the same operation.

Status Affected: Sign, Zero



XCHF

EXCHANGE 32-BIT STACK OPERANDS

	7	6	5	4	3	2	1	0
Binary Coding:	sr	0	0	1	1	0	0	1

Hex Coding: 99 with sr = 1
19 with sr = 0

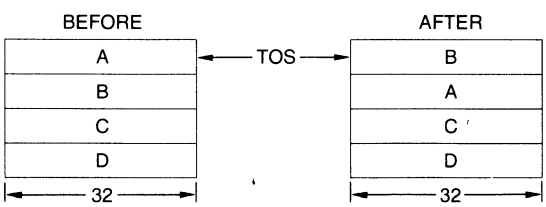
Execution Time: 26 clock cycles

Description:

32-bit operand A at the TOS and 32-bit operand B at the NOS are exchanged. After execution, B is at the TOS and A is at the NOS. All operands are unchanged. XCHD and XCHF execute the same operation.

Status Affected: Sign, Zero

STACK CONTENTS



XCHS

EXCHANGE 16-BIT STACK OPERANDS

	7	6	5	4	3	2	1	0
Binary Coding:	sr	1	1	1	1	0	0	1

Hex Coding: F9 with sr = 1
79 with sr = 0

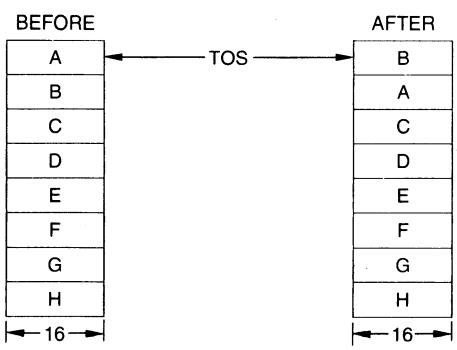
Execution Time: 18 clock cycles

Description:

16-bit operand A at the TOS and 16-bit operand B at the NOS are exchanged. After execution, B is at the TOS and A is at the NOS. All operand values are unchanged.

Status Affected: Sign, Zero

STACK CONTENTS



The Am9517 Multimode Direct Memory Access Controller

TABLE OF CONTENTS

INTRODUCTION

General

Direct Memory Access (DMA), also sometimes known as "channel I/O" or "cycle stealing", has long been a feature of mini- and mainframe computer architectures. It was developed as a means to provide data transfer between system memory and peripheral devices at speeds higher than those obtainable under control of the CPU. This is achieved by bypassing the CPU and creating a direct path between memory and the peripheral device.

DMA capability significantly enhances the throughput performance of a processor system. To understand why this is so, recall that a CPU exercises its functions by reading an instruction from memory, decoding it, performing any address calculations necessary to locate operands, and then executing the specified operation. These are necessary steps with any processor, and it may take several instruction fetch/execute sequences to transfer each byte or word. For repetitive sequential data movement operations, the CPU can be removed from the transfer path and the normal fetch/execution steps simplified.

As an example, a data acquisition subroutine flow chart is illustrated in Figure 1. The subroutine stores bytes of data from an external source into successive memory locations. The main loop consists of several instructions requiring many clock cycles for each word transferred.

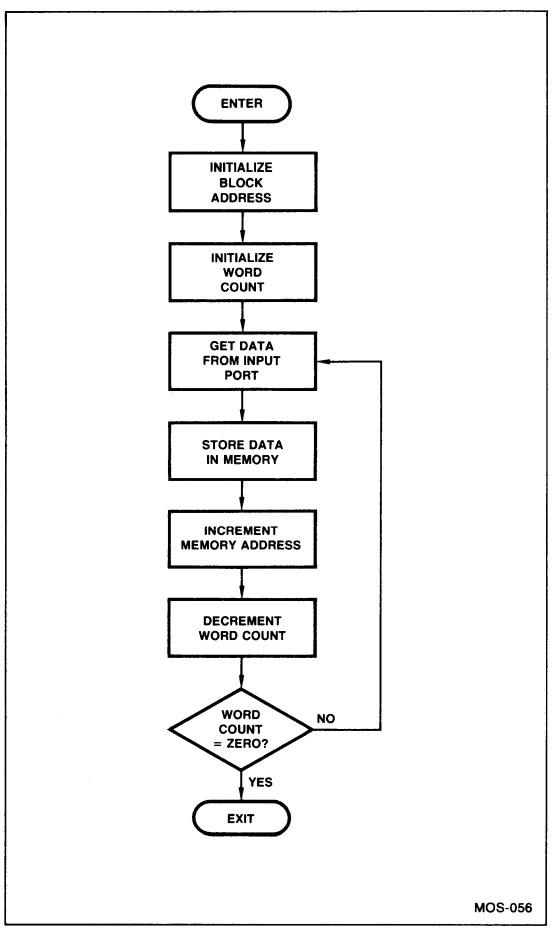


Figure 1. Block Transfer Flow Chart.

However, if what is required is to transfer a complete block of data between a source and a destination, a great deal of overhead can be eliminated by specialized hardware logic which provides access to system memory without CPU intervention. Direct Memory Access (DMA) consists of replacing the functions in the software loop with dedicated hardware. This can reduce the number of cycles required per word transferred and dramatically increase the information transfer rate.

For a more concrete comparison, the flow chart of Figure 1 has been coded in 8080A/8085 assembly language as shown in Figure 2. The transfer loop takes 10 bytes of program and executes in 46 clock cycles per byte. The same task executed in the Am9517 DMA Controller requires a little more initialization time but results in a transfer loop that takes only 3 clock cycles per byte (and an optional operating mode allows transfers only 2 clocks long for extra high speed). Thus, DMA operation can provide throughput gains of much more than an order of magnitude.

Architectural and semiconductor processing developments have occurred rapidly since the introduction of the first 8-bit general purpose microprocessor in 1973. Basic instruction execution times and minimum system component counts have both improved by more than an order of magnitude. CPU costs have fallen from several hundred dollars to well under ten dollars. The result has been an unprecedented growth in the applications for microprocessors. Furthermore, during this same interval, the 8-bit microprocessor that was originally conceived as a smart controller has evolved into a sophisticated computing element. This evolution has generated a concomitant need for efficient and high speed I/O transfers which is the forte' of direct memory access.

The ever increasing density of MOS/LSI has allowed the considerable amount of logic required within a useful direct memory access controller to be almost entirely incorporated on a single chip. Indeed, the only reason that more than one chip is required is the limitation on the number of pins available in industry-standard packages.

```
LOC   OBJ          SEQ     SOURCE STATEMENT
                     1 ;
                     2 ;     SUBROUTINE TO MOVE A BLOCK OF DATA
                     3 ;     FROM AN INPUT PORT INTO MEMORY
                     4 ;
                     5 ;
                     6 ;
                     7       EXTRN MEMA,CNT
                     8 ;
0001                 9 PORT1 EQU 01H       ;INPUT PORT NO. 1
                    10 ;
                    11       CSEG
                    12 ;
0000  210000   E    13 BM17:  LXI H,MEMA    ;INIT. MEMORY ADDRESS
0003  010000   E    14        LXI B,CNT     ;INIT. WORD COUNT
0006  DB01          15 LOOP:  IN PORT1      ;READ FROM INPUT PORT
0008  77            16        MOV M,A       ;STORE DATA IN MEMORY
0009  23            17        INX H         ;INCREMENT MEMORY POINTER
000A  0B            18        DCX B         ;DECREMENT WORD COUNT
000B  78            19        MOV A,B       ;TEST IF WORD COUNT = 0?
000C  B1            20        ORA C
000D  C20600   C    21        JNZ LOOP      ;LOOP UNTIL DONE
0010  C9            22        RET
                    23 ;
                    24 ;
                    25        END
```

Figure 2. Programmed Block Transfer.

Various forms of DMA control have been implemented in the past. One approach is to interleave individual memory transfers with continuing CPU memory operations. This allows "transparent" DMA, but does not take advantage of the available memory bandwidth, plus the interface and control logic becomes very CPU-specific.

The Am9517 uses another technique where it takes over complete system control and can therefore make full use of the memory speed. This Application Note describes the Am9517 developed by Advanced Micro Devices. In addition to a full description of the part and its various modes of operations, implications and configuration suggestions are made to aid the system designer.

Am9517 Overview

The functional specification of the Am9517 Multimode Direct Memory Access Controller was developed to offer a very general DMA capability with a wide range of programmable options, many system-oriented features, and a general purpose interface facilitating the use of the device with a wide range of system architectures.

Careful study of the needs of a wide variety of applications which could benefit from DMA capability indicated the need for a minimum (but expandable) set of four separate and independent channels. Each channel in the Am9517 has associated with it two 16-bit registers which contain the current address and current word count information and two more registers which contain the base address and base word count. The base registers permit any channel to be automatically re-initialized at the end of a transfer. In addition, each channel has associated with it a 6-bit mode register which determines the types of transfers and options to be executed.

Overriding control of the operation of the DMA controller is provided by a master enable/disable bit in an internal command register. In addition, a four-bit mask register is provided to allow individual channels to be enabled and disabled. An important feature of the mask register is that its contents may be set or cleared in two ways. All four channels may be simultaneously enabled and/or disabled by means of a single command from the CPU. Alternatively, individual channels may be enabled or disabled without disturbing the status of the other channels. The use of this latter technique makes it unnecessary for the system software to maintain the mask status of all channels when changing just one.

Priority resolution logic is provided in order to resolve potential conflicts among requests for DMA service. Two software-selectable priority strategies are available to the system designer. Fixed priority gives the highest priority to channel 0 and the lowest to channel 3. Rotating priority maintains the same relative order as fixed priority, but assigns the lowest priority to the channel last serviced, thus preventing any one channel from monopolizing the controller.

Each of the channels operates in one of four modes. In the Single transfer mode one word is transferred in response to each DMA request of the channel. Block transfer mode causes the DMA controller to make continuous transfers until the word count for the active channel goes to 0. Demand transfer mode makes transfers as long as the request for DMA service is active and the word count for the channel is non-zero. The fourth mode of operation, called the cascade mode, is used to provide nearly unlimited expansion of the number of DMA channels available. A channel operating in cascade mode responds to a DMA request from a cascaded DMA controller by issuing a request to the CPU for control of the bus in the usual way. Acknowledgement by the CPU of the request is passed on to the cascaded controller by acknowledging the DMA request. No other address or control signals are activated by a cascade mode channel.

Two of the channels of the Am9517 can be used to provide memory-to-memory transfer capability. This feature offers very fast transfers of data blocks within system memory and is especially valuable in editing, initialization and other data movement operations. Channel 0 provides the source address while channel 1 provides the destination address and word count. A programmable feature of the memory-to-memory transfer operation is the ability to hold the source address constant. This allows the data contained in a single memory location to be replicated at very high speed throughout a block of memory.

Other programmable features which apply to all modes include the ability to select either incrementing or decrementing of the current address during transfers, a compressed timing feature which allows transfers to be executed in just two clock cycles, and the ability to select the active sense of the DMA Request and DMA Acknowledge signals.

A software DMA request capability is included which allows DMA transfers to be initiated by the processor on any channel. This powerful feature permits the processor itself to take full advantage of the capability of the DMA controller. An external hardware input is provided that allows the system to terminate a transfer when desired.

The Am9517 makes use of Advanced Micro Devices' LINOX N-channel silicon gate MOS technology. This process utilizes low profile structures, triple ion implantation, and both depletion and enhancement transistors to achieve very dense, high speed, low power circuitry. The chip contains 6350 transistors, has a total area of 41,580 square mils and is packaged in a standard 40-pin dual in-line package.

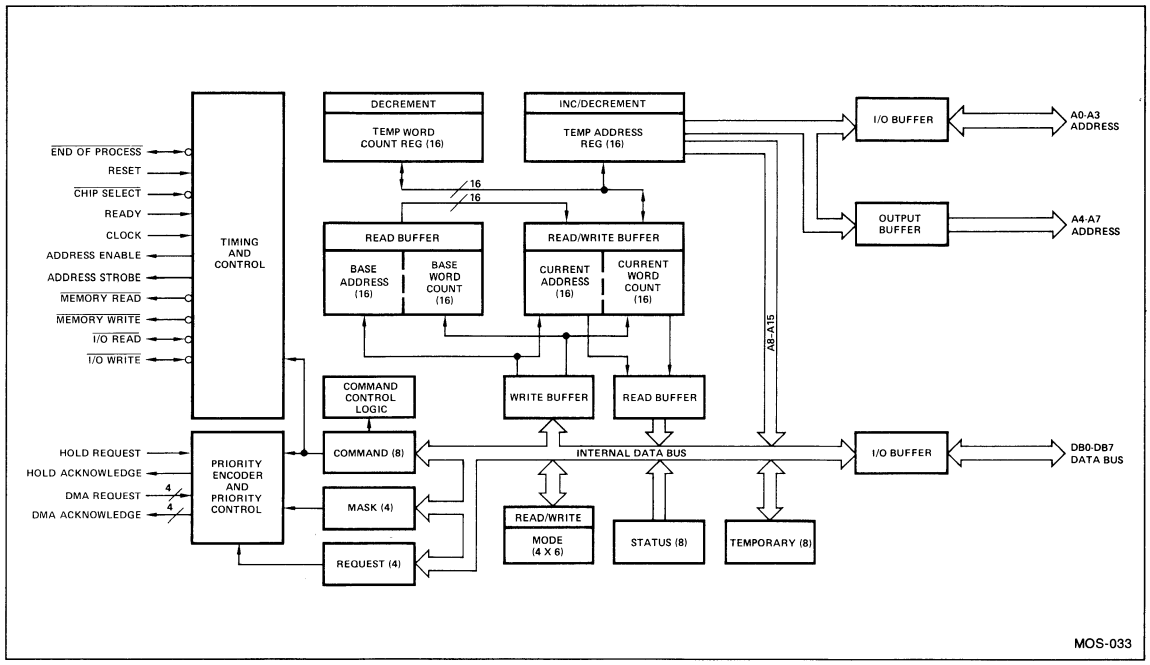


Figure 3. Am9517 Block Diagram.

INTERFACING

Block Diagram

The block diagram of the Am9517 (Figure 3) shows all of the interface signals in addition to the internal functional blocks and their data interconnections.

A peripheral device requiring service generates a DMA request to the Am9517. If the channel receiving the request is enabled, a Hold Request to the system CPU is issued by the controller. When the CPU relinquishes control over the system busses, a Hold Acknowledge signal is output to the DMA controller to indicate that transfers may begin. On receipt of Hold Acknowledge the Am9517 issues a DMA Acknowledge to the highest priority, unmasked requesting device and begins issuing the control signals and addresses necessary to effect the desired transfers. Upon completion or termination of the transfer the Hold Request and DMA Acknowledge signals are terminated and the CPU regains control of the system busses. This procedure allows the DMA Controller to take full advantage of the available memory bandwidth and provides the greatest possible flexibility for transfer timing.

In order to establish the required operating characteristics within the DMA controller, internal registers are loaded under software control by the CPU. The numerous internal registers are addressed by means of the four least significant address lines (A0 through A3) which are thus made bidirectional. Address lines A4 through A7 are output by the controller and the eight high order address bits (A8 through A15) are demultiplexed from the data bus using the Address Strobe signal. The high order address byte is stored in an external latch and supplied to the address bus when required by the Address Enable (AEN) output signal. The I/O Read and I/O Write signals, in conjunction with Chip Select and the low order address bits, are used by the CPU to communicate with the controller.

During a DMA transfer the controller generates the combinations of read and write signals necessary to effect the transfers, using the Ready input, where necessary, to synchronize timing. End-Of-Process is a bidirectional signal which, as an output, indicates that a DMA transfer has been completed and, as an input, may be used to terminate any current transfer.

Interface Considerations

All of the input and output signals of the Am9517 are specified with worst-case levels identical to those of standard TTL circuits. Input logic levels are 2.0V high and 0.8V low; output logic levels are 2.4V high and 0.4V low. Thus, the normal worst-case noise immunity of 400mV offered by standard TTL logic is maintained. The logic level specifications take into account worst-case combinations of the three variables that effect the logic level thresholds: ambient temperature, supply voltage and processing parameters. Actual operating margins will be better than worst-case to the extent that these variables depart from worst-case conditions.

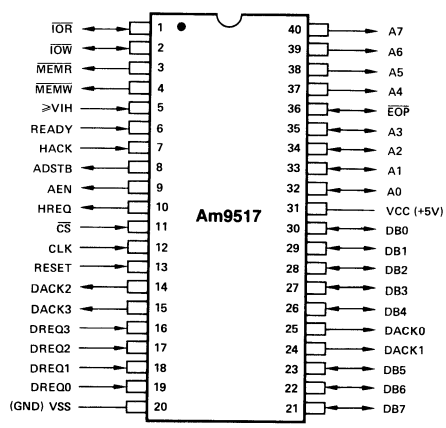
All outputs source at least 200 microamps at 2.4V. The Hold Request output is also specified for 100 microamps source current at 3.3V. All outputs sink a minimum of 3.2 milliamps at 0.4V. All the interface signals of the Am9517 are summarized by type in Figure 4a and their pin assignments are shown in Figure 4b.

The very high resistance of open gate MOS transistors exposes the device's input circuits to the risk of damaging accumulations of static charge. If charge enters the gate node of such an input faster than it can be discharged, the gate voltage can rise high enough to cause oxide breakdown, thus damaging or destroying the transistor.

All inputs to the Am9517 include protection networks designed to slow the transition times of incoming current surges and to provide low impedance discharge paths for voltages beyond normal

Signal Name	Abbreviation	Type	No. of Pins
Clock	CLK	Input	1
Chip Select	$\overline{CS}$	Input	1
Reset	RESET	Input	1
Ready	READY	Input	1
Hold Acknowledge	HACK	Input	1
DMA Request	DREQ0-DREQ3	Input	4
Hold Request	HREQ	Output	1
DMA Acknowledge	DACK0-DACK3	Output	4
Address Bus 4-7	A4-A7	Output	4
Address Strobe	ADSTB	Output	1
Address Enable	AEN	Output	1
Memory Read	$\overline{MEMR}$	Output	1
Memory Write	$\overline{MEMW}$	Output	1
I/O Read	$\overline{IOR}$	Input/Output	1
I/O Write	$\overline{IOW}$	Input/Output	1
Data Bus	DB0-DB7	Input/Output	8
Address Bus 0-3	A0-A3	Input/Output	4
End of Process	$\overline{EOP}$	Input/Output	1
+5 Volts	VCC	Power	1
Ground	VSS	Power	1

(a) Signal Summary.



(b) Connection Diagram.

MOS-034

Figure 4. Am9517 Interface Signals.

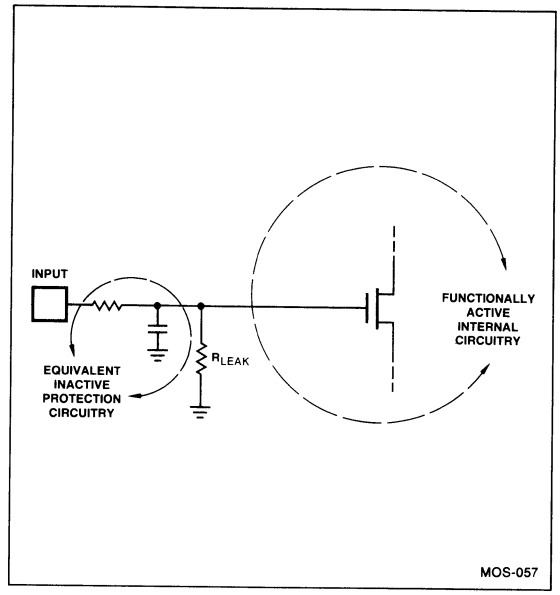


Figure 5. Input Circuitry.

operating levels. Note, however, that careless handling of MOS components can result in transfers of charge which cannot be absorbed without damage and conventional MOS handling precautions should be observed at all times.

In normal operation the input protection circuitry is inactive and may be considered as a lumped series RC network as shown in Figure 5. The active input connection during normal operation is the gate of an MOS transistor. No active sources or drains are connected to the inputs so that neither transient nor steady state currents are impressed upon the driving signals by the Am9517. The input signal is required only to charge or discharge the input capacitance and to overcome the leakage associated with the protection network and input circuit. Input capacitances are typically 6pF and leakage currents are usually less than 1μA. As is typical with MOS components, input drive specifications will usually be limited by transition time considerations rather than DC current limitations.

Good MOS design practice dictates that all inputs be terminated in order to provide discharge paths for transients. Unused inputs should be tied directly to ground or VCC as appropriate. Any input which is driven directly from a card edge connector should be terminated on the card in order to protect the input when the connection is broken. A simple pull-up resistor or on-board gate will suffice.

In general, on-chip delays will always track to a great extent and worst/best combinations will never occur together. The rising and falling edges of the read and write control pulses will track to provide minimum active widths.

INTERFACE SIGNALS

Clock

All the internal operations are clocked by this input which is used by the Am9517 to create four internal clocks. The number of operations to be performed within the controller and the high speed at which the device has been specified to operate, impose constraints on the input clock specification as illustrated in Figure 6. As long as the specified minimum high and low times are observed, the designer may use any convenient clock duty cycle. The greatest operating margins, and the best transition time tolerance, occurs when both clock low and clock high times are mutually maximized. Slowing the clock slightly, and thus extending TCY somewhat, also provides room for greater margins.

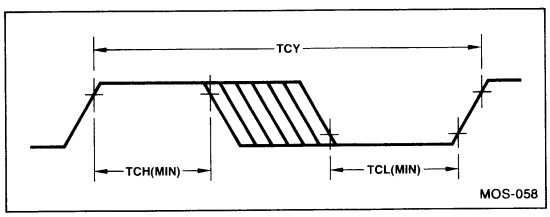


Figure 6. Clock Waveform Specifications.

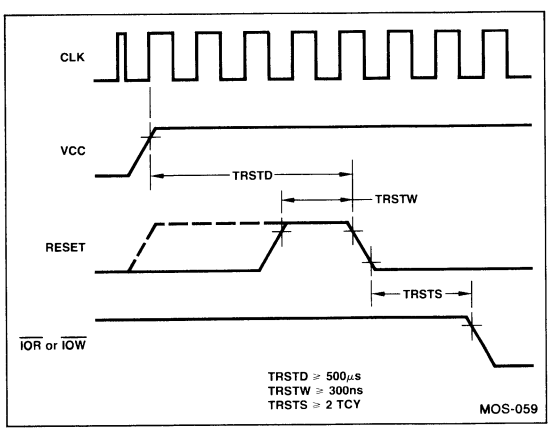


Figure 7. Reset Timing.

Chip Select ($\overline{CS}$)

Chip Select is an active-low input that enables data transfers between the DMA controller and the data bus. It is usually derived from an address output by the CPU to specify the device to be operated upon. The Chip Select input is recognized by the controller only when no active DMA or memory-to-memory transfers are taking place. It is ignored whenever the HACK input is true.

Reset

Reset is an active-high asynchronous input which terminates any operation that may be in progress within the controller. This input also clears the internal control registers, with the exception of the mask register which is set to all ones thus disabling all channels. After a reset the controller is ready to accept initialization commands from the CPU. Reset must be applied for a minimum of 300ns in order to insure that the controller is reset. The end of Reset should occur at least 500μs after both VCC and CLK are stable. At least two clock cycles must elapse following the end of Reset before the first I/O write is applied to the controller. Figure 7 shows the reset timing.

Ready

Ready is an active-high input which can be used to extend the read and write pulses generated by the DMA controller. If the Ready input is low throughout the Ready setup (TRS) and hold (TRH) times as shown in the left portion of Figure 8, the read and write pulses will be extended by one full clock cycle. The right portion of Figure 8 shows extension by two clocks. Ready is tested on the falling edge of each succeeding clock cycle and the read and write pulses are extended in multiple increments of TCY until Ready becomes true prior to the setup time. When utilizing the compressed timing feature (discussed later) to achieve a transfer rate of one word every two clock cycles, care must be taken to insure that Ready is true throughout the setup and hold time prior to the read and write pulses being true. Ready transitions should not occur during the defined setup-hold window in any operating mode.

In addition to extending the width of the Read and Write pulses, the Ready input going low causes the state of the address, data and control lines to be held constant. Note that, just as in the case of the CPU, the Ready input to the DMA controller remaining low for an extended period will hang up the system.

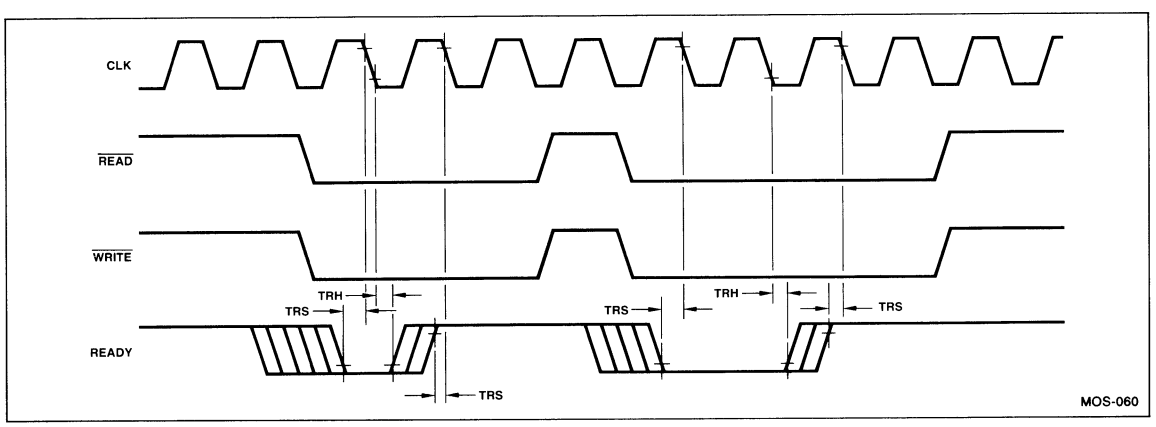


Figure 8. Ready Timing.

Hold Acknowledge (HACK)

The active-high Hold Acknowledge signals the controller that the system busses have been released by the CPU and placed in the high impedance state. This input initiates DMA transfers and should be asserted only in response to the issuance of a request for service by the Am9517 (HREQ). The DMA operations begin with the falling edge of the clock cycle following the satisfaction of the Hold Acknowledge setup time requirement (THS). The Hold Acknowledge input must remain true until the Am9517 relinquishes control of the system busses. The controller requires that one full clock cycle transpire between issuance of a HREQ and receipt of the Hold Acknowledge.

DMA Request (DREQ0-DREQ3)

The four asynchronous DMA Request inputs are used by peripheral devices to request DMA service. The polarity of the DREQ inputs is program selectable to be either active-high or active-low. A reset places them in the active-high condition.

An active DMA request is recognized by the Am9517 at the clock falling edge next following the satisfaction of the DREQ setup time (TQS). Any or all of the DMA request inputs may be active simultaneously and contention is resolved by priority logic contained within the DMA controller. Each Hold Acknowledge received by the controller selects the highest priority unmasked active DMA Request for the next transfer sequence. This means that a DMA transfer must be completed or otherwise terminated in order for a higher priority channel to be serviced.

Once asserted, an active DREQ input should be maintained at least until the corresponding DACK goes active. The implications of various methods of managing the DREQ signal timing after DACK is returned will depend on the operating mode being used for the associated channel.

Hold Request (HREQ)

The active-high Hold Request output indicates that the Am9517 requires service and is generated whenever an unmasked active DMA Request input is received. Timing of the Hold Request relative to the DREQ input is shown in Figure 9. In order to accommodate processors with higher level input specifications, the Hold Request output is designed to source at least 100 microamps at a VOH of 3.3 volts. The TDQ parameter shown in Figure 9 is specified at both 2.4 volts and 3.3 volts in the Am9517 data sheet. The higher level can be attained without assistance, but the timing specified requires an external pullup resistor.

DMA Acknowledge (DACK)

The four DMA Acknowledge outputs are each associated with one of the DMA Request inputs. Their active levels are selectable under program control. Unlike the DREQ inputs, after a reset the DMA Acknowledge outputs will be in the active-low condition. When a HACK is received from the CPU in response to the HREQ from the DMA controller, the highest priority, active, unmasked DMA Request will be granted service and the DMA Acknowledge output associated with that channel will become active, as shown in Figure 9. The DMA Acknowledge output from the Am9517 remains true until the completion of the requested DMA service and becomes inactive after the Hold Request output becomes inactive as shown in Figure 9. There will never be more than one DACK active at a time. No DACK is issued for memory-to-memory operations.

Address Bus (A0-A15)

In order to accommodate all of the functions provided by the Am9517 within the constraints of a 40-pin package, the 16 bits of address information provided by the device are output on two paths. The least significant eight are output on the eight address lines A0-A7. The four least significant address lines are bidirectional. As inputs they address the internal registers of the Am9517 when programming the device. Address lines A4 through A7 are tri-state outputs which are enabled only during DMA operations. The most significant eight bits of the address are output on the data bus during certain portions of the DMA operation. They can be demultiplexed from the data bus and stored in an external latch. The timing for the address bits and the two associated control lines is shown in Figure 10.

Address Strobe (ADSTB)

The active-high Address Strobe output from the Am9517 is the control signal used to latch the high order address bits (A8-A15) from the data bus into an external register or latch. Note that, as shown in Figure 10, the falling edge of Address Strobe should be used to clock the address bits into the latch; the data bus may not be valid at the rising edge. An important feature of the Am9517 is that the high order address and its associated strobe are issued only when required, namely during the first active cycle of a transfer and thereafter only when a carry or borrow is generated by the least significant address byte. This eliminates a clock cycle from the vast majority of transfers.

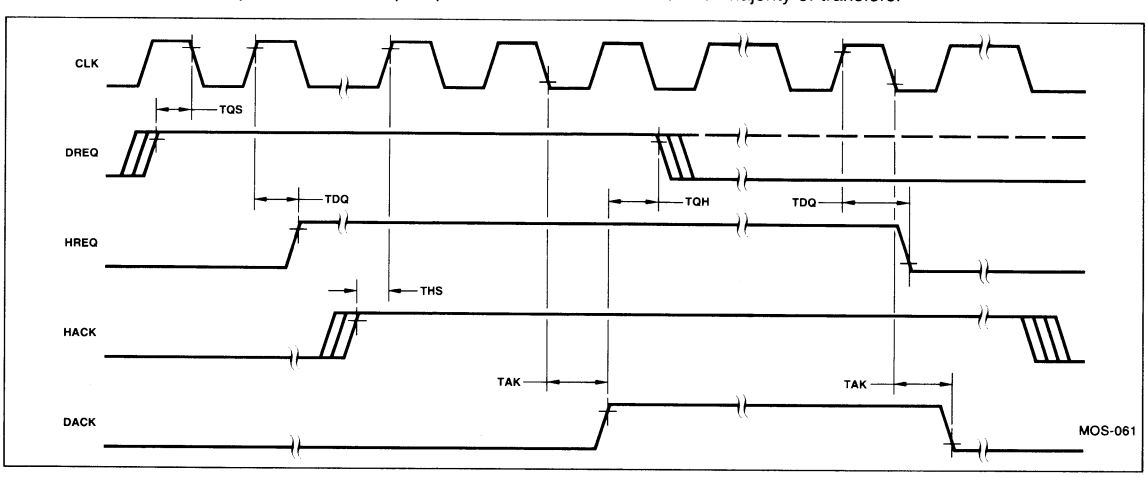


Figure 9. Peripheral and CPU Handshaking Interfaces.

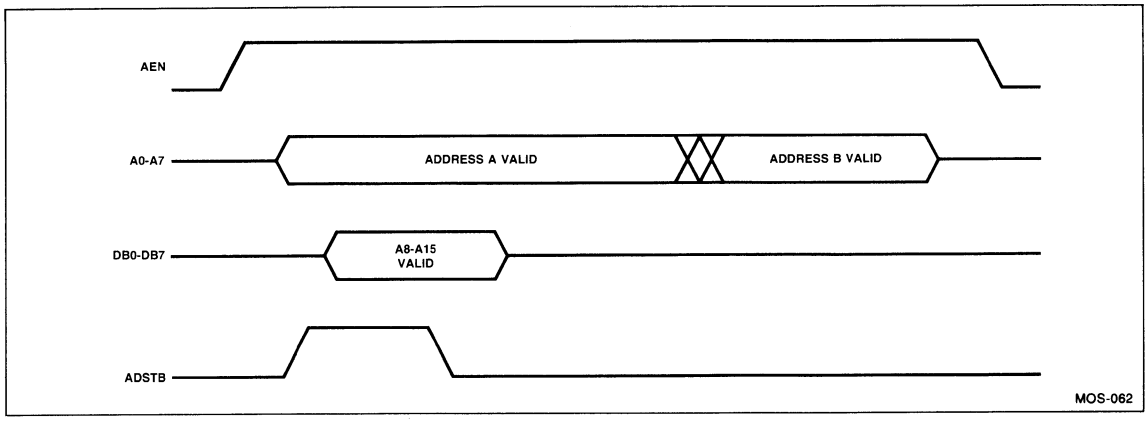


Figure 10. Address Control Relationships.

Address Enable (AEN)

Address Enable is an active-high control signal output by the Am9517 during the first clock cycle of a DMA operation. It remains valid throughout the transfer, as shown in Figure 10. The principal function of this signal is to enable the outputs of the tri-state latch which holds the eight high order address bits. Since the Address Enable output is asserted early in the DMA transfer and remains true until completion, it may also be used to put other system signals into their tri-state condition and to disable system activities such as IO chip select decoding. If AEN is true and all DACK remain false, a memory-to-memory operation is taking place.

Memory Read ($\overline{\text{MEMR}}$)

The transfer of data under the control of the Am9517 requires, in addition to the generation of address information, the provision of control signals to read data from a source location and write it into a destination. These control signals are derived from internally generated read and write signals based upon the type of transfer being executed. The active-low, three-state Memory Read output is used to initiate the reading of data from system memory.

Memory Write ($\overline{\text{MEMW}}$)

The active-low three-state Memory Write output is one of a group of four control signals utilized to initiate the reading and writing of data under the control of Am9517. Its function is to control the writing of data into the system memory.

IO Read ($\overline{\text{IOR}}$)

IO Read is a bidirectional active-low signal. As an output it is used to control the reading of data from an external peripheral port. As an input, IO Read is recognized only if the DMA controller has been selected by the Chip Select input and no DMA operations are underway. If these conditions are met the IO Read input will cause an 8-bit byte to be read from the register addressed by A0-A3 onto the data bus.

IO Write ($\overline{\text{IOW}}$)

IO Write is a bidirectional active-low signal. As an output it is used to control the writing of data into peripheral ports. Like IO Read, this signal will not be recognized as an input unless CS is valid and no DMA operations are in progress. When recognized as an input this signal causes the information on the data bus to be loaded into the Am9517 register addressed by A0-A3.

$\overline{\text{IOR}}$, $\overline{\text{IOW}}$, $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$ operate in pairs to control DMA information transfers. For peripheral-to-memory, $\overline{\text{IOR}}$ and $\overline{\text{MEMW}}$ are both active at the same time. For memory-to-peripheral, $\overline{\text{MEMR}}$ and $\overline{\text{IOW}}$ are both active in the same cycle. For memory-to-memory only $\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$ are used and only one at a time.

End of Process ($\overline{\text{EOP}}$)

End of Process is a bidirectional active-low signal. As an output it is active for a single clock period when the Word Count of an active DMA channel goes to zero. Asserting End of Process as an input causes the termination of DMA operations.

$\overline{\text{EOP}}$ may be used in many ways. As an interrupt, it can inform the CPU that a DMA transfer has occurred. It also can help coordinate peripheral device activity. When channel-specific signals are desired, $\overline{\text{EOP}}$ can be simply gated with individual DACK lines to generate EOP0-EOP3.

Data Bus (DB0-DB7)

The eight bidirectional three-state data bus signals transfer information between the Am9517 and the system data bus. During DMA operations the data bus signals are activated as outputs to supply the high order address byte. Note that the DMA data being transferred does not enter the Am9517 except in the case of memory-to-memory operation. During memory-to-memory operations the data being transferred is stored in a temporary register within the Am9517 between the read and write operations. During memory-to-memory operations the controller cycle which outputs the high order address byte and the address strobe is always present. During programmed IO operations on the Am9517 the data bus is utilized to transfer bytes between the CPU and the DMA controller.

Power (VCC, VSS)

The Am9517 makes use of a single +5 volt power supply and ground. One pin (pin 5) of the device which is not used by the interface must be at a logic high level. An internal pullup resistor is connected to pin 5 to provide the high level when the input is floated. Pin 5 may also be connected directly to VCC. The Am9517 requires a maximum of 150mA at 5V ±5% over the standard operating temperature range of 0°C to 70°C and 175mA at 5V ±10% over the full military temperature range of −55°C to +125°C. These maximum supply currents are worst-case values and apply at the lowest specified temperatures. Supply current always decreases with increasing temperatures; worst-case current at 25°C is 130mA.

REGISTER DESCRIPTION

Figure 11 summarizes the registers contained within the Am9517. The various Address and Word Count registers control locations and numbers of transfers for active operations. The Command, Mode, Mask and Request registers manage the operating options and control features available to the system. Figure 12 shows the addressing used to access the Address and Word Count locations. Notice that A3 is always logic zero for that range of addresses. When A3 is a logic one, other locations are addressed as shown in Figure 13. All operations marked illegal should not be attempted as results will be unknown.

Name	Size	Number
Base Address Registers	16 bits	4
Base Word Count Registers	16 bits	4
Current Address Registers	16 bits	4
Current Word Count Registers	16 bits	4
Temporary Address Register	16 bits	1
Temporary Word Count Register	16 bits	1
Status Register	8 bits	1
Command Register	8 bits	1
Temporary Register	8 bits	1
Mode Registers	6 bits	4
Mask Register	4 bits	1
Request Register	4 bits	1

Figure 11. Am9517 Internal Registers.

Address and Word Count Registers

Each of the four channels provided by the Am9517 has associated with it four 16-bit programmable registers. Two of these, the current address and base address registers, are used to provide address information for data transfer. The current word count and base word count registers determine the number of words to be transferred by a DMA operation.

The base registers are loaded in parallel with the current registers. Two single-byte IO write operations to the same address are used to fill the 16-bit registers. An internal byte pointer flip-flop, which is cleared by a reset, master clear, or by IO command, changes state each time one of the 16-bit registers is accessed. It is used to steer the incoming 8-bit data to the least and most significant halves of the registers.

Two points must be emphasized with regard to the loading of the address and word count registers. First, since the current and base registers are loaded in parallel, no attempt should be made to change the contents of the base register while a DMA service is in progress on that channel. If, for example, transfer concatenation is desired, two channels should be utilized, with the incoming DMA requests being switched between them.

Second, the byte pointer flip-flop toggles automatically upon register access. This requires that care must be taken when accessing these registers other than in the initialization mode. For example, a subroutine which is called as a result of an interrupt and which accesses the address or word count registers should include the IO instruction which clears the byte pointer flip-flop.

Channel	Register	Operation	Interface Signals						Byte Pointer Flip/Flop	Data Bus DB0-DB7
			$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0		
0	Base & Current Address	Write	1	0	0	0	0	0	0	A0-A7
			1	0	0	0	0	0	1	A8-A15
	Current Address	Read	0	1	0	0	0	0	0	A0-A7
			0	1	0	0	0	0	1	A8-A15
	Base & Current Word Count	Write	1	0	0	0	0	1	0	W0-W7
			1	0	0	0	0	1	1	W8-W15
	Current Word Count	Read	0	1	0	0	0	1	0	W0-W7
			0	1	0	0	0	1	1	W8-W15
1	Base & Current Address	Write	1	0	0	0	1	0	0	A0-A7
			1	0	0	0	1	0	1	A8-A15
	Current Address	Read	0	1	0	0	1	0	0	A0-A7
			0	1	0	0	1	0	1	A8-A15
	Base & Current Word Count	Write	1	0	0	0	1	1	0	W0-W7
			1	0	0	0	1	1	1	W8-W15
	Current Word Count	Read	0	1	0	0	1	1	0	W0-W7
			0	1	0	0	1	1	1	W8-W15
2	Base & Current Address	Write	1	0	0	1	0	0	0	A0-A7
			1	0	0	1	0	0	1	A8-A15
	Current Address	Read	0	1	0	1	0	0	0	A0-A7
			0	1	0	1	0	0	1	A8-A15
	Base & Current Word Count	Write	1	0	0	1	0	1	0	W0-W7
			1	0	0	1	0	1	1	W8-W15
	Current Word Count	Read	0	1	0	1	0	1	0	W0-W7
			0	1	0	1	0	1	1	W8-W15
3	Base & Current Address	Write	1	0	0	1	1	0	0	A0-A7
			1	0	0	1	1	0	1	A8-A15
	Current Address	Read	0	1	0	1	1	0	0	A0-A7
			0	1	0	1	1	0	1	A8-A15
	Base & Current Word Count	Write	1	0	0	1	1	1	0	W0-W7
			1	0	0	1	1	1	1	W8-W15
	Current Word Count	Read	0	1	0	1	1	1	0	W0-W7
			0	1	0	1	1	1	1	W8-W15

Figure 12. Address for Word Count and Address Registers.

Interface Signals						Operation
A3	A2	A1	A0	$\overline{IOR}$	$\overline{IOW}$	
1	0	0	0	0	1	Read Status Register
1	0	0	0	1	0	Write Command Register
1	0	0	1	0	1	Illegal
1	0	0	1	1	0	Write Request Register
1	0	1	0	0	1	Illegal
1	0	1	0	1	0	Write Single Mask Register Bit
1	0	1	1	0	1	Illegal
1	0	1	1	1	0	Write Mode Register
1	1	0	0	0	1	Illegal
1	1	0	0	1	0	Clear Byte Pointer Flip/Flop
1	1	0	1	0	1	Read Temporary Register
1	1	0	1	1	0	Master Clear
1	1	1	0	0	1	Illegal
1	1	1	0	1	0	Illegal
1	1	1	1	0	1	Illegal
1	1	1	1	1	0	Write All Mask Register Bits

Figure 13. Register and Function Addressing.

Similarly, if only a single byte of these registers is to be accessed care must be taken to properly maintain the status of the byte pointer.

The Current Address register contains the memory address that is provided by the DMA controller during a transfer on that channel. The Current Address is automatically incremented or decremented, depending upon the programmable option selected, after each word is transferred and so, when read, will indicate the address of the next word to be transferred.

If the autoinitialization feature has been enabled for the channel, the end of a DMA operation, as indicated by either internal or external $\overline{EOP}$, will cause the contents of the Base Address register to be transferred to the Current Address register. Similarly, the Current Word Count register, which is decremented after each word is transferred, may be reinitialized with the contents of the Base Word Count register.

Status Register

This 8-bit read only register, which is accessed by an $\overline{IOR}$ at the address shown in Figure 13, provides the status of the four DREQ inputs and indicates whether a DMA operation has been completed. See Figure 14.

The four least significant bits of the status byte are individually set by an internal or external $\overline{EOP}$ signal. These bits are cleared by a reset, a master clear command, or by reading the status register. Since the status is not retained by the DMA controller after a read, system software will usually save all four of the least significant bits in order to insure that all completed DMA operations, and not merely the one of interest, may be detected.

The four high-order bits of the status register indicate the state of the four DREQ inputs. An active level at DREQ, independent of the programmed DREQ polarity, sets the status bit corresponding to the channel requesting service. Reading the status register has no effect upon these bits.

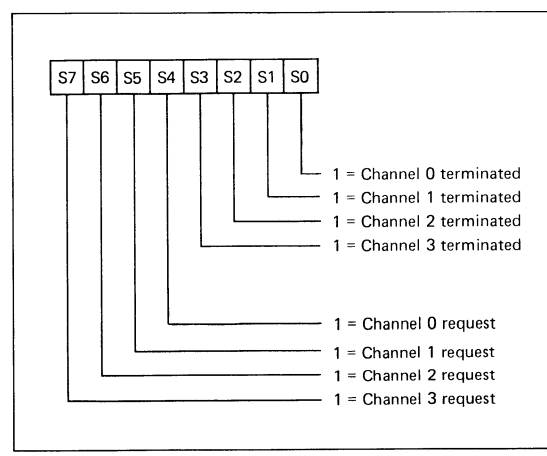


Figure 14. Status Register Bit Assignments.

Command Register

The 8-bit write-only command register is accessed at the location shown in Figure 13. It is cleared by a reset or master clear. Figure 15 indicates the functions carried out by each bit of the command register.

The least significant command bit (C0) controls the memory-to-memory feature. When performing memory-to-memory transfers the Channel 0 Address registers provide the source address, the Channel 1 Address registers provide the destination address and the Channel 1 Word Count registers determine the number of words to be transferred. Memory-to-memory operations are initiated by setting the software DREQ for channel 0.

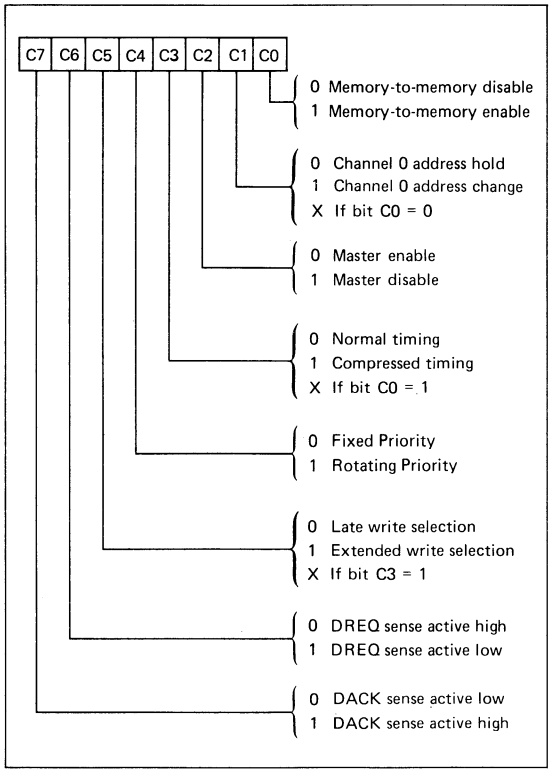


Figure 15. Command Register Bit Assignments.

Transfers proceed at a rate of 8 clock cycles per word. The transfers occur in block mode, that is to say, words will be transferred continuously until the Channel 1 word count reaches 0. It is recommended that Channels 0 and 1 be masked and that the Channel 0 Word Count be set to the same value as that in Channel 1 in preparation for memory-to-memory.

Command bit C1 is effective only if memory-to-memory transfers have been enabled. Under these conditions, setting this bit causes the normal incrementing or decrementing of the Channel 0 Current Address to be inhibited. The result is that the contents of the location defined by the Channel 0 Address register will be written throughout the block of memory defined by the Channel 1 Address and Word Count registers. This feature is useful in applications which require inserting spaces, building histograms and other multiple uses of a single character within data buffers for printers or displays. In some data acquisition applications it is useful to initialize a memory block with an offset value. In displays it will often be convenient to be able to clear screen very rapidly.

Command bit C2 controls the master enable/disable function. When this bit is set the HREQ output of the Am9517 is inhibited, thus preventing any DMA operations from occurring. Note that the entire command register is cleared by a reset or master clear operation, including C2. Although all the hardware DREQ inputs to the Am9517 are disabled by reset, software DMA requests are not masked and should be handled with care.

The compressed timing feature of the Am9517 is selected by means of Command bit C3. Normal timing uses three clock cycles per transfer except when the high-order address bits are output and four clocks are used. Compressed timing removes one clock cycle from each type of transfer thus shortening the transfers to two and three clocks. The effect of this is to reduce the read pulse width by TCY and to cause the read and write pulses to coincide. Where the requirements of system memory and the peripheral controller permit, a substantial increase in throughput can be obtained. This feature is not available during memory-to-memory transfers and the compressed timing bit is ignored if bit zero of the command word is set.

Bit C4 of the command word determines the type of priority arbitration to be utilized in resolving contending active DREQ inputs. If C4 is cleared, the four channels will be prioritized in fixed order, with channel 0 having the highest priority and channel 3 the lowest. If C4 is set, rotating priority is selected. The relative sequence of channel priorities will remain the same; however, upon completion of a DMA operation the most recently serviced channel will become the lowest priority. Thus if channel 2 where the last channel serviced, the order of priority would be channels 3, 0, 1 and 2. Rotating priority prevents a single channel from blocking service to other channels.

Priority arbitration is carried out as the first action of a DMA service upon receipt of the HACK input to the DMA controller. Thus, the highest priority unmasked DREQ input or software DMA request present at that time will be selected for service. Once a channel has been selected for service, control remains with that channel until the service is terminated. HREQ is relinquished following each service so reprioritization will occur.

When the cascade mode of operation is in use, service requests from cascaded DMA controllers are prioritized just like any other DREQ input before being passed on.

Bit C5 of the command register controls the Write pulse width and placement relative to the Read pulse. The optional extended write, which may be required for some memory systems or for some special IO requirements, is selected by this bit. The effect is similar to that of the compressed timing feature in that the write pulse becomes active simultaneously with the read pulse, although both are now two clock cycles wide. The extended write control bit is ignored with the compressed timing option is selected.

The last two bits (C6, C7) of the command register control the active levels of the DREQ inputs and DACK outputs. Note that the polarity of the two bits is such that DREQ will be active-high following reset and DACK will be active-low following reset.

Request Register

The 4-bit write-only Request register is accessed at the location shown in Figure 13. Each bit in the request register may be individually set or cleared based upon the state of the three least significant data bus bits. See Figure 16. The two least significant data bus bits select a channel while the third bit determines whether the selected bit is to be set or cleared. All four of the Request register bits are cleared by a reset or master clear. The request bit for an active channel is cleared by an $\overline{EOP}$.

Software DMA requests are nonmaskable but are disabled by the master disable bit in the command word and are subject to priority arbitration. Due to the nonmaskable nature of these requests, they should be issued only at the end of an initialization or other command sequence when all system setup is complete.

Mask Register

The four-bit write-only Mask register provides the capability to disable any or all of the hardware DREQ inputs to the Am9517. In order to provide as much flexibility as possible in controlling the mask bits, two addresses are assigned, as shown in Figure 13.

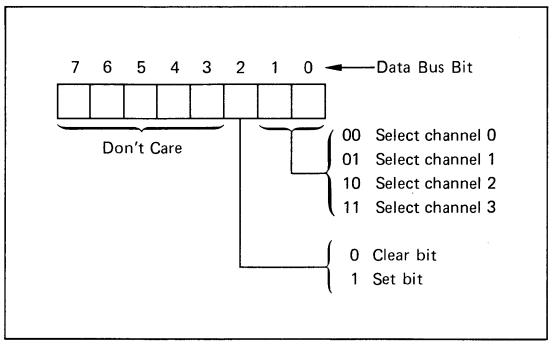


Figure 16. Single Bit Control for Request and Mask Registers.

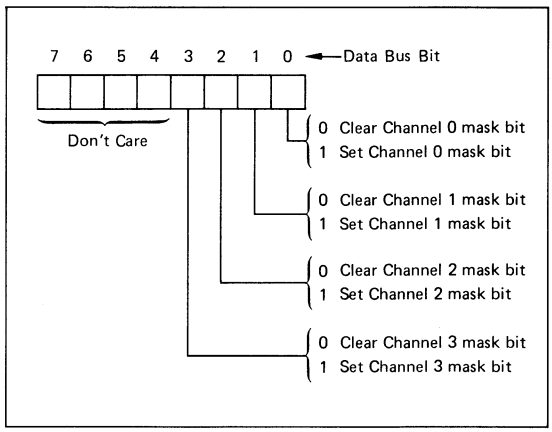


Figure 17. Parallel Mask Loading.

$\overline{IOW}$ commands enabled by $\overline{CS}$ and directed to address 1010 set or clear individual mask bits using the format of Figure 16. Alternatively, all four bits of the mask register may be written with a single command to address 1111. This command utilizes the four least significant data bus inputs to establish the status of the four DMA channels as shown in Figure 17.

In addition to program control of the mask register, the entire register is set by a reset or master clear thus disabling all external DMA requests. Furthermore, an $\overline{EOP}$ on an active channel not programmed to autoinitialize will set the corresponding bit in the mask register. This is done to prevent another DMA transfer from occurring before new address and word data have been set up. Software DMA requests are not maskable.

Mode Register

Each of the four DMA channels has an independent 6-bit write-only Mode register associated with it. This register is accessed at the location shown in Figure 13. When accessing the Mode registers the two least significant data bus inputs select the mode register to which the remaining 6 bits are to be transferred, as shown in Figure 18. These six bits determine the type of transfer, its mode, whether the transfers are to be in ascending or descending order, and whether autoinitialization is to be utilized.

Three types of transfer are selectable by the two least significant bits of the mode register (M2, M3). The verify transfer is a dummy operation during which all program selected functions of the Am9517 are executed except that the read and write control outputs are disabled. This permits the device and its addresses to be exercised without actually transferring data and can be used to verify proper operation of the controller.

The read transfer moves data from system memory to an IO device by activating the $\overline{MEMR}$ and $\overline{IOW}$ control outputs of the Am9517. Write transfers utilize the $\overline{IOR}$ and $\overline{MEMW}$ control lines to move data from an IO device to system memory. The fourth possible combination of M2, M3 is an undefined state and should not be used. If the channel has been programmed for cascade operation the type of transfer is determined by the attached controller and bits M2, M3 are ignored.

Mode bit M4 specifies the autoinitialization option for the channel. When M4 = 0, the Current Address and Word Count registers are not affected by $\overline{EOP}$ and the associated mask bit is set, disabling the channel. When M4 = 1, occurrence of $\overline{EOP}$ causes the contents of the Base Address and Word Count registers to be transferred into the respective Current Address and Word Count registers. The mask bit is not set.

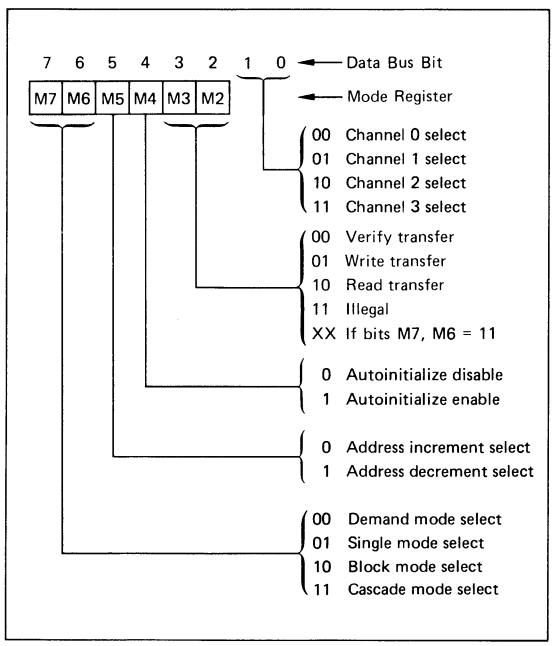


Figure 18. Mode Register Addressing and Assignments.

Autoinitialization allows repetitive DMA operations to proceed without software intervention between blocks. Since each channel has independent base registers, each can be independently autoinitialized without disturbing other channels.

Mode bit M5 specifies the address increment/decrement option for the channel. When M5 = 0 the address will increment following each transfer. When M5 = 1 the address will decrement following each transfer. This feature allows significant versatility in data movement. Blocks that may arrive from peripherals in reverse can be written in descending order in memory so that they end up being forward in memory. With the source incrementing and the destination decrementing, a memory-to-memory move can invert a list.

Memory-to-memory control can override the M5 bit for channel 0, forcing the address to neither increment nor decrement. See the Command Register description for details.

Mode bits M6 and M7 specify one of four available operating modes for the channel. These types of transfer management provide versatility for the interface between the peripheral device and the DREQ input to the Am9517. One mode is also provided to greatly simplify expansion of the DMA system. All DMA transfers are initiated by an active-going DREQ signal. (Memory-to-memory transfers are initiated by a software request.) All DMA transfers are terminated by an internal (word count = 0) or external $\overline{EOP}$, and by a reset or master clear. The following mode descriptions indicate methods for managing transfers between initiation and final termination.

When M7,M6 = 00 Demand mode is selected. Once the DREQ has been accepted, continuous transfers will occur until the DREQ goes inactive (or until $\overline{EOP}$). When DREQ returns active, transfers will resume where they left off. This allows the requesting device to control the lengths of sub-block-sized bursts of transfers.

For example, if DREQ is cleared at the time that DACK is received, only one word will be transferred. Alternatively, if DREQ is cleared at the time that the internal $\overline{EOP}$ goes active, a complete block (as defined by the word count) will be transferred. Between those extremes Demand mode allows interaction of system activities with DMA transfers. A memory refresh cycle can be executed in the midst of a transfer; availability of external data can control the transfer duty cycle.

When M7,M6 = 01 the Single mode is selected. It operates in two ways. This mode always returns system control to the CPU following each word transferred. If DREQ is then inactive, transfers do not continue. If DREQ remains active transfers will continue (as long as word count is greater than zero) but will always be interleaved with a full HREQ/HACK handshake with the CPU. In the case of the 8080A, this means that machine cycles will alternate with transfers of single words. Notice that the recurring arrival of active HACK means that priority will be re-resolved after each Single transfer. If a higher priority request is pending, it will be serviced. Using rotating priority arbitration with several channels set up in Single mode would then interleave a transfer on each channel with CPU machine cycles.

When M7,M6 = 10, the Block mode is selected. Once the DREQ has been acknowledged (DACK), continuous transfers will take place until $\overline{EOP}$ occurs, independent of the state of the DREQ input. Thus a DREQ pulse wide enough to encompass DACK will cause the movement of an entire block of data. Memory-to-memory operations use Block mode exclusively.

When M7,M6 = 11, the channel may be used to cascade an additional Am9517 circuit in order to expand the channel capacity of the DMA system. Any channel or combination of channels at any level may be used for expansion. Two cascaded Am9517 chips provide a net of seven available channels.

A channel used for cascading simply provides access to the internal priority resolution circuitry by bypassing the other functions of the channel. Address, data and control outputs are disabled when a cascade channel is active, allowing the next active chip to be wire-ORed to the system signals.

Byte Pointer Flip/Flop

An internal flip/flop, toggled by each access to 16-bit registers, is used to select the most significant or least significant register byte. An $\overline{IOW}$ operation to address 1100 clears the pointer, causing it to select the least significant byte of the next 16-bit register accessed. The flip/flop is also cleared by a reset or by the master clear command.

Temporary Data Register

The 8-bit Temporary Data register is used during memory-to-memory transfers to provide temporary storage of the data being transferred. Each byte transferred remains in the temporary register until overwritten by the next and may be read out by the CPU. The Temporary Data register is not used during DMA transfers. It is cleared by a reset or a master clear.

Programming

The Am9517 will accept programming from the host processor any time that HACK is inactive; this is true even if HREQ is active. The responsibility of the host is to assure that programming and HACK are mutually exclusive. Note that a logical conflict can occur if the host masks out a DREQ that has just initiated a HREQ: when HACK arrives no valid request may be pending. To prevent this situation it is suggested that the controller be disabled before the channel mask is set, and then that the controller be re-enabled.

After power-up it is suggested that all internal locations, especially the Mode registers, be loaded with some valid value. This should be done even if some channels are unused.

SYSTEM INTERFACE

Software Configurations

Direct Memory Access is, by definition, transparent to the CPU and does not involve direct software. The programmer (and system designer) will, however, be concerned with initialization of the device, subsequent changes to its programmed configuration, and the potential effect on system activities of a device which is capable of suspending CPU operations for indeterminate times and is, when active, beyond control of the CPU.

This section presents a few routines as examples of ways to drive the Am9517. They are shown in 8080A/8085 coding. The comments in the routines plus the surrounding text should provide sufficient guidance to allow translation into other machine languages without difficulty. Similarly, these approaches should be modified and extended to reflect the differing requirements of specific applications.

Figure 19 is an "EQU" table that defines the mnemonic labels used in the routines. The values are taken from Figures 12 and 13 and are written in binary to shown that correspondence. Some programmers may want to translate those entries to octal or hex values. Note that this table assumes that hardware IO port Chip Select decoding for the Am9517 selects zero for system address lines A4 through A7. For other arrangements the four high order bits in each EQU table entry should be changed to the value decoded.

Figure 20 shows a simple, straight-forward routine to configure the Am9517 as part of a system initialization procedure, perhaps following power-on for example. It shows the setup for a single channel – in this case channel 2 – but could easily be expanded to include more channels.

Interrupts are disabled to prevent other routines from possibly disturbing the byte pointer flip/flop. The command byte (line 50) specifies these options:

DACK active low
DREQ active low
Extended Write
Fixed Priority
Normal Timing
Controller Enabled
Address not held
Memory-to-memory off.

This routine does not use a software DMA request. If it did, the command byte might want to disable the controller until the initialization is complete in order to prevent unwanted transfers. Master Clear blocks hardware-originated DMA transfers by setting all mask bits, but does not prevent software-originated requests.

```
LOC     OBJ     SEQ             SOURCE STATEMENT
                  1 ;
                  2 ;
                  3 ;PORT ASSIGNMENTS FOR AM9517 A0-A3 INPUTS.
                  4 ;
                  5 ;ADDRESS AND WORD COUNT REGISTERS:
                  6 ;
0000              7 ADR0      EQU 00000000B     ;ADDRESS REGISTERS
0002              8 ADR1      EQU 00000010B
0004              9 ADR2      EQU 00000100B
0006             10 ADR3      EQU 00000110B
0001             11 WCT0      EQU 00000001B     ;WORD COUNT REGISTERS
0003             12 WCT1      EQU 00000011B
0005             13 WCT2      EQU 00000101B
0007             14 WCT3      EQU 00000111B
                 15 ;
                 16 ;CONTROL REGISTERS:
                 17 ;
0008             18 STAT      EQU 00001000B     ;STATUS REGISTER
0008             19 CMND      EQU 00001000B     ;COMMAND REGISTER
0009             20 RQST      EQU 00001001B     ;REQUEST REGISTER
000B             21 MODE      EQU 00001011B     ;MODE REGISTER
000D             22 TEMP      EQU 00001101B     ;TEMPORARY DATA REGISTER
000F             23 MSKR      EQU 00001111B     ;FULL MASK REGISTER
000A             24 MSKB      EQU 00001010B     ;SINGLE MASK BIT
                 25 ;
                 26 ;DIRECT COMMANDS:
                 27 ;
000C             28 CLBP      EQU 00001100B     ;CLEAR BYTE POINTER
000D             29 MCLR      EQU 00001101B     ;MASTER CLEAR
                 30 ;
                 31 ;
                 32 ;
```

Figure 19. EQU Table.

```
LOC     OBJ     SEQ         SOURCE STATEMENT
                42 ;
                43 ;
                44 ;SETUP ROUTINE FOR DMA CHANNEL #2
                45 ;
3000            46          ORG 3000H
                47 ;
3000 F3         48 STUP:    DI              ;DISABLE INTERRUPTS.
3001 D30D       49          OUT MCLR        ;MASTER CLEAR.
3003 3E62       50          MVI A,01100000B ;SELECT COMMAND OPTIONS,
3005 D308       51          OUT CMND        ;OUTPUT TO COMMAND PORT.
3007 3E9A       52          MVI A,10011010B ;SELECT MODE OPTIONS,
3009 D30B       53          OUT MODE        ;OUTPUT TO MODE PORT.
300B 3E00       54          MVI A,0         ;FORM LOWER BYTE,
300D D304       55          OUT ADR2        ;OUTPUT TO ADDRESS REG.
300F 3E0F       56          MVI A,0FH       ;FORM UPPER BYTE,
3011 D304       57          OUT ADR2        ;OUTPUT TO ADDRESS REG.
3013 3E07       58          MVI A,7FH       ;FORM LOWER BYTE,
3015 D305       59          OUT WCT2        ;OUTPUT TO WORD COUNT.
3017 3E00       60          MVI A,0         ;FORM UPPER BYTE,
3019 D305       61          OUT WCT2        ;OUTPUT TO WORD COUNT.
301B 3E02       62          MVI A,00000010B ;CLEAR CHANNEL #2
301D D30A       63          OUT MSKB        ;MASK BIT.
301F FB         64          EI              ;ENABLE INTERRUPTS.
3020 C9         65          RET             ;RETURN.
                66 ;
                67 ;
                68 ;
```

Figure 20. Simple SETUP Routine.

The mode byte (line 52) specifies these options:

Block transfer mode
Address increment
Autoinitialize
Read transfer.

With the autoinitialization option in effect, this channel will not have to be setup again until the channel function changes. The Read transfer moves data from the system memory out to the peripheral on Channel 2.

The memory addess of the first byte to be transferred is 0F00 hex. The number of bytes to be transferred is 007F hex. In both cases, the upper and lower bytes are output to the same port and are steered internally by the byte pointer flip-flop.

Once the channel is ready to go, its mask can be cleared (line 63) so that it will recognize a DREQ input. Interrupts are then enabled and control returned to the main program. If this routine, or a variation of it, is used as part of a more general system initialization program segment, it may be appropriate to not clear the mask (and possibly to not enable interrupts) until the complete system setup is finished. If this routine is embedded in the midst of application programming, it may be appropriate to omit the Master Clear function and instead to simply set the mask bit for the channel to be changed. In that case it would also be appropriate to clear the byte pointer before the address is output.

General Control Routine

The approach outlined in Figure 20 can be expanded, of course, to include as many channels as desired. In applications where there are variations in the setup data for a given channel, however, this scheme can be awkward. Figure 21 shows a more general design that provides more versatility for many applications.

The SDMA routine picks up the parameters it needs from the calling program. These "in-line" parameters are located immediately following the instruction that calls SDMA. The format is shown at the start of the routine. SDMA first pulls in the mode data which contains the channel number information as well. This is used to index into a branch table that then transfers control to the code segment appropriate for the channel. This portion of the routine then moves the Address and Word Count values from their in-line position into the DMA registers. SDMA assumes that the command configuration has already been established and will not be changed.

Notice that SDMA masks out the channel selected and then clears the mask after the changes are made. Some applications may want to wait until some other point in the program before clearing the mask.

Once SDMA is in place, other configurations and control sequences are easier to implement. For example, the STUP routine in Figure 20 can then be accomplished by inserting a CALL SDMA procedure at line 52 and eliminating lines 52 through 64.

```
LOC     OBJ       SEQ          SOURCE STATEMENT
                   75 ;
                   76 ;
                   77 ;GENERAL PURPOSE ROUTINE TO SETUP DMA CHANNELS
                   78 ;FOR THE AM9517. SETUP PARAMETERS ARE PASSED
                   79 ;IN-LINE FROM THE CALLING PROGRAM.
                   80 ;
                   81 ;
                   82 ;
                   83 ;CALL FORMAT:
                   84 ;        CALL SDMA
                   85 ;        (MODE BYTE)
                   86 ;        (LOW ADDRESS BYTE)
                   87 ;        (HIGH ADDRESS BYTE)
                   88 ;        (LOW WORD COUNT BYTE)
                   89 ;        (HIGH WORD COUNT BYTE)
                   90 ;
                   91 ;
                   92 ;
3000               93          ORG 3000H
                   94 ;
                   95 ;
                   96 ;
3000 E3            97 SDMA:  XTHL              ;GET ADDRESS OF MODE BYTE.
3001 7E            98        MOV A,M           ;GET MODE BYTE.
3002 23            99        INX  H            ;POINT TO NEXT PARAMETER
3003 E3           100        XTHL              ;AND REPLACE ADDRESS.
3004 D30B         101        OUT  MODE         ;MODE BYTE TO MODE PORT.
3006 E603         102        ANI  03H          ;ISOLATE CHANNEL #
3008 F604         103        ORI  04H          ;FORM MASK BIT FORMAT AND
300A D30A         104        OUT  MSKB         ;MASK OUT THE BIT.
300C E603         105        ANI  03H          ;RE-ISOLATE CHANNEL # AND
300E 07           106        RLC               ;MULTIPLY BY 2.
300F 217C30       107        LXI  H,BTAB       ;GET BRANCH TABLE ADDRESS
3012 85           108        ADD  L            ;AND INDEX INTO TABLE BY
3013 6F           109        MOV L,A           ;TWICE THE CHANNEL #.
3014 D21830       110        JNC  BBB          ;COMPLETE 16 BIT ADDRESS
3017 24           111        INR  H            ;IF NECESSARY
3018 5E           112 BBB:   MOV E,M           ;USING INDEXED TABLE
3019 23           113        INX  H            ;POINTER, ASSEMBLE
301A 56           114        MOV D,M           ;BRANCH ADDRESS AND
301B EB           115        XCHG              ;MOVE IT INTO H,L.
301C D30C         116        OUT  CLBP         ;CLEAR BYTE POINTER.
301E F3           117        DI                ;DISABLE INTERRUPTS
301F E9           118        PCHL              ;BRANCH TO CODE SEGMENT
                  119                          ;FOR SELECTED CHANNEL.
                  120 ;
                  121 ;
                  127 ;
                  128 ;
3020 E1           129 CH0:   POP  H            ;ADDRESS AND WORD COUNT
3021 7E           130        MOV A,M           ;PARAMETERS ARE
3022 D300         131        OUT  ADR0         ;FETCHED FROM CALLING
3024 23           132        INX  H            ;PROGRAM AND OUTPUT
3025 7E           133        MOV A,M           ;TO CHANNEL 0.
3026 D300         134        OUT  ADR0
3028 23           135        INX  H
3029 7E           136        MOV A,M
302A D301         137        OUT  WCT0
302C 23           138        INX  H
```

Figure 21. General Purpose SETUP Routine.

```
LOC  OBJ    SEQ     SOURCE STATEMENT
302D 7E     139     MOV A,M
302E D301   140     OUT WCT0
3030 23     141     INX H
3031 FB     142     EI
3032 3E00   143     MVI A,0
3034 D30A   144     OUT MSKB        ;CLEAR #0 MASK.
3036 E9     145     PCHL            ;BRANCH TO CALLER.
            146 ;
            147 ;
3037 E1     148 CH1: POP H          ;ADDRESS AND WORD COUNT
3038 7E     149     MOV A,M         ;PARAMETERS ARE
3039 D302   150     OUT ADR1        ;FETCHED FROM CALLING
303B 23     151     INX H           ;PROGRAM AND OUTPUT
303C 7E     152     MOV A,M         ;TO CHANNEL 1.
303D D302   153     OUT ADR1
303F 23     154     INX H
3040 7E     155     MOV A,M
3041 D303   156     OUT WCT1
3043 23     157     INX H
3044 7E     158     MOV A,M
3045 D303   159     OUT WCT1
3047 23     160     INX H
3048 FB     161     EI
3049 3E01   162     MVI A,01H
304B D30A   163     OUT MSKB        ;CLEAR #1 MASK.
304D E9     164     PCHL            ;BRANCH TO CALLER.
            165 ;
            166 ;
            167 ;
            171 ;
            172 ;
            173 ;
304E E1     174 CH2: POP H          ;ADDRESS AND WORD COUNT
304E 7E     175     MOV A,M         ;PARAMETERS ARE
3050 D304   176     OUT ADR2        ;FETCHED FROM CALLING
3052 23     177     INX H           ;PROGRAM AND OUTPUT
3053 7E     178     MOV A,M         ;TO CHANNEL 2.
3054 D304   179     OUT ADR2
3056 23     180     INX H
3057 7E     181     MOV A,M
3058 D305   182     OUT WCT2
305A 23     183     INX H
305B 7E     184     MOV A,M
305C D305   185     OUT WCT2
305E 23     186     INX H
305F FB     187     EI
3060 3E02   188     MVI A,02H
3062 D30A   189     OUT MSKB        ;CLEAR #2 MASK.
3064 E9     190     PCHL            ;BRANCH TO CALLER.
            191 ;
            192 ;
            193 ;
3065 E1     194 CH3: POP H          ;ADDRESS AND WORD COUNT
3066 7E     195     MOV A,M         ;PARAMETERS ARE
3067 D306   196     OUT ADR3        ;FETCHED FROM CALLING
3069 23     197     INX H           ;PROGRAM AND OUTPUT
306A 7E     198     MOV A,M         ;TO CHANNEL 3.
306B D306   199     OUT ADR3
306D 23     200     INX H
```

Figure 21. General Purpose SETUP Routine. (Cont.)

```
LOC    OBJ      SEQ          SOURCE STATEMENT
306E 7E         201          MOV A,M
306F D307       202          OUT WCT3
3071 23         203          INX H
3072 7E         204          MOV A,M
3073 D307       205          OUT WCT3
3075 23         206          INX H
3076 FB         207          EI
3077 3E03       208          MVI A,03H
3079 D30A       209          OUT MSKB        ;CLEAR #3 MASK.
307B E9         210          PCHL            ;BRANCH TO CALLER.
                211 ;
                212 ;
                213 ;
307C 2030       214 BTAB:    DW  CH0         ;BRANCH TABLE
307E 3730       215          DW  CH1
3080 4E30       216          DW  CH2
3082 6530       217          DW  CH3
                218 ;
                219 ;
```

Figure 21. General Purpose SETUP Routine. (Cont.)

Hardware Configurations

Figure 22 shows the detailed interconnections for interfacing a single Am9517 to an 8080A system and an 'LS373. Other 8-bit latches may also be used and Figure 23 shows several other possibilities for both single and double controller configurations. The 'LS373 and 'LS374 parts offer small 20-pin packages and low power.

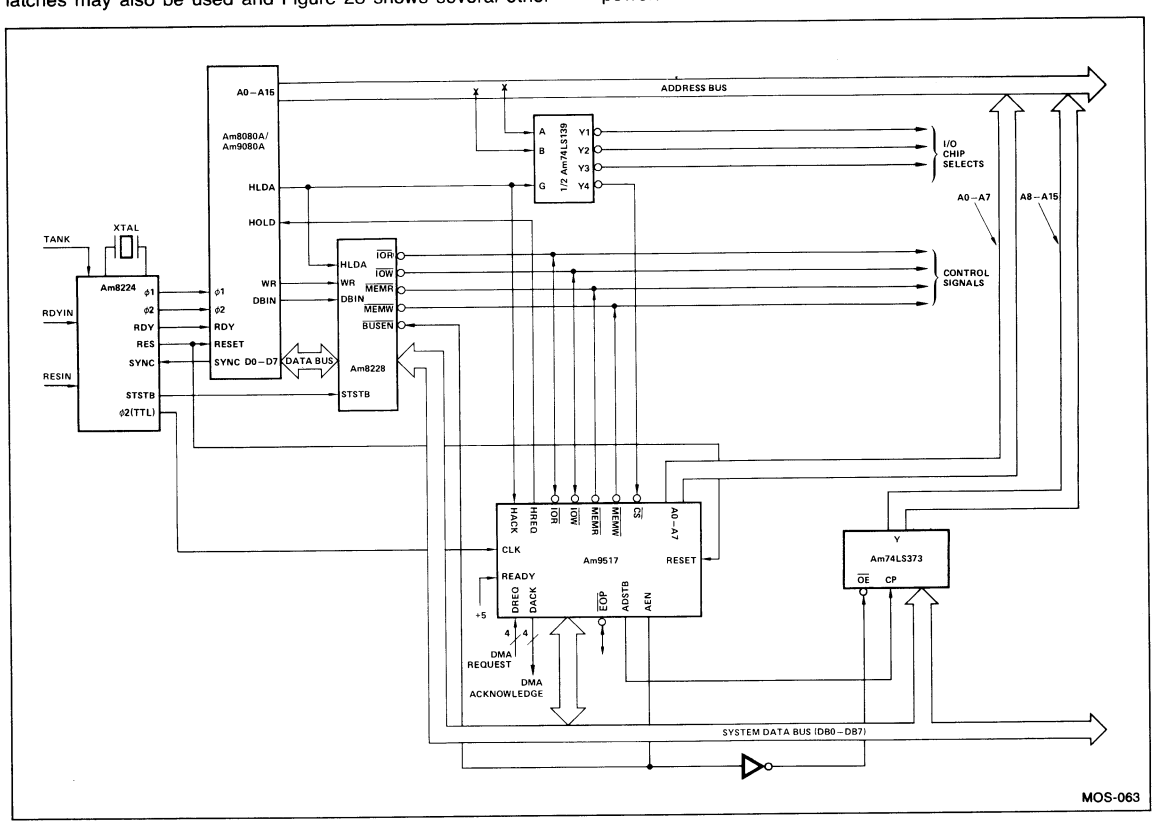


Figure 22. Am9517 Connection to 8080A System.

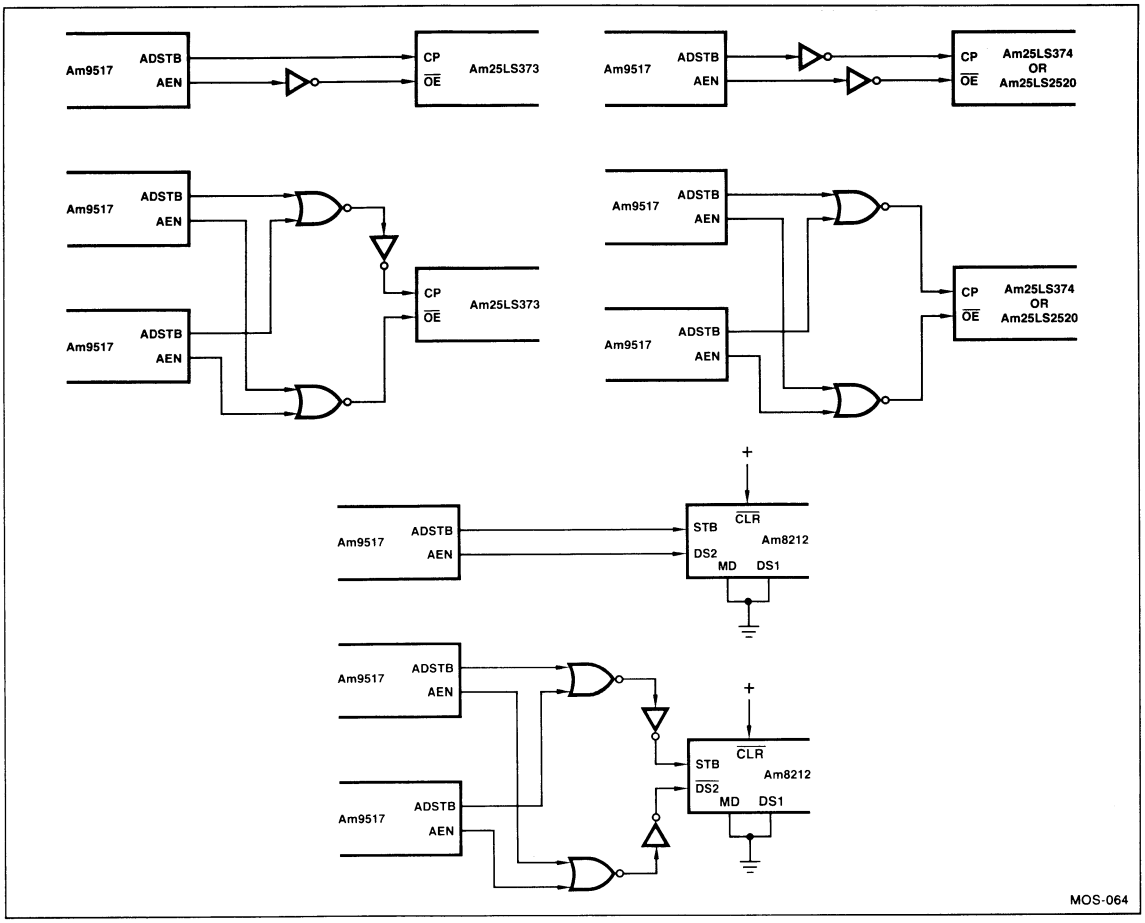


Figure 23.

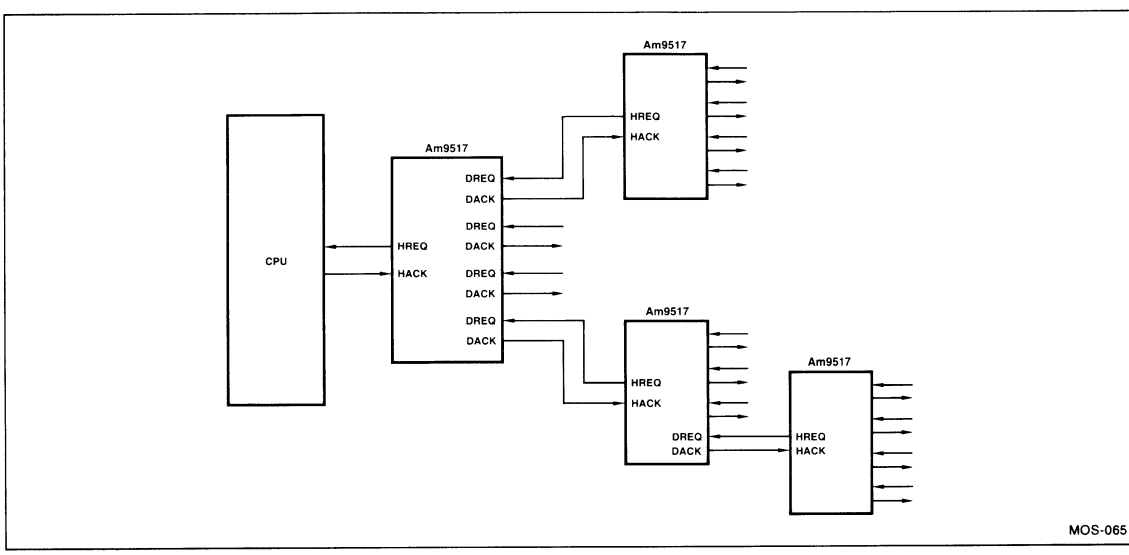


Figure 24.

Figure 24 is a block diagram of the general Am9517 expansion scheme. A detailed diagram for a seven channel setup is shown in Figure 25. A high-performance computer system is illustrated in Figure 26. There the Am9517 is used to improve the operand transfer time to the Am9511 Arithmetic Processor. Only one channel is connected in this example, but similar applications can make good use of two or even three channels. In some cases it will also be convenient to dedicate Channels 0 and 1 to memory-to-memory operations.

The Am9517 provides another significant tool for the system designer to use in the continuing quest for improved system price/performance.

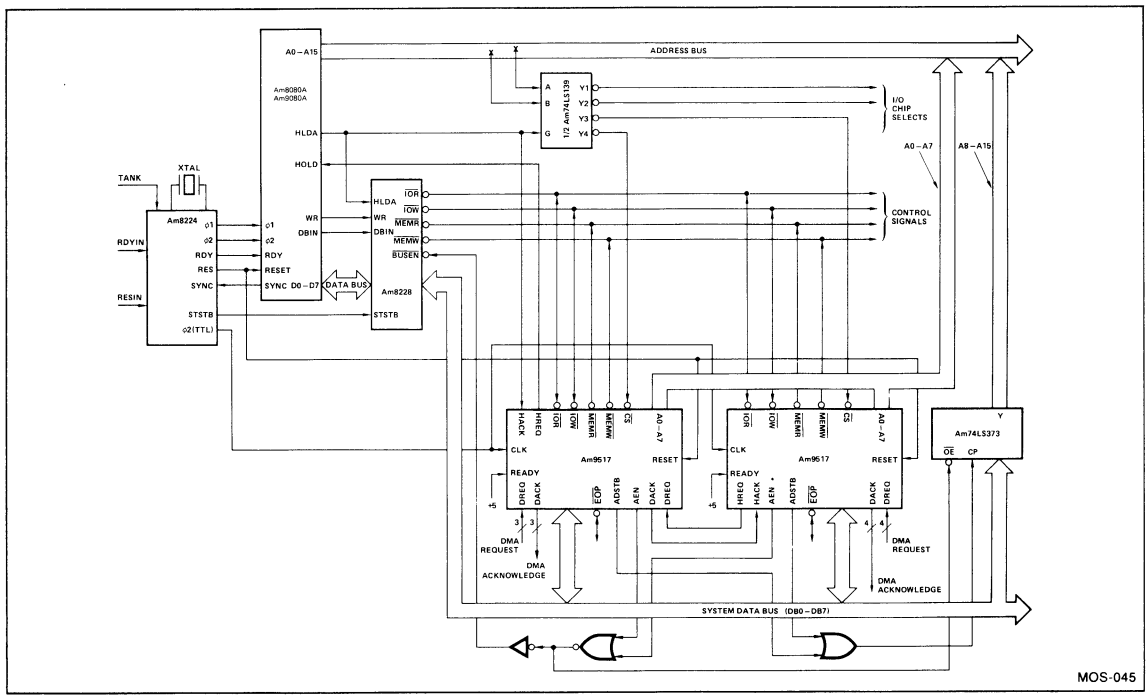


Figure 25. Expanded Am9517 Configuration.

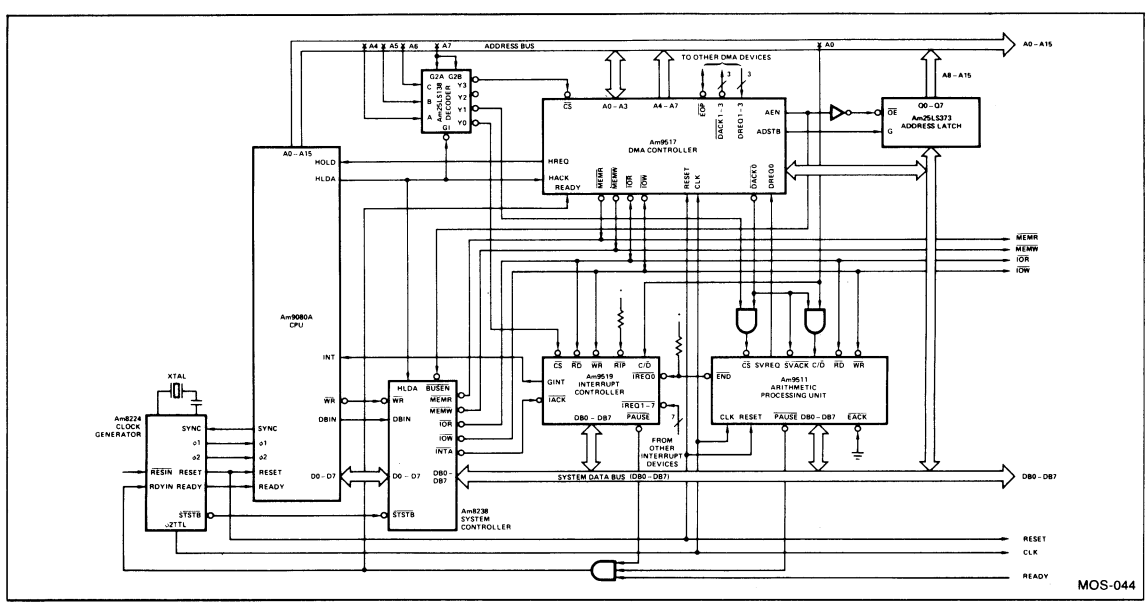


Figure 26. Am9517 Application Example.

Designing Interrupt Systems With the Am9519 Universal Interrupt Controller

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INTRODUCTION

General

Processors exist as tools for the implementation of information system transfer functions. All useful processor systems include at least one peripheral device in order to communicate with the user of the system. The processor not only manipulates information once it is in the system, but also handles the transfer of information to and from the user via the peripherals. Often several devices are integral parts of the overall system. All peripherals must be serviced in one way or another by the system processor. The basic parameters that influence the design of peripheral servicing algorithms are the frequency of service required, the service latency allowed and the service duty cycle of the devices.

There are two general methods used to initiate and coordinate this activity: Program controlled service and Interrupt driven service. In program controlled transfers, the processor schedules all peripheral events; an Interrupt driven system, on the other hand, allows modification of the system activities by external devices.

With no interrupt capability, processors must depend on software polling techniques to service peripheral devices. As the number of such devices grows and/or as the complexity of service increases, the polling program becomes very time consuming and the overhead devoted to polling becomes a significant fraction of the available processing resource. When this limits system performance, the use of interrupts can often provide substantial improvement.

Interrupts are used to enhance processor system throughput and response time by minimizing or eliminating the need for software polling procedures. Interrupts are hardware mechanisms that allow devices external to the processor to asynchronously modify the instruction sequence of the processor program being executed. An elementary single interrupt could be used simply to alert the processor to the fact that some kind of service is desired and thus to initiate a polling routine. More complex systems may have multiple interrupts and vectoring protocols which can be used to further improve performance and eliminate all polling requirements. Vectoring allows direct identification of the interrupting device and its associated service routine.

Figure 1 illustrates the essential functioning of a typical interrupt procedure. As the main program is executing instructions, an external interrupt arrives, in this example during instruction M+2.The processor completes M+2 and then, instead of executing M+3, it performs some kind of interrupt acknowledge procedure, often involving execution of an additional interrupt instruction. The result will usually be that the address of instruction M+3 is saved for future reference, and the location of instruction N is determined. The processor then proceeds to execute the interrupt service routine starting with instruction N. The service routine may save, and later restore, the processor status as well as perform tasks requested by the interrupting device. The last instruction in the routine (N+K) directs the processor to resume the main program at instruction M+3.

Notice that the presence of the hardware interrupt has caused a modification of the sequence of instruction execution; an additional block of instructions has been inserted in the main program. Interrupts provide the system designer with a significant capability that can help optimize his cost/performance tradeoffs.

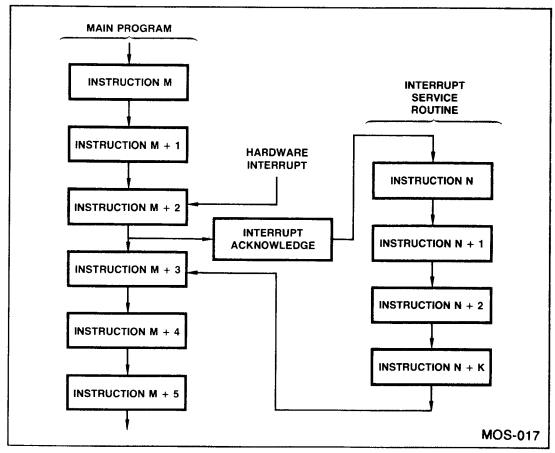


Figure 1. Basic Interrupt Procedure.

Features

The Am9519 Universal Interrupt Controller is a processor support device designed to enhance the interrupt handling capability of a wide variety of processors. A single Am9519 manages the masking, priority resolution and vectoring of up to eight interrupts. It may be easily expanded by the addition of other Am9519 chips to handle a nearly unlimited set of interrupt inputs. It offers many programmable operating options to improve both the efficiency and versatility of its host system operations. The Am9519 is well adapted to a wide range of uses including small, simple, as well as large, sophisticated, interrupt systems.

The Am9519 provides any mix of one, two, three and four byte responses to the host processor during the interrupt acknowledge process. The response bytes are all fully programmable so that any appropriate addressing, vectoring, instruction or other message protocol may be used. Contention among multiple interrupts is managed internally using either fixed or rotating priority resolution circuitry. The direct vectoring capability of the Am9519 may be bypassed using the polled mode option.

An internal mask register permits individual interrupts to be disabled. It may be loaded in parallel by the host processor with any bit pattern, or mask bits may be individually controlled. The interrupt inputs use "pulse-catching" circuitry so that an external register is not needed to capture interrupt pulses. Narrow noise pulses, however, are ignored. The interrupt polarity may be selected as either active-high or active-low.

Another important feature of the Am9519 is its ability to generate software interrupts. The host processor can set interrupt requests under program control, thus permitting hardware to resolve the priority of software tasks. This is often a powerful system asset, especially for sophisticated operating software, as well as an aid for system testing, diagnostic, debugging and maintenance procedures.

The Am9519 is implemented with AMD's LINOX n-channel silicon gate MOS technology. This process features low profile structures, triple ion-implantation, both depletion and enhancement transistors, and small, low capacitance, low power, high speed circuitry. The chip contains 4,400 transistors within a total chip area of 28,765 square mils. It is packaged in a standard 28-pin dual in-line package.

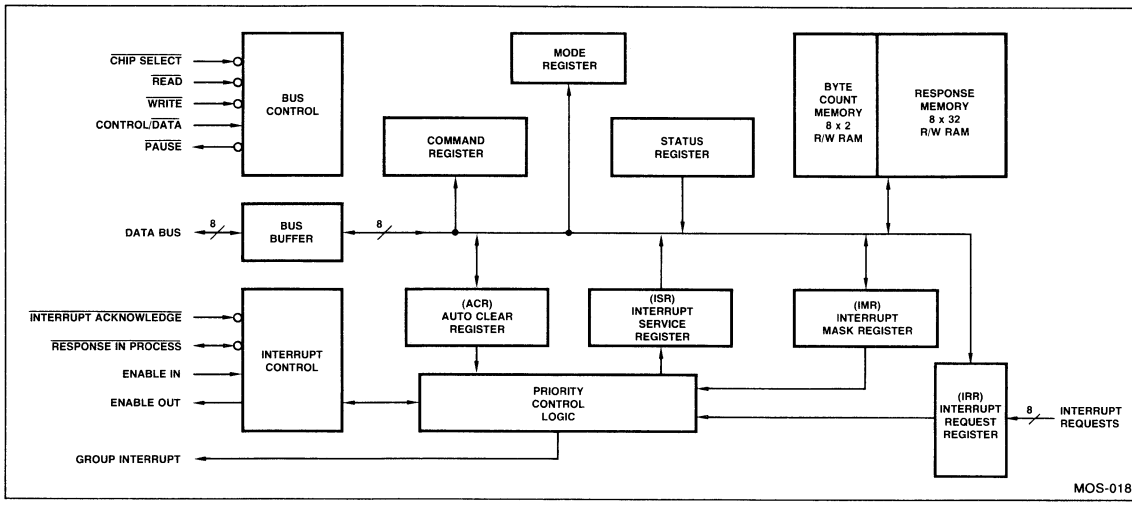


Figure 2. Am9519 Block Diagram.

HARDWARE INTERFACE

Block Diagram

The block diagram of the Am9519 shown in Figure 2 indicates the interface signals and the basic internal information flow. Interrupt Request inputs are captured and latched in the Interrupt Request register. Any requests not masked by the Interrupt Mask register will cause a Group Interrupt output to the host processor if the unit is enabled. When the processor is ready to handle the interrupt it issues an Interrupt Acknowledge pulse which causes (a) the priority of pending interrupts to be resolved and (b) a byte from the response memory associated with the highest priority interrupt to be transferred to the data bus. The transfer of additional response bytes is controlled by additional Interrupt Acknowledge signals. Other interrupt management functions are controlled by the Auto Clear register, the Interrupt Service register and the Mode register. Control of the Am9519 is exercised by the host processor using the Command register. The Status register reports on the internal condition of the part.

The Am9519 is addressed by the host processor as two distinct ports: a control port and a data port. The control port provides direct access to the Status register and the Command register. The data port is used to communicate with all other internal locations.

Interface Signal Description

Figure 3 summarizes the interface signals. Figure 4 shows the interface signal pin assignments.

Data Bus (DB)

The eight three-state bidirectional data bus lines are used to transfer information between the Am9519 and the system data bus. The direction of information flow is controlled by the $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ and $\overline{IACK}$ input signals. Data and command information are written into the device; status, data and response information are output by it.

Description	Abbreviation	Type	Pins
+5 Volts	VCC	Power	1
Ground	VSS	Power	1
Data Bus	DB	I/O	8
Response In Process	RIP	I/O	1
Interrupt Request	IREQ	Input	8
Chip Select	CS	Input	1
Read	RD	Input	1
Write	WR	Input	1
Control/Data	C/D	Input	1
Interrupt Acknowledge	IACK	Input	1
Enable In	EI	Input	1
Enable Out	EO	Output	1
Group Interrupt	GINT	Output	1
Pause	PAUSE	Output	1

Figure 3. Am9519 Interface Signal Summary.

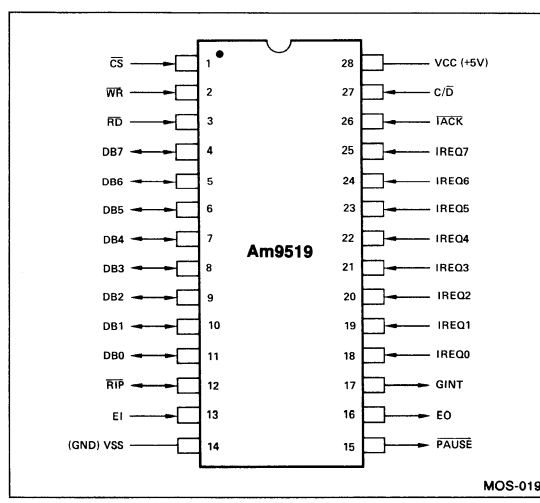


Figure 4. Connection Diagram.

Chip Select ($\overline{CS}$)

The Chip Select input is an active low signal used to condition the chip for read and write operations on the data bus; Read/Write transfers will not take place unless the $\overline{CS}$ input is low. Chip Select does not condition Interrupt Acknowledge operations. Chip Select is usually derived by decoding an address output by the host processor; the negative-true polarity matches outputs from typical decoder circuits.

Read ($\overline{RD}$)

The Read input is an active low signal conditioned by Chip Select that indicates information is to be transferred from the Am9519 to the data bus. Read is usually a timed pulse issued by the host processor.

Write ($\overline{WR}$)

The Write input is an active low signal conditioned by Chip Select that indicates information is to be transferred from the data bus to the Am9519. Write is usually a timed pulse issued by the host processor.

Control/Data (C/$\overline{D}$)

The Control/Data input acts as the port address line and is used to select source and destination locations for read and write transfers. Data transfers (C/$\overline{D}$=0) are made to or from preselected internal memory or register locations. Control transfers (C/$\overline{D}$=1) write into the command register or read from the status register.

Interrupt Request (IREQ)

The eight Interrupt Request inputs are used by external devices to indicate that service is desired. The Interrupt Request Register associated with the inputs uses asynchronous pulse-catching circuitry to latch any active requests that occur. The input polarity may be programmed to capture either positive-going or negative-going transitions. Reset selects the active low option.

Response In Process ($\overline{RIP}$)

The Response In Process signal is a bidirectional line designed to be used when two or more Am9519 circuits are connected together. $\overline{RIP}$ is used to prevent new higher priority interrupts from interferring with an Interrupt Acknowledge process that is underway. An Am9519 that is responding to a selected interrupt will treat $\overline{RIP}$ as an output and will hold the signal low until the acknowledge response is complete. An Am9519 without a selected interrupt will treat $\overline{RIP}$ as an input and will ignore $\overline{IACK}$ pulses as long as $\overline{RIP}$ is low. The $\overline{RIP}$ lines from multiple Am9519 circuits may be wired directly together. $\overline{RIP}$ is an open drain signal, and requires an external pullup resistor to VCC in order to establish the logic high level.

Group Interrupt (GINT)

When active, the Group Interrupt output indicates that at least one bit is set in the Interrupt Request Register (IRR) which is not masked by the Interrupt Mask Register or the Interrupt Service Register. GINT is used to notify the host processor that service is desired. It may be programmed for either active high or active low polarity in order to simplify the interface with the host circuitry. Reset selects active low. When active high is selected the output is a standard two-state buffer configuration. When active low is selected the output is open drain and requires an external pullup resistor to VCC in order to establish the logic high level. The open drain configuration is useful for wired-or connections in systems with more than one Am9519.

Interrupt Acknowledge ($\overline{IACK}$)

The Interrupt Acknowledge input is an active low signal generated by the host processor and used to request interrupt response information. One response byte will be transferred by the Am9519 for each $\overline{IACK}$ pulse received and up to four bytes may be transferred during each interrupt acknowledge sequence. The first $\overline{IACK}$ pulse following a GINT output also initiates the internal selection of the highest priority unmasked interrupt.

Many processors provide interrupt acknowledge signals directly, including the 8085, the 8080A and the 2650. For others, such as the Z80 and the 6800, it can be generated quite easily with simple gating.

Pause

The Pause output is an active low signal used during $\overline{IACK}$ cycles to indicate that the Am9519 has not completed the data bus transfer operation presently underway. The $\overline{IACK}$ pulse should be extended by the host processor at least until the $\overline{PAUSE}$ output goes high. The width of active $\overline{PAUSE}$ pulses is a function of several variables; it will be quite short in some systems and longer in others. $\overline{PAUSE}$ is an open drain output and requires an external pullup resistor to establish the high logic level. $\overline{PAUSE}$ signals should be wired together in multiple chip interrupt systems.

Enable In (EI)

The Enable In input is an active high signal used to implement a "daisy-chain" expansion capability with other Am9519 chips. EI may also be used as a hardware disable/enable input for the interrupt system. When EI is low, $\overline{IACK}$ inputs to the chip are ignored. Internally, a relatively high impedance resistor is connected between EI and VCC so that an unused EI requires no external pullup resistor.

Enable Out (EO)

The Enable Out output is an active high signal used to implement a "daisy-chain" expansion capability with other Am9519 chips. When the $\overline{IACK}$ input goes low, EO goes low until EI goes high and the chip determines that no unmasked request is pending. EO is a two-state output with relatively modest drive capability.

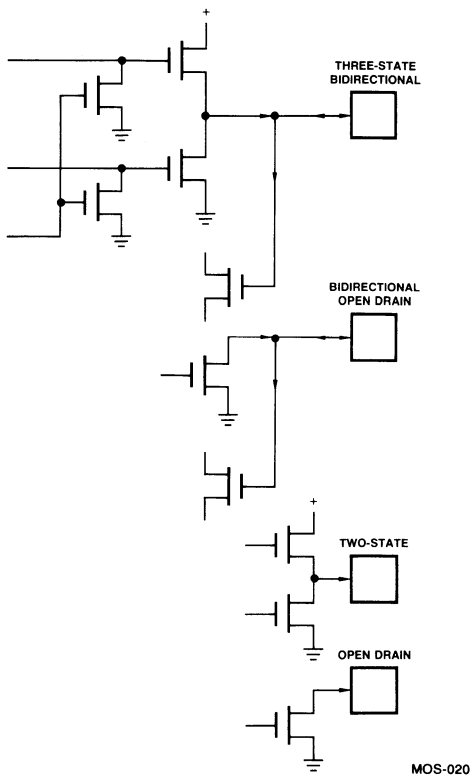
Interface Considerations

All of the input and output signals for the Am9519 are specified with logic levels identical to those of standard TTL circuits. The worst-case input logic levels are 2.0V high and 0.8V low. Except for the open drain signals, the worst-case output logic levels are 2.4V high and 0.4V low. Thus, for TTL interfacing, the normal worst-case noise immunity of at least 400mV is maintained. The logic level specifications take into account all combinations of the three variables that affect the logic level threshold: ambient temperature, supply voltage and processing parameters. A change in any of these toward nominal values will improve the actual operating margins.

The $\overline{PAUSE}$ and $\overline{RIP}$ outputs are open drain with no active pullup transistors; their output high levels are established by the external circuitry. The GINT output, when programmed for active low polarity ($\overline{GINT}$), is also an open drain output that does not control its output high level.

All of the output buffers except EO and the open drain outputs can source at least 200μA worst-case and can sink at least 3.2mA worst-case while maintaining TTL output logic levels. EO normally only drives EI of another Am9519 chip and is specified with less drive capability in order to improve the

priority resolution speed in multi-chip interrupt systems. The open drain outputs all sink at least 3.2mA as the other outputs do. Current sourcing for the open drain outputs is determined by the external circuitry. Figure 5 summarizes the types of outputs on the Am9519.



Signal	Output Description
Data Bus (DB0-DB7)	Bidirectional, Three-State
Response In Process (RIP)	Bidirectional, Open-drain
Pause	Open-drain
Group Interrupt (GINT)	Two-State when active high Open-Drain when active low
Enable Out (EO)	Two-state, low drive

Figure 5. Am9519 Output Buffer Summary and Circuitry.

Unprotected open gate inputs of high quality MOS transistors exhibit very high resistances on the order of 10^{14} ohms. It is easy in many circumstances for charge to enter the gate node of such an input faster than it can be discharged and consequently for the gate voltage to rise high enough to break down the oxides and destroy the transistor. All inputs to the Am9519 include protection networks to help prevent damaging accumulations of static charge. The protection circuitry is designed to slow the transitions of incoming current surges and to provide low impedance discharge paths for voltages beyond the normal operating levels. Please note, however, that input energy levels can nonetheless be too high to be successfully absorbed. Conventional design, storage, and handling precautions should be observed so that the protection networks themselves are not overstressed.

Within the limits of normal operation, the input protection circuitry is inactive and may be modeled as a lumped series RC as shown in Figure 6. The functionally active input connection during normal operation is the gate of an MOS transistor. Except for EI, no active sources or drains are connected to the inputs so that neither transient nor steady-state currents are impressed on the driving signals by the Am9519 other than the charging or discharging of the input capacitance and the accumulated leakage associated with the protection network and the input circuit. Lumped input capacitances are usually around 6pF and leakage currents are usually less than 1μA.

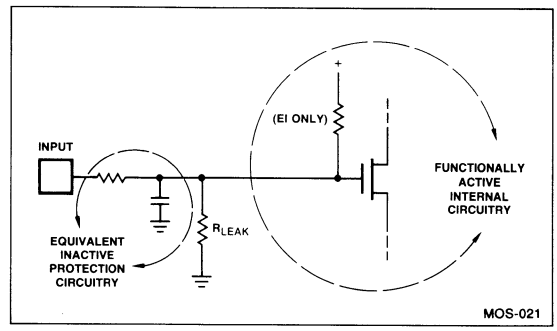


Figure 6. Input Circuitry.

Fanout from the driving circuitry into the Am9519 inputs will generally be limited by transition time considerations rather than DC current limitations when the loading is dominated by MOS circuits like the Am9519. In an operating environment, all inputs should be terminated so they do not float and accumulate stray static charges. Unused inputs should be tied directly to Ground or to VCC, as appropriate. An input in use will have some type of logic output driving it and termination during operation will not be a problem. Where inputs are driven from logic external to the card containing this chip, however, on-board termination should be provided to protect the chip when the board is unplugged and the input would otherwise float. A pull-up resistor or a simple inverter or gate will suffice.

IREQ Timing

The circuitry at the IREQ inputs is quite straightforward and is illustrated in Figure 7. Inverters 1 and 2 buffer the input and shift the logic voltages to the somewhat wider swing used internally. The exclusive-or gate is used to select the sense of the active transition edge that will set the IRR. Mode register bit M4 is used directly for control of the exclusive-or gate. The selected interface edge will always produce a negative going transition at output 3. Inverters 4, 5, 6, 7 and 8 form a delay chain. Nor gate 9 has three inputs and the IRR bit will be set when all three inputs to 9 are low. As shown in the timing diagram of Figure 8, the input to gate 9 from inverter 8 is normally low when there is no active IREQ signal at the interface. When a transition occurs, the output of gate 3 will go low and only the signal from inverter 5 prevents the immediate setting of the IRR bit. As shown in the left portion of the timing diagram, if the output from 3 has returned high before the output from 5 goes low, the IREQ transition will be ignored and the IRR bit will not be set. On the other hand, the right side of the timing diagram shows that if the active IREQ input is present long enough, then the output from both 3 and 5 will become low at the same time, and output 9 will go high. Output 8 is used to turn off Nor gate 9 after the IRR bit is set.

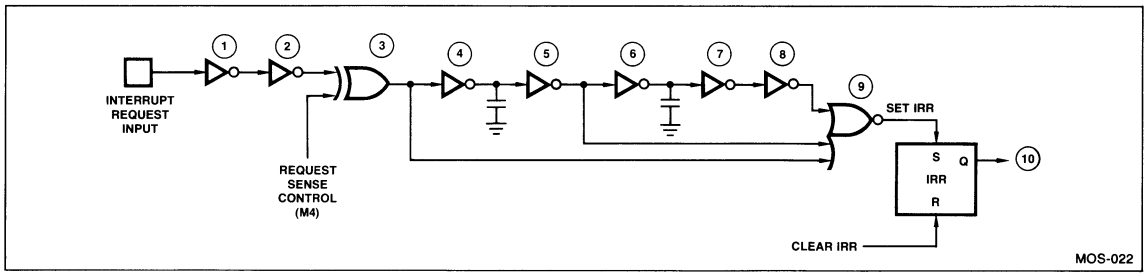


Figure 7. Interrupt Request Logic.

In summary, the input circuitry for the IREQ signals provides these characteristics:

1. Polarity for IREQ inputs is controlled;
2. Narrow IREQ pulses are ignored;
3. Wide IREQ pulses are captured;
4. Transitions to active levels are captured just once;
5. New transitions are required to generate new interrupts.

The IRR thus acts in a "pulse-catching" mode with respect to the IREQ inputs. Figure 9 shows the types of IREQ waveforms that will be recognized and latched by the IRR. Note that a transition to a level may be used although only a pulse is required; it is not necessary to maintain an IREQ input active level. Further, a continuously active level on IREQ will not cause a new interrupt each time IRR is cleared. There must be a new active transition on IREQ after IRR is cleared in order to generate a new interrupt. An active level must go inactive for a specific interval before its new active edge will be recognized.

To minimize noise sensitivity, all active IREQ pulses narrower than a specific value will be ignored by the IRR. To maintain the pulse-catching characteristics, all active IREQ pulses wider than the specified data sheet minimum will be captured by the IRR. The results for intermediate pulse widths will depend on characteristics of the particular part being used and its operating conditions, especially temperature.

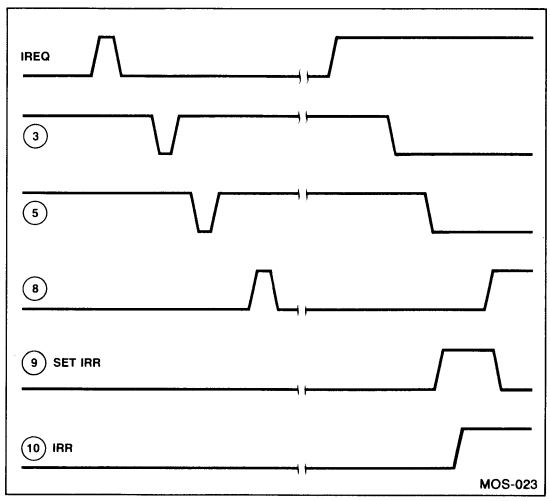


Figure 8. IREQ Internal Timing.

Power Supply

The Am9519 requires only a single +5V power supply. The commercial temperature range parts have a voltage tolerance of ±5%; the military temperature range tolerance is ±10%. Maximum supply currents are specified in the data sheet at the high end of the voltage tolerance and the low end of the temperature range. In addition, the current specifications take into account the worst-case distribution of processing parameters that may be encountered during the manufacturing life of the product. Typical supply current values, on the other hand, are specified for a nominal supply of +5.0 volts, nominal ambient temperature of 25°C, and nominal processing parameters. Supply current always decreases with increasing ambient temperature; thermal run-away is not a problem.

Although supply current will vary from part to part, a given unit at a given operating temperature will exhibit a nearly constant power drain. There is no functional operating region that will cause more than a few percent change in the supply current. Decoupling of VCC, then, is straightforward and will generally be used simply to isolate the Am9519 from external VCC noise.

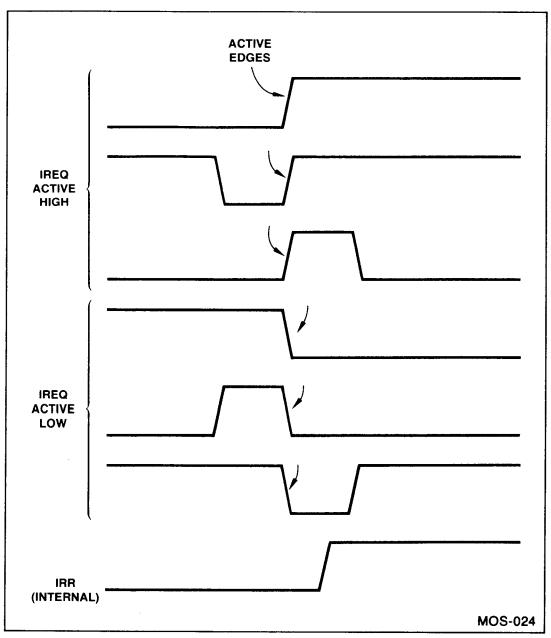


Figure 9. IREQ Waveforms.

OPERATING DESCRIPTION

Reset

The Am9519 does not include an external hardware reset input. The reset function is accomplished either by software command or automatically during power-up. The reset may be initiated by the host processor at any time simply by writing all zeros into the command port. Power-up reset circuitry is internally triggered by the rising VCC voltage when a predetermined threshold is reached, generating a brief internal reset pulse.

The response memory and byte count registers are not affected by resets. Their content after power-up are unpredictable and if they are to be used, they must first be initialized by the host processor. A software reset does not disturb previous response memory and byte count contents.

The Interrupt Mask register is set to all ones by a reset, thus disabling recognition of interrupts by the chip. The Status register continues to reflect the internal condition of the chip and is not otherwise directly affected by a reset. All other registers are cleared to all zeros by a reset. The polarities of the Mode register control bits are assigned to provide a reasonable operating option environment when cleared by a reset.

Register Description

The Am9519 uses several control and operation registers plus the response memory to perform and manage its many functions. Figure 10 lists these elements and summarizes their size and number.

Description	Abbreviation	Bit Size	Quantity
Interrupt Request Register	IRR	8	1
Interrupt Service Register	ISR	8	1
Interrupt Mask Register	IMR	8	1
Auto Clear Register	ACR	8	1
Status Register	–	8	1
Mode Register	–	8	1
Command Register	–	8	1
Byte Count	–	2	8
Response Memory	–	32	8

Figure 10. Am9519 Register and Memory Summary.

Interrupt Request Register (IRR)

The IRR is eight bits long and is used to recognize and store active transitions on the eight Interrupt Request input lines. A bit in the IRR is set whenever the corresponding IREQ input makes an inactive-to-active transition and meets the minimum active pulse width requirements. IRR bits may also be set by the host processor under program control using two types of commands. This capability allows software initiated interrupts, and is a significant tool for system testing and for sophisticated software designs.

All IRR bits are cleared by a reset. Individual IRR bits are cleared automatically when their interrupts are acknowledged by the host processor. Four types of commands, in addition to reset, allow the host program to clear IRR bits.

The IRR may be read onto the data bus by preselecting it in Mode register bits M5 and M6, followed by a read operation at the data port.

Interrupt Service Register (ISR)

The ISR is eight bits long and is used to store the acknowledge status of individual interrupts. When an $\overline{IACK}$ pulse arrives, the Am9519 selects the highest priority request that is pending, then clears the associated IRR bit and sets the associated ISR bit. When the ISR bit is programmed for automatic clearing, it is reset by the internal hardware before the end of the acknowledge sequence. When the ISR bit is not programmed for automatic clearing, it must be reset by command from the host processor.

Internally, the Am9519 uses the ISR to erect a "masking fence". When an ISR bit is set and fixed priority mode is selected, only requests of higher priority will cause a new GINT output. Thus, requests from lower priority interrupts (and from new requests associated with the set ISR bit) will be fenced out and ignored until the ISR bit is cleared. In the rotating priority mode, all requests are fenced by an ISR bit that is set, and no new GINT outputs will be generated until the ISR is cleared. When auto clear is specified, no fence is erected since the ISR bit is cleared.

If an unmasked interrupt arrives from a device of higher priority than the current ISR, GINT will go true and the host processor will be interrupted if its interrupt input is enabled. When the new interrupt is acknowledged, the associated higher priority ISR bit is set and the fence moves up to the new level. When the new ISR bit is cleared, the fence will then fall back to the previous ISR level.

The ISR may be read onto the data bus by preselecting it in Mode register bits M5 and M6, followed by a read operation at the data port.

Interrupt Mask Register (IMR)

The IMR is eight bits long and is used to enable/disable the processing of individual interrupts. Only unmasked IRR bits can cause a Group Interrupt to be generated. The IMR does not otherwise affect the operation of the IRR. An IRR bit that is set while masked will cause a GINT when its IMR bit is cleared.

All eight IMR bits may be set, cleared, read or loaded in parallel by the host processor. In addition, individual IMR bits may be set or cleared by command. This allows a control routine to directly enable and disable an individual interrupt without disturbing the other mask bits and without knowledge of their state or the system context.

The IMR polarity is active high for masking; a zero enables the interrupt and a one disables it. The power-on reset and the software reset cause all IMR bits to be set, thus disabling all requests.

Auto Clear Register (ACR)

The ACR is eight bits long and specifies the automatic clearing option for each of the ISR bits. When an auto clear bit is set, the corresponding ISR bit that has been set in an $\overline{IACK}$ cycle is cleared by the internal hardware before the end of the $\overline{IACK}$ sequence. When an auto clear bit is not set, the corresponding ISR bit that has been set in an $\overline{IACK}$ cycle is cleared by command from the host processor.

The auto clear option, when selected, provides two concomitant functional effects. First, it eliminates the need for the associated interrupt service routine to issue a command to clear the ISR bit. Secondly, it eliminates the masking fence that would otherwise have been erected, allowing lower priority interrupts to cause a new GINT output.

The ACR is loaded in parallel from the data bus by issuing the ACR load preselect command followed by a write into the data port. The ACR may be read onto the data bus by preselecting it in Mode register bits M5 and M6, followed by a read operation at the data port.

Status Register

The Status Register is eight bits long and contains information describing the internal state of the Am9519 chip. The Status register is read directly by executing a read operation at the control port. Figure 11 shows the Status bit assignments.

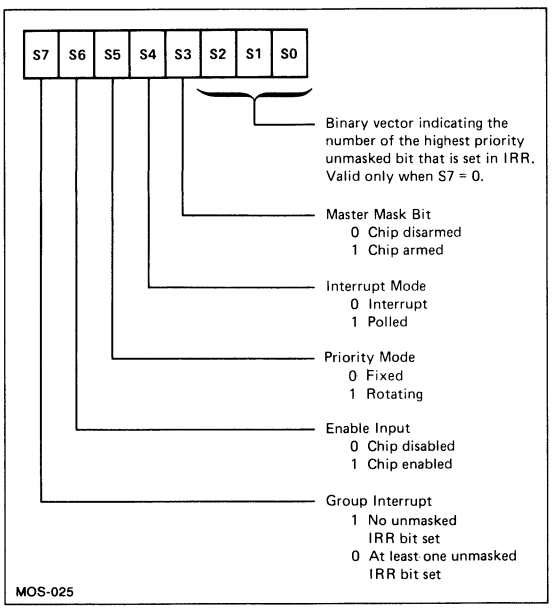


Figure 11. Status Register Bit Assignments.

The high order status bit, S7, reflects the information state of the Group Interrupt signal. Note that the polarity definition of S7 is independent of the defined polarity of GINT (Mode bit M3). Bit S7 remains valid when GINT is disabled by the polled mode option, thus permitting the host processor to check for "interrupts" by reading the Status register.

Status bit S6 reflects the state of the Enable In input signal and is used to indicate, in a multiple chip interrupt structure, which chips in the chain are disabled. When S6 is high, the chip can generate a GINT output and operation of its EO signal proceeds. When S6 is low, no GINT will be generated and EO will be forced low.

Status bit S5 reflects the state of the Priority Mode option, as specified by bit M0 of the Mode register. When S5 is high, rotating priority has been selected. When S5 is low, fixed priority has been selected.

Status bit S4 reflects the state of the Interrupt Mode option, as specified by bit M2 of the Mode register. When S4 is high, the polled mode has been selected and GINT disabled. When S4 is low, the interrupt mode has been selected.

Status bit S3 reflects the state of the Master Mask bit as specified by bit M7 of the Mode register. When S3 is low, the chip has been disarmed and IRR bits that are set will not generate GINT outputs. When S3 is high, the chip has been armed and interrupts can occur.

Status bits S2, S1 and S0 form a three bit field indicating the encoded binary number of the highest priority unmasked bit that is set in the IRR. This field should be considered invalid except when bit S7 of the Status register is low, indicating that at least one unmasked interrupt request is present. The binary coding of the field corresponds to the zero through seven numbering of the IREQ inputs. When more than one unmasked IRR bit is set, the S2, S1, S0 field will indicate the one unfenced request that is the highest priority as determined by the priority mode being used. Thus, the number of the dominant interrupt after all masking, fencing and priority resolution, is encoded into the Status register. This field is quite useful in the polled mode since it can act as a psuedo-vector for the host processor software.

Command Register

The Command Register is eight bits long and is used to store the most recently entered command. It is loaded directly from the data bus by executing a write operation at the control port. Depending on the specific command opcode that is entered, an immediate internal activity may be initiated or the part may be preconditioned for subsequent data bus transfers. The "Command Description" section of this note explains each command operation. The commands are summarized in Figure 17.

Mode Register

The Mode register is eight bits long and controls the operating modes and options of the Am9519. Figure 12 shows the bit assignments for the Mode register. No single command or interface operation will load all bits of the Mode register in parallel. The five low order bits (M0 through M4) are loaded in parallel directly from the command register. Mode bits M5, M6, and M7 are controlled by separate commands. The Mode register cannot be read out on the data bus. The data in Mode bits M0, M2, and M7 are available as part of the Status register. The Mode register is cleared by a software reset or a power-up reset. The "Operating Options" section of this note describes the detailed functions associated with each Mode bit.

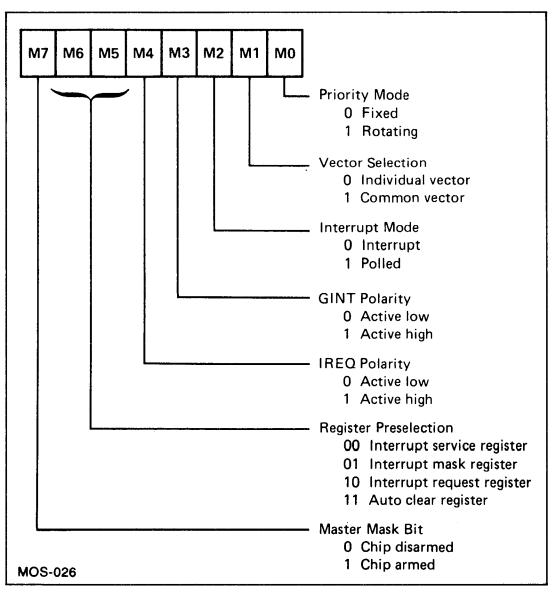


Figure 12. Mode Register Bit Assignments.

Information Transfers

Figure 13 summarizes the control signal configurations for all information transfers on the Am9519 data bus. The interface control logic assumes the following conventions:

1. $\overline{RD}$ and $\overline{WR}$ are never active at the same time.
2. $\overline{RD}$, $\overline{WR}$ and C/$\overline{D}$ are ignored unless $\overline{CS}$ is low.
3. $\overline{IACK}$ will not go low when the chip is being selected by the host.

Control Input					Data Bus Operation
$\overline{CS}$	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{IACK}$	
0	0	0	1	1	Transfer contents of data register specified by Mode bits M5, M6 to data bus.
0	0	1	0	1	Transfer contents of data bus to data register specified by Command register.
0	1	0	1	1	Transfer contents of Status register to data bus.
0	1	1	0	1	Transfer contents of data bus to Command register.
1	X	X	X	0	Transfer contents of selected response memory location to data bus.
1	X	X	X	1	No information transferred; data bus outputs off.

Figure 13. Summary of Data Bus Transfers.

When $\overline{IACK}$ is low, internal logic disables the $\overline{CS}$ input. This prevents signals on the address bus from inadvertently selecting the chip.

The host processor may read the Status register directly by simply performing a read operation with the control port selected. When a read is executed at the data port, the information transferred will be the contents of the ISR, IMR, IRR or ACR, depending on the state of Mode register bits M5 and M6.

The host processor may write directly into the command register by simply performing a write operation with the control port selected. When a write is executed into the data port, the contents of the data bus will be transferred to the ACR, IMR or response memory, depending on which command preceded the data write. Note that Mode bits M5 and M6 do not preselect the location for data write operations; only a command can do so.

When the response memory preselect command is issued, it should be followed by an appropriate number of data write operations to load 1, 2, 3, or 4 bytes of response information. If more than four bytes are written, the response memory addressing will "wrap around" and overwrite the information already entered. Response bytes are output by the Am9519 during $\overline{IACK}$ operations in the same order they were entered. Entry of response information into each new level must be preceded by a new response memory preselect command.

Interrupt Acknowledge operations are initiated by the host processor and occur following recognition of a GINT signal from the Am9519. When an $\overline{IACK}$ signal arrives, the interrupt system selects the highest priority unmasked pending interrupt request and then outputs a response byte associated with the selected interrupt. The selection process and the access of the response byte will take a variable amount of time that depends on several parameters, including:

1. the operating temperature,
2. the actual internal logic delays,
3. the number of Am9519 chips cascaded together,
4. the priority level of the interrupt being acknowledged,
5. the Mode register operating options,
6. the byte position within the response sequence.

The worst-case $\overline{IACK}$ pulse widths must be long enough to accomodate the accumulated delays that can occur in large interrupt systems operating in worst-case situations. Yet small systems operating under typical conditions will require only relatively narrow $\overline{IACK}$ pulses. The $\overline{PAUSE}$ output from the Am9519 is designed to provide interactive feedback to the host processor so that the $\overline{IACK}$ pulse width may be adaptively adjusted to meet the requirements of the actual interrupt being processed. $\overline{PAUSE}$ will go low fairly quickly following the falling edge of $\overline{IACK}$, and will return high when $\overline{IACK}$ is no longer required.

During the first $\overline{IACK}$ of a complete acknowledge sequence, the $\overline{PAUSE}$ output remains low until the highest priority interrupt has been selected and the $\overline{RIP}$ output goes low. On subsequent $\overline{IACK}$ pulses for additional responses bytes associated with the same interrupt ($\overline{RIP}$ still low), $\overline{PAUSE}$ will remain high. The Am9519 expects the first $\overline{IACK}$ input to remain low at least until the $\overline{PAUSE}$ output goes high. Subsequent $\overline{IACK}$ inputs should meet the specified input pulse width requirements as called out in the data sheet.

It will normally be convenient for the $\overline{PAUSE}$ signal to provide a "not ready" indication to the host processor which would then stall the Interrupt Acknowledge operation until $\overline{PAUSE}$ goes high. In 8080A/9080A microprocessor systems, $\overline{PAUSE}$ can be used directly in the CPU Ready logic and many other processor systems have similar coordination schemes.

Operating Options

The Mode register bits are used to establish the operating modes and conditions for the many functional features of the Am9519. The Mode register allows the host processor to personalize the interrupt system for the application at hand.

Priority Selection

Bit M0 in the Mode register specifies the priority operating mode for the Am9519. When M0=0, fixed priority is selected and the eight IREQ inputs are assigned a priority based on their physical location at the chip interface. IREQ0 has the highest priority and IREQ7 has the lowest. See Figure 14.

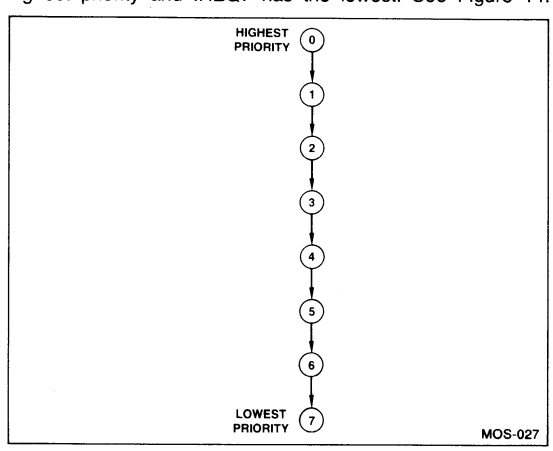


Figure 14. Fixed Priority Mode.

Priority is not resolved until the host processor initiates the interrupt acknowledge sequence. Thus, for example, an IREQ5 input may cause a GINT output to the host, but if an input on IREQ2 arrives before the falling edge of $\overline{IACK}$, then it is IREQ2 that will be selected and serviced. Notice that inherent in the fixed priority structure is the possibility that IREQ5 might never be selected and serviced as long as there are higher priority interrupts pending. IREQ2 could end up being serviced many times before IREQ5 is acknowledged. In many systems this is an appropriate method for handling the interrupting devices. Where circumstances permit, the masking capability of the Am9519 can be used by the host processor to modify the effective priority structure, perhaps by masking out recently serviced high priority devices, thus allowing lower priority inputs to be recognized.

Alternatively, where the eight interrupts have similar priority and service bandwidth requirements, the rotating priority mode may be selected (Mode register bit M0=1). As shown in Figure 15 the relative priorities remain the same as in the fixed mode; that is, IREQ2 is higher than IREQ3 which is higher than IREQ4, etc. However, in rotating priority mode, the lowest priority position in the circular chain is assigned by the hardware to the most recently serviced interrupt.

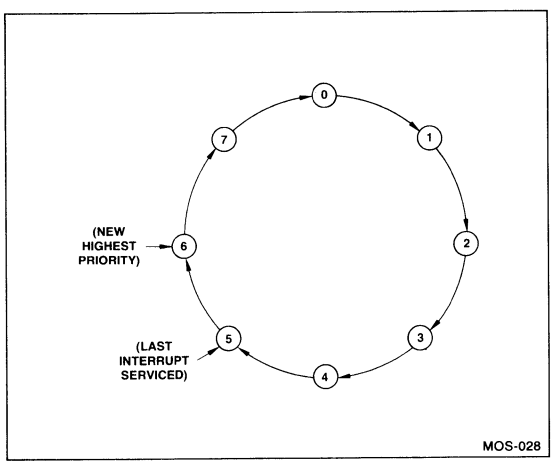


Figure 15. Rotating Priority Mode.

The example illustrated in Figure 15 assumes that IREQ5 has just finished being serviced and has therefore been assigned the lowest priority. Thus, IREQ6 occupies the new highest priority position, IREQ7 next-to-highest, etc. If two new interrupts then arrive at level 1 and level 4, IREQ1 will be selected and serviced, and will become the lowest priority. IREQ4 will then be acknowledged unless an active input on IREQ2 or IREQ3 has arrived in the meantime.

This rotating priority scheme prevents any request from dominating the system. It assures that an input will not have to wait for more than seven other service cycles before being acknowledged. Rotation occurs when the ISR bit of the presently selected interrupt is cleared.

In the rotating priority mode, inputs other than the one currently being serviced are fenced out and will not cause interrupts until the ISR bit is cleared. Thus, only one bit at a time will be set in the ISR. Care should be used when selecting the rotating mode to keep from doing so at a time when more than one ISR is set.

Vectoring

Bit M1 of the Mode register specifies the vectoring option. When M1=0 the individual vector mode is selected and each interrupt is associated with its own unique four-byte location in the response memory. When M1=1, on the other hand, the common vector mode is selected and all response information is supplied from the location associated with IREQ0, no matter which request is being acknowledged. This operating option will be useful in situations where several similar devices share a common service routine and direct individual device identification is not important. This may be true simply because of the nature of the peripheral/system interaction, or it may be a transient system condition that only uses the common vector option temporarily, perhaps to save the overhead involved in filling the response memory twice.

Polled Mode

Bit 2 of the Mode register allows the system to disable the GINT output. When M2=0 the interrupt mode is selected with the GINT output enabled. This might be considered the "normal" interrupt mode and makes full use of the interrupt control and management capabilities of the Am9519. When M2=1 the polled mode is selected which prevents the GINT output from going true by forcing it to its inactive state. In this condition, since no interrupts are supplied to the host processor, there will usually not be any $\overline{IACK}$ pulses returned to the Am9519. Consequently, ISR bits are not set, fences are not erected and IRR bits will not be automatically cleared. In the polled mode the host processor may read the Status register to determine if a request is pending and which request has the highest priority. IRR bits may be cleared by the host software. When the polled option is selected, the EI input is connected directly to the EO output thus functionally removing the polled chip from the external priority hierarchy.

Effectively, the polled mode of operation bypasses the hardware interrupt, inter-chip priority resolution, vectoring and fencing functions of the Am9519. What remains is the request latching, masking and intra-chip priority resolution.

GINT Polarity

Bit 3 of the Mode register specifies the sense of the GINT output. When M3=0, Group Interrupt is selected as active low ($\overline{GINT}$) and becomes an open drain output. This allows simple wired-or connections to other similar Am9519 outputs as well as to other sources of interrupts, and matches the polarity required by many processors. When M3=1, Group Interrupt is selected as active high (GINT) and becomes a two-state push-pull output, simplifying the interface to processors with active high interrupt inputs.

IREQ Polarity

Bit 4 of the Mode register specifies the sense of the IREQ inputs. When M4=0 the Interrupt Request signals are selected as active low ($\overline{IREQ}$) and a negative-going transition is required to set the IRR. When M4=1 the Interrupt Request signals are selected as active high (IREQ) and a positive-going transition is required to set the IRR. This sense option helps simplify the interface to interrupting devices.

Register Preselection

Bits 5 and 6 of the Mode register specify the internal data register that will be output by the Am9519 on any read operation at the data port ($\overline{CS}$=0, $\overline{RD}$=0, C/$\overline{D}$=0). These bits do not affect destinations for write operations. The four

registers available for reading are the IRR, ISR, IMR and ACR. Preselect coding for each register is shown in Figure 12. The preselection remains in effect for all data read transfers until the contents of M5 and M6 are changed.

The ability to examine these important operating registers, combined with the information available in the Status register, provides significant insight into the internal conditions of the Am9519. This allows the host processor not only enhanced dynamic operating flexibility, but also access to important diagnostic/testing/debugging information.

Master Mask

Bit 7 of the Mode register specifies the armed status of the Am9519 by way of the Master Mask control bit. When M7=0 the chip is disarmed just as if all eight bits in the IMR had been set. That is, IREQ inputs will be accepted and latched but will not cause GINT outputs to the host. In addition, the EO output is brought low, disabling any lower priority chips that may be attached. When M7=1, the chip is armed and any active unmasked interrupt inputs will be able to cause GINT outputs to the host processor.

The Master Mask capability permits the host system to disarm a chip and prevent processing of the interrupts without disturbing the contents of the IMR. Thus when the chip is re-armed, the old IMR conditions remain in effect and need not be reloaded. Note that a single command to the Master Mask bit of the highest priority interrupt chip is able to shut down the complete interrupt system, no matter how large.

Mode Reset

When a power-up or software reset occurs, the Mode register is cleared to all zeros. This means that after reset the following Mode register operating options will be in effect:

Fixed priority
Individual vectoring
Interrupt (non-polled) operation
GINT active low sense
IREQ active low sense
ISR preselected for reading
Chip disarmed by Master Mask

Operating Sequence

The management of interrupts by the Am9519 is illustrated below with a description of a fairly typical sequence of events. The Am9519 has already been initialized and enabled and is ready to run. The host processor has enabled its internal interrupt structure.

1. One (or more) of the IREQ inputs becomes active indicating that service is desired.
2. The requests are captured and latched in the IRR asynchronously. The latching action of the IRR cannot be disabled and active requests will always be stored unless a previous request at the same IRR bit has not been cleared.
3. If the active IRR bit is masked by the corresponding bit in the IMR, no further action takes place. When the IRR bit is not masked, an active Group Interrupt output will be generated if the Am9519 is not in its polled mode.
4. The GINT output from the Am9519 is used by the host processor as an interrupt input. When GINT is recognized by the host, it normally will complete the execution of its current instruction and will then execute some form of interrupt acknowledge sequence instead of the next program instruction. As part of the acknowledge cycle, the processor usually automatically disables its interrupt input. The Am9519 expects to receive one or more $\overline{IACK}$ signals from the processor during the acknowledge sequence.
5. When $\overline{IACK}$ is received, the Am9519 brings its $\overline{PAUSE}$ output low and begins selection of the highest priority unmasked active IRR bit. All interrupts that have become active before the falling edge of $\overline{IACK}$ are considered. When selection is complete, the $\overline{RIP}$ output is pulled low by the Am9519 and the contents of the first byte in the response memory associated with the selected request is accessed. $\overline{PAUSE}$ stays low until $\overline{RIP}$ goes low. $\overline{RIP}$ stays low until the last byte of the response has been transferred.
6. After $\overline{PAUSE}$ goes high, the host processor accepts the response byte on the data bus and brings the $\overline{IACK}$ line high. If another byte of response is required, another $\overline{IACK}$ pulse is output and is used by the Am9519 to access the next byte.
7. In parallel with the transfer of the first response byte, the Am9519 automatically clears the selected IRR bit and automatically sets the selected ISR bit. If the auto clear function is not in force for the selected interrupt, the ISR bit will cause a masking fence to be erected and GINT will be disabled until a higher priority interrupt arrives or until the ISR bit is cleared. The interrupt service routine will usually clear the ISR bit, often near the end of the routine.
8. If a higher priority request arrives while the current request is being serviced, and if the fixed priority mode is in effect, then GINT will be output again by the Am9519. The GINT signal will be recognized by the host processor only if the host has enabled its interrupt input. If this new request is acknowledged, the Am9519 will clear the corresponding IRR bit and set the corresponding ISR bit.
9. When the host processor has completed all interrupt service activity to satisfy the interrupting devices, it will normally clear the remaining ISR bit, if any, enable its internal interrupt system, if it has not already done so, and then return to the main program.

COMMAND DESCRIPTIONS

The Am9519 command set allows the host processor to customize and alter the interrupt operating modes and features for particular applications, to initialize and update the response locations, and to manipulate the internal controlling bit sets during interrupt servicing. Commands are entered from the data bus directly into the Command register by writing into the Am9519 control port ($\overline{CS}$=0, $\overline{WR}$=0, C/$\overline{D}$=1). All the available commands are described below and are summarized in Figure 17. In the binary coding of the commands, "X" indicates a do-not-care bit position.

RESET

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
0	0	0	0	0	0	0	0

Description: The Reset command allows the host processor to establish a known internal condition. The response memory and byte count registers are not affected by the software reset. The IMR is set to all ones. The ISR, IRR, ACR and Mode registers are cleared to all zeros.

CLEAR IRR AND IMR

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
0	0	0	1	0	X	X	X

Description: All bits in the IMR and all bits in the IRR are cleared at the same time. Thus all interrupts are enabled and the previous history of all IREQ transitions is forgotten. If GINT was active when the command was entered, it will go inactive.

CLEAR SINGLE IMR AND IRR BIT

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
0	0	0	1	1	B2	B1	B0

Description: The same single bit position is cleared in both the IMR and the IRR. Other bits are not changed. If the specified IRR bit was generating an active interrupt output, GINT may go inactive upon entry of the command. The bit position cleared is specified by the B2, B1, B0 field as shown in Figure 16.

CLEAR IMR

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
0	0	1	0	0	X	X	X

Description: All bits in the IMR are cleared to zeros. All IRR bits will therefore be unmasked and any IRR bits that had been set will be able to cause an active GINT output after the command is entered.

CLEAR SINGLE IMR BIT

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
0	0	1	0	1	B2	B1	B0

Description: A single bit in the IMR is cleared. Other bits are not changed. If the corresponding bit in the IRR was set, it will be unmasked and will be able to cause an active GINT after entry of the command. The IMR bit cleared is specified by the B2, B1, B0 field as shown in Figure 16.

SET IMR

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
0	0	1	1	0	X	X	X

Description: All bits in the IMR are set to ones. All IRR bits will therefore be masked and unable to generate an active GINT. If GINT had been active, it will go inactive after the command is entered.

SET SINGLE IMR BIT

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
0	0	1	1	1	B2	B1	B0

Description: A single bit in the IMR is set. Other bits are not changed. If the corresponding bit in the IRR was active and generating a GINT output, GINT will become inactive after the command is entered. The IMR bit set is specified by the B2, B1, B0 field as shown in Figure 16.

CLEAR IRR

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
0	1	0	0	0	X	X	X

Description: All bits in the IRR are cleared to zeros. GINT will become inactive. New transitions on the IREQ inputs will be necessary to cause an interrupt.

CLEAR SINGLE IRR BIT

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
0	1	0	0	1	B2	B1	B0

Description: A single bit in the IRR is cleared to zero. It will not cause an active GINT until it is set. The IRR bit cleared is specified by the B2, B1, B0 field as shown in Figure 16.

SET IRR

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
0	1	0	1	0	X	X	X

Description: All bits in the IRR are set to ones. Any that are unmasked will be able to cause an active GINT output. This command allows the host CPU to initiate eight interrupts in parallel.

SET SINGLE IRR BIT

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
0	1	0	1	1	B2	B1	B0

Description: A single bit in the IRR is set to a one. If it is unmasked it will be able to generate an active GINT. This command allows the host processor to simulate with software the arrival of a hardware interrupt request. It also gives the software access to the hardware priority resolution, masking and control features of the Am9519. The bit set is specified by the B2, B1, B0 field as shown in Figure 16.

CLEAR HIGHEST PRIORITY ISR BIT

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
0	1	1	0	X	X	X	X

Description: A single bit in the ISR is cleared to zero. If only one bit was set, that is the one cleared. If more than one bit was set, this command clears the one with the highest priority. This command is useful in software contexts where the service routine does not know which device is being serviced. It should be used with caution since the highest priority ISR bit may not really be the bit intended. When using the auto clear option on some interrupts and/or when a subroutine nesting hierarchy is not priority driven, the highest priority ISR bit may not correspond to the one being serviced.

CLEAR ISR

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
0	1	1	1	0	X	X	X

Description: All bits in the ISR are cleared to zeros. Mask fencing is eliminated.

CLEAR SINGLE ISR BIT

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
0	1	1	1	1	B2	B1	B0

Description: A single bit in the ISR is cleared to zero. If the bit was already cleared, no effective operation takes place. The bit cleared is specified by the B2, B1, B0 field as shown in Figure 16. This will be the most useful command for service routines to use in managing the ISR without the help of the auto-clear option.

LOAD MODE BITS M0 THROUGH M4

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	0	0	M4	M3	M2	M1	M0

Description: The five low order bits of the Command register are transferred into the five low order bits of the Mode register. This command controls all of the Mode options except the master mask and the register preselection.

CONTROL MODE BITS M5, M6, M7

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	0	1	0	M6	M5	N1	N0

Description: The M6, M5 field in the command is loaded into the M6, M5 locations in the Mode register. This field controls the register preselection bits in the Mode register. The N1, N0 field in the command controls Mode bit M7 (Master Mask) and is decoded as follows:

N1	N0	
0	0	No change to M7
0	1	Set M7
1	0	Clear M7
1	1	(Illegal)

Thus, this command may be considered as three distinct commands, depending on the coding of N1 and N0:

1. Load M5, M6 only
2. Load M5, M6 and set M7
3. Load M5, M6 and clear M7

The Command Summary in Figure 17 lists all three versions.

PRESELECT IMR FOR WRITING

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	0	1	1	X	X	X	X

Description: The IMR is targeted to be loaded from the data bus when the next write operation occurs at the data port. All subsequent data write operations will also load the IMR until a different command is entered. Read operations may be successfully inserted between the entry of this command and the subsequent writing of data into the IMR. The Mode register is not affected by this command.

PRESELECT ACR FOR WRITING

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	1	0	0	X	X	X	X

Description: The ACR is targeted to be loaded from the data bus when the next write operation occurs at the data port. All subsequent data write operations will also load the ACR until a different command is entered. Read operations may be successfully inserted between the entry of this command and the subsequent writing of data into the ACR. The Mode register is not affected by this command.

PRESELECT RESPONSE MEMORY FOR WRITING

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	1	1	BY1	BY0	L2	L1	L0

Description: One level in the response memory is targeted for loading from the data bus by subsequent data write operations. The byte count register for that level is loaded from the BY1, BY0 field in the command. The L2, L1, L0 field specifies which of the eight response levels is being selected. This command should be followed by one to four data write operations to load response bytes. Field coding:

BY1	BY0	Count
0	0	1
0	1	2
1	0	3
1	1	4

L2	L1	L0	Level
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

The byte count value does not control the number of bytes entered into the response memory. It does control the number of bytes read from the memory by $\overline{IACK}$ pulses. Response bytes are output by the Am9519 in the same order they were entered.

B2	B1	B0	Bit Specified
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Figure 16. Coding of B2, B1, B0 Field of Commands.

COMMAND CODE								COMMAND DESCRIPTION
7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
0	0	0	1	0	X	X	X	Clear all IRR and all IMR bits
0	0	0	1	1	B2	B1	B0	Clear IRR and IMR bit specified by B2, B1, B0
0	0	1	0	0	X	X	X	Clear all IMR bits
0	0	1	0	1	B2	B1	B0	Clear IMR bit specified by B2, B1, B0
0	0	1	1	0	X	X	X	Set all IMR bits
0	0	1	1	1	B2	B1	B0	Set IMR bit specified by B2, B1, B0
0	1	0	0	0	X	X	X	Clear all IRR bits
0	1	0	0	1	B2	B1	B0	Clear IRR bit specified by B2, B1, B0
0	1	0	1	0	X	X	X	Set all IRR bits
0	1	0	1	1	B2	B1	B0	Set IRR bit specified by B2, B1, B0
0	1	1	0	X	X	X	X	Clear highest priority ISR bit
0	1	1	1	0	X	X	X	Clear all ISR bits
0	1	1	1	1	B2	B1	B0	Clear ISR bit specified by B2, B1, B0
1	0	0	M4	M3	M2	M1	M0	Load Mode register bits 0–4 with specified pattern
1	0	1	0	M6	M5	0	0	Load Mode register bits 5, 6 with specified pattern
1	0	1	0	M6	M5	0	1	Load Mode register bits 5, 6 and set Mode bit 7
1	0	1	0	M6	M5	1	0	Load Mode register bits 5, 6 and clear Mode bit 7
1	0	1	1	X	X	X	X	Preselect IMR for subsequent loading from data bus
1	1	0	0	X	X	X	X	Preselect ACR for subsequent loading from data bus
1	1	1	BY1	BY0	L2	L1	L0	Load BY1, BY0 into byte count register and preselect response memory level specified by L2, L1, L0 for subsequent loading from data bus

Figure 17. Am9519 Command Summary.

SYSTEM INTERFACE

Expansion

Several Am9519 chips may be cascaded to expand the number of interrupts than can be handled by the system. A two-chip configuration is shown connected to an 8080A/9080A microprocessor in Figure 18. In general, expansion past a single Am9519 will require simply an added Chip Select signal for each extra chip, and perhaps an inverter for the GINT signal if the processor interrupt input is active-high. The $\overline{\text{GINT}}$, $\overline{\text{PAUSE}}$, and $\overline{\text{RIP}}$ signals are all designed to be wire-OR'ed in expanded systems.

Priority management in expanded systems is controlled by the Enable In, Enable Out and Response In Process signals. Figure 19 shows the basic interconnections for an example interrupt system that can accept up to 40 interrupts, using five Am9519 chips. Notice that $\overline{\text{IACK}}$ is wired in parallel to all five circuits, and that the $\overline{\text{GINT}}$, $\overline{\text{RIP}}$, and $\overline{\text{PAUSE}}$ lines are respectively tied together. The three pullup resistors are used to establish the high logic levels for the open-drain outputs. Enable In of the first chip (A) is allowed to float, or may be tied high. Each Enable Out signal is connected to the next lower level Enable In input. Each chip accepts eight IREQ inputs; for purposes of this example it is assumed that an active interrupt arrives at chip D in the chain.

Figure 20 shows the timing relationships for the configuration of Figure 19. When the IREQ arrives, a $\overline{\text{GINT}}$ output is generated by chip D and is used to interrupt the host processor. When the host returns an $\overline{\text{IACK}}$ pulse, all the EO lines are brought low in parallel. $\overline{\text{PAUSE}}$ also goes low, and is used to extend the $\overline{\text{IACK}}$ pulse.

After the fall of $\overline{\text{IACK}}$, all chips wait until a brief internal delay elapses and then examine EI. If EI is low, internal activity is suspended until EI goes high. If EI is high, then the internal circuitry is checked to see if an unmasked request is pending. If so, $\overline{\text{RIP}}$ is brought low, $\overline{\text{PAUSE}}$ is brought high, EO is kept low, and the first response byte is output on the data bus. In this example, there is no request in chip A and therefore the EO(A) line is brought high. This then allows chip B to see if it has an unmasked request waiting for service. If not, EO(B) goes high also and, with no interrupts at C, EO(C) goes high, driving EI(D) high. Since chip D finds a waiting request, it does not bring EO(D) high but it does bring $\overline{\text{RIP}}$ low. When $\overline{\text{RIP}}$ goes low it allows all the $\overline{\text{PAUSE}}$ outputs to switch high which permits the termination of the $\overline{\text{IACK}}$ pulse.

It can be seen, then, that the $\overline{\text{PAUSE}}$ output will automatically adjust the position of its rising edge to accommodate the exact functional and operational conditions that occur for each particular $\overline{\text{IACK}}$ cycle. For larger systems, like that in Figure 19, operating at high temperatures with slow versions of the Am9519 and servicing low priority interrupts, the processor delay caused by $\overline{\text{PAUSE}}$ may be quite long and a few processor wait cycles may be required to extend the $\overline{\text{IACK}}$ pulse. On the other hand, when a system like Figure 18 is running at typical room temperatures with typical parts and the interrupt is a high priority one, the $\overline{\text{PAUSE}}$ output width will be quite narrow and no wait cycles will be necessary.

The $\overline{\text{RIP}}$ output serves two basic functions within the interrupt system. First, its falling edge informs the other connected chips that an interrupt request has been selected and $\overline{\text{PAUSE}}$ may, therefore, be released. Secondly, as long as $\overline{\text{RIP}}$ is low, only the single chip that is pulling $\overline{\text{RIP}}$ down is allowed to respond to $\overline{\text{IACK}}$ inputs. $\overline{\text{RIP}}$ stays low until all response bytes for the selected interrupt have been transferred.

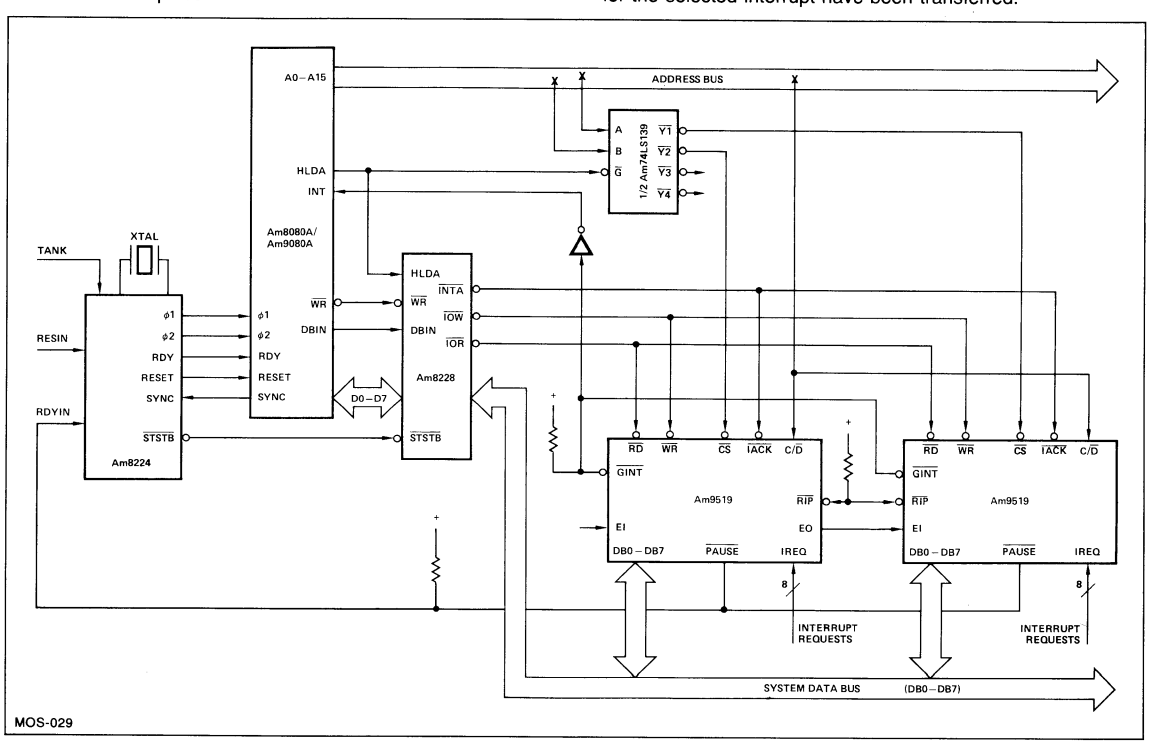


Figure 18. 16 Interrupt Configuration with 8080A/9080A.

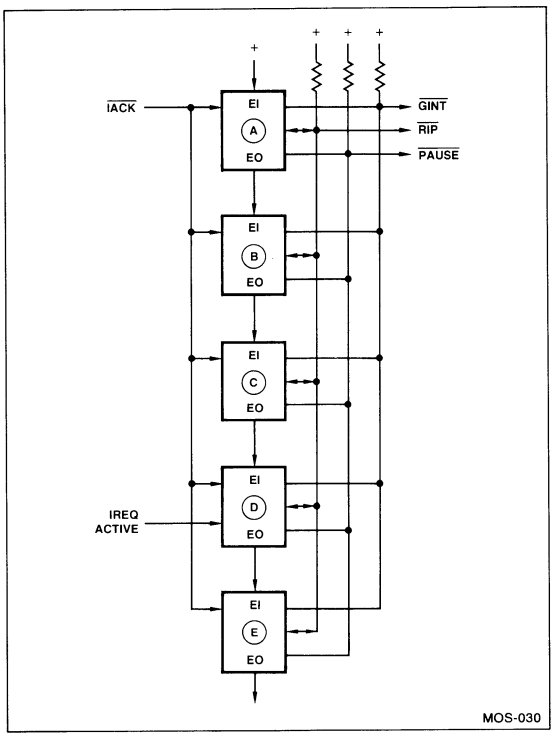


Figure 19. Five-Chip Expansion Example.

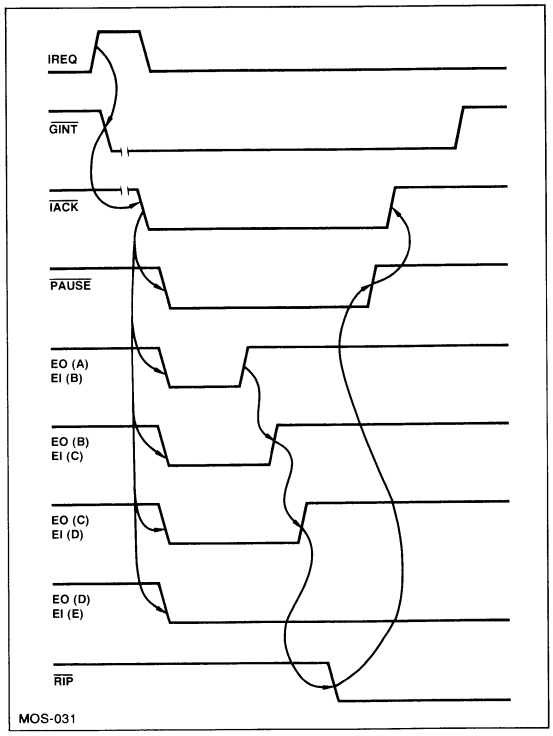


Figure 20. Inter-Chip Priority Resolution.

Assume that a new interrupt arrives at chip B in Figure 19 during the time that the first byte of a multibyte response for the interrupt at chip D is being transferred. Without the $\overline{RIP}$ signal there would be confusion when the second $\overline{IACK}$ pulse arrives. Both chips might try to send out response bytes since the interrupt at chip B is a higher priority, yet chip D is in the midst of a response sequence. With $\overline{RIP}$ present, however, no problem arises. Chip D pulls $\overline{RIP}$ low when it is selected and keeps $\overline{RIP}$ low until its response is complete. Chip B treats $\overline{RIP}$ as an input and will not respond to $\overline{IACK}$ until $\overline{RIP}$ goes high.

Initialization and Support

Before the Am9519 can perform useful work, it must be initialized to customize it for a particular application and to load it with appropriate data values. During active operation, control options may be changed and response data may be modified. Because of the many ways it might be used, the Am9519 can be programmed using many different approaches. The following sequence description shows only one of several possible methods for constructing a basic service routine:

1. Disable processor interrupts.
2. Execute software reset at Am9519.
3. Transfer commands and response data from a control table into the Am9519.
4. Transfer operating options into the Mode register.
5. Transfer the operating Mask conditions into the IMR.
6. Clear the IRR.
7. Clear Master Mask.
8. Enable processor interrupts.
9. Return.

Figure 21 shows an example listing for such a routine using 8080A/9080A coding. Several assumptions are made about the hardware and software environment in which the routine will function:

1. When the routine is entered, register pair H, L contains the address of the first location of a control table, and register B contains a count that indicates how many entries the table contains.
2. One Am9519 is in the system. Its data port is decoded by the hardware as hex I/O address C2. Its control port is hex I/O address C3.
3. Only the first five interrupts will be in use by the main program. The others will be used later to support other processes.
4. Main program options: Fixed priority, Individual vectoring, Interrupt mode, GINT active high, IREQ active low, IRR selected for reading, Auto clear not used.

The control table is an important part of the routine and contains command information as well as the response data itself. The table consists of up to eight entries, each up to five bytes long, with all entries the same length. The first byte of each entry contains the response memory preselect command code with fields for the BY1, BY0 byte count and the L2, L1, L0 level pointer. The next one to four bytes of each entry contain the data loaded into the response memory. In this example the table has entries of four bytes each and is illustrated in Figure 22.

This type of table organization may contain extra bytes, but it compensates for this by allowing a brief, simple program to handle it. The table is fairly general and allows any length response to be programmed independently for each interrupt. It

```
LOC  OBJ          SEQ          SOURCE STATEMENT

                    0 ;
                    1 ;       * * * * * * * * * * * * * * * * * * * *
                    2 ;       *                                       *
                    3 ;       *          EXAMPLE PROGRAM              *
                    4 ;       *  FOR CONTROL AND INITIALIZATION       *
                    5 ;       *          OF THE AM9519                *
                    6 ;       *  UNIVERSAL INTERRUPT CONTROLLER       *
                    7 ;       *                                       *
                    8 ;       * * * * * * * * * * * * * * * * * * * *
                    9 ;
                   10 ;
                   11 ;
3000               12           ORG 3000H
                   13                                ;
00C3               14 CPORT     EQU 0C3H             ; CONTROL PORT ADDRESS.
00C2               15 DPORT     EQU 0C2H             ; DATA PORT ADDRESS.
00B0               16 IMASK     EQU 10110000B        ; LOAD MASK COMMAND.
00E0               17 MASK1     EQU 11100000B        ; MASK VALUE TO ENABLE THE FIRST
                   18                                ;   FIVE INTERRUPTS.
0088               19 MODE1     EQU 10001000B        ; MODE COMMAND FOR 'NORMAL'
                   20                                ;   OPERATION. (M0 - M4 ONLY)
00A9               21 MODE2     EQU 10101001B        ; MODE COMMAND TO CLEAR MASTER
                   22                                ;   MASK AND PRESELECT IRR.
0040               23 CLIRR     EQU 01000000B        ; CLEAR IRR COMMAND.
                   24                                ;
                   25                                ;
3000 F3            26 ENTRY:    DI                   ; DISABLE CPU INTERRUPTS
3001 3E00          27           MVI A,00000000B      ; GET SOFTWARE RESET COMMAND AND
3003 D3C3          28           OUT CPORT            ; SEND TO CONTROL PORT.
                   29                                ;
3005 7E            30 AAA:      MOV A,M              ; GET CONTROL BYTE FROM TABLE &
3006 D3C3          31           OUT CPORT            ; SEND TO CONTROL PORT.
3008 23            32           INX H                ; INCREMENT TABLE POINTER.
3009 0E03          33           MVI C,3              ; INITIALIZE VECTOR BYTE COUNT.
300B 7E            34 BBB:      MOV A,M              ; GET VECTOR BYTE AND
300C D3C2          35           OUT DPORT            ; SEND TO DATA PORT.
300E 23            36           INX H                ; POINT TO NEXT TABLE BYTE.
300F 0D            37           DCR C                ; DECREMENT BYTE COUNT.
3010 C20B30        38           JNZ BBB              ; ENTRY DONE?  NO:BACK TO BBB.
3013 05            39           DCR B                ; YES:DECREMENT ENTRY COUNTER.
3014 C20530        40           JNZ AAA              ; TABLE DONE? NO:BACK TO AAA.
                   41                                ;
3017 3E88          42           MVI A,MODE1          ; YES: PROCEED WITH MODE BYTE.
3019 D3C3          43           OUT CPORT            ; SEND MODE TO CONTROL PORT.
301B 3EB0          44           MVI A,IMASK          ; GET MASK LOAD COMMAND AND
301D D3C3          45           OUT CPORT            ; SEND TO CONTROL PORT.
301F 3EE0          46           MVI A,MASK1          ; GET OPERATING MASK AND
3021 D3C2          47           OUT DPORT            ; SEND TO DATA PORT.
3023 3E40          48           MVI A,CLIRR          ; GET CLEAR IRR COMMAND AND
3025 D3C3          49           OUT CPORT            ; SEND TO CONTROL PORT.
3027 3EA9          50           MVI A,MODE2          ; GET CLEAR MASTER MASK COMMAND
3029 D3C3          51           OUT CPORT            ; AND SEND TO CONTROL PORT.
302B FB            52           EI                   ; ENABLE CPU INTERRUPTS.
302C C9            53           RET                  ; RETURN TO CALLING PROGRAM.
                   54                                ;
                   55           END
```

Figure 21. Example Routine.

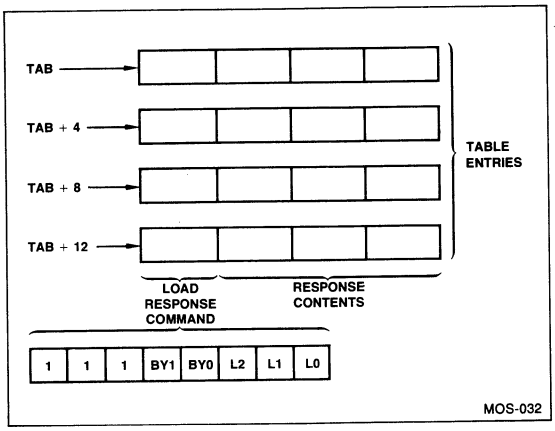


Figure 22. Example Control Table.

also allows any number of response locations to be updated in any order. The program driving the table simply assumes that every response level receives the same number of bytes as the level with the longest response.

Other table organizations are also possible. A more general table could contain the IMR value to be used, the ACR value, the table byte length, the operating mode values, etc. As more of the variable control information is added to the table, the software routine becomes more general and can be used not only for initialization, but for operational changes as well. Then there might be several tables in memory with an address supplied to the routine that points to the controlling table to be used. Note that the calling program can use just portions of an existing table if desired, simply by controlling the contents of the machine registers when the routine is entered.

Another approach is to omit the byte count/level command code from the table and compute its value in the driving routine. This may be especially appropriate when all the response entries are the same length and contiguous levels are being filled. The BY1, BY0 field need not change then, and a simple increment instruction will generate the proper command coding by changing the L2, L1, L0 field. To minimize the table length, which might become an important consideration for larger systems with many more interrupts, it is also possible to use the byte count to control the number of bytes transferred into each memory level.

The Am9519 offers new levels of versatility and sophistication for interrupt systems. It represents interesting opportunities for both hardware and software engineers to enhance new designs and to take advantage of the features now available.

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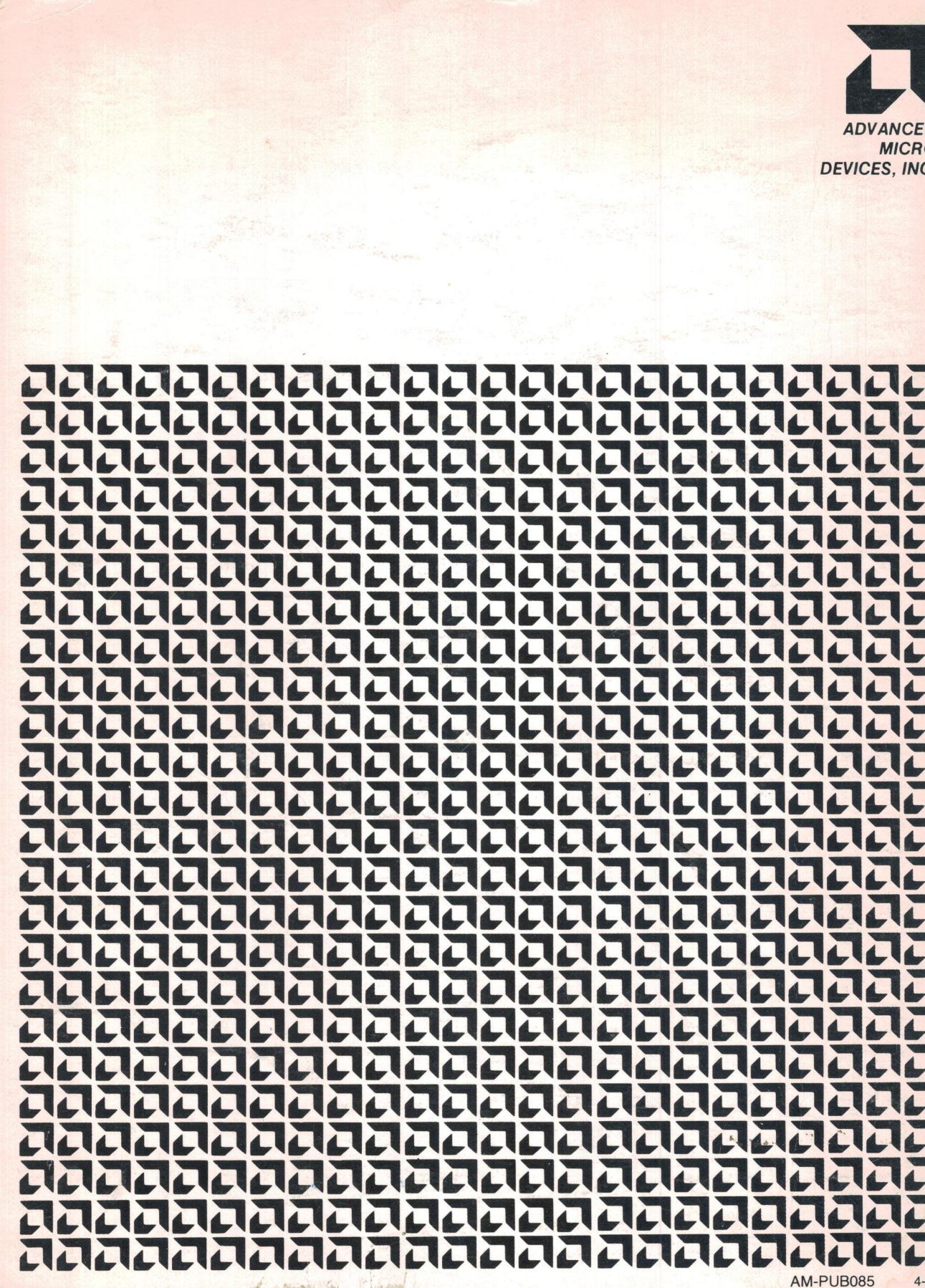

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